ONFI Technical Errata

Errata ID	**025**
Affected Spec Ver.	**ONFI 3.0, 3.1, 3.2, 4.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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This errata updates Zio Input/Ouput Zpkg spec for 800MT/s from 40 Ohms Min to 35 Ohms Min. To align Min value with other I/O speeds and to support new package technology.

The errata removes language which imposes a Timing Mode 0, 100ns maximum limit for for the clock period in NV-DDR and tDSC and tRC specs in NV-DDR2/3. This allows Timing Mode 0 in NV-DDR/NV-DDR2/3 to support slower operation.

The errata also corrects the description for NV-DDR2 and NV-DDR3 differential signaling Reset(FFh) behavior.

Description of the specification change

Update table 45 Package Electrical Specifications for 800 MT/s Min value currently set at 40 Ohms to 35 Ohms. This will align the 800 MT/s with both slower speed and higher speed devices that will be introduced with ONFI 4.1. This will accommodate a potential new 3-layer package technology that could reduce the impedance of the signals.

ONFI 4.0

Section 4.10.3. Package Electrical Specification and Pad Capacitance

Table 45 Package Electrical Specifications

Current Table

Symbol	Parameter	<=400 MT/s		533 MT/s		667 MT/s		800 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Z_{IO}	Input/Output Zpkg	35	90	35	90	35	90	40	90	Ohms
Td_{IO}	Input/Output Pkg Delay	-	160	-	160	-	100	-	80	ps
Td_{IO}Mismatch	Input/Output Pkg Delay Mismatch	-	50	-	25	-	25	-	25	ps
D $Z_{IO\ DQS}$	Delta Zpkg for DQS_t and DQS_c	-	10	-	10	-	10	-	10	Ohms
D $Td_{IO\ DQS}$	Delta Pkg Delay for DQS_t and DQS_c	-	10	-	10	-	10	-	10	ps
D $Z_{IO\ RE}$	Delta Zpkg for RE_t and RE_c	-	10	-	10	-	10	-	10	Ohms
D $Td_{IO\ RE}$	Delta Pkg Delay for RE_t and RE_c	-	10	-	10	-	10	-	10	ps

NOTE:

Proposed New Table
ONFI 4.0
Table 45 Package Electrical Specifications

Symbol	Parameter	<=400 MT/s		533 MT/s		667 MT/s		800 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Z_{IO}	Input/Output Zpkg	35	90	35	90	35	90	35 ~~40~~	90	Ohms
Td_{IO}	Input/Output Pkg Delay	-	160	-	160	-	145	-	130	ps
$Td_{IO\ RE}$	Input/Output Pkg Delay	-	160	-	160	-	145	-	130	ps
Td_{IO}Mismatch	Input/Output Pkg Delay Mismatch	-	50	-	40	-	40	-	40	ps
D $Z_{IO\ DQS}$	Delta Zpkg for DQS_t and DQS_c	-	10	-	10	-	10	-	10	Ohms
D $Td_{IO\ DQS}$	Delta Pkg Delay for DQS_t and DQS_c	-	10	-	10	-	10	-	10	ps
D $Z_{IO\ RE}$	Delta Zpkg for RE_t and RE_c	-	10	-	10	-	10	-	10	Ohms
D $Td_{IO\ RE}$	Delta Pkg Delay for RE_t and RE_c	-	10	-	10	-	10	-	10	ps

Modify Section 4.18.2 "NV-DDR"

Table 85 describes the standard NV-DDR data interface timing modes. The host is not required to have a clock period that exactly matches any of the clock periods listed for the standard timing modes. The host shall meet the setup and hold times for the timing mode selected. If the host selects timing mode *n* using Set Features, then its clock period shall be faster than the clock period of timing mode *n-1* and slower than or equal to the clock period of timing mode **n**. For example, if the host selects timing mode 2, then the following equation shall hold:
30 ns > host clock period >= 20 ns

~~If timing mode 0 is selected, then the clock period shall be no slower than 100 ns. The only exception to this requirement is when the host is issuing a Reset (FFh) in SDR timing mode 0 (see section 4.5)~~

Modify Section 4.18.3 "NV-DDR2/NV-DDR3"

The timing modes shall meet the testing conditions defined in Table 29. For speeds faster than 200 MT/s, the timing parameters are verified using the 35 Ohm drive strength, differential signaling for both RE_n (RE_t/RE_c) and DQS (DQS_t/DQS_c) signals, and external VREFQ. For speeds faster than 533 MT/s, the timing parameters are verified with ZQ calibration performed. For speeds faster than 200 MT/s, implementations may use alternate drive strength settings, single-ended signaling, and/or internal VREFQ; verification of timing parameters in these cases is left to the implementer. ~~If timing mode 0 is selected, then the tRC and tDSC period shall be no slower than 100 ns.~~

Modify Section 4.14 "Differential Signaling (NV-DDR2/NV-DDR3)"

~~If there is a Reset (FFh) operation, differential signaling is disabled.~~ In NV-DDR2, if there is a Reset (FFh) operation, differential signaling is disabled. In NV-DDR3 however, differential signaling settings are retained across a Reset (FFh) operation. Synchronous Reset (FCh) and Reset LUN (FAh) have no effect on differential signaling.

Disposition log

07/25/2017	Erratum captured for package change.
09/21/2017	Erratum captured for timing mode 0 period limit.
09/28/2917	Erratum captured for differential signaling Reset(FFh) behavior (NV-DDR2/NV-DDR3)

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