ONFI Technical Errata

Errata ID	**007**
Affected Spec Ver.	**ONFI 3.0, 3.1, 3.2, 4.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
Terry Grunzke	Micron	12/23/14

The erratum clarifies definition of ILO (output leakage), separates output leakage for Pull-Up and Pull-Down, and proposes new values for output leakage.

The erratum also fixes an error in measurement description for pad input/output capacitance.

Description of the specification change

Modify Section 2.12 "DC and Operating Characteristics", shown below:

The maximum input leakage current requirements (ILI) in **Error! Reference source not found.**, Table 12, Table 13 and 14 are tested across the entire allowed VccQ range, specified in **Error! Reference source not found.**. The maximum output leakage current requirements (ILO) in **Error! Reference source not found.** ~~and~~ **Error! Reference source not found.** -are tested across the entire allowed VccQ range, specified in **Error! Reference source not found.**. Table 15 specifies output leakage current requirements (ILO) with VOUT for conditions of VccQ of 1.8V and 1.2V across the entire allowed VccQ range specified in Table 7 for 1.8V I/O signaling and 1.2V I/O signaling.

Remove ILO row from Tables 12, 13, and 14.

Add Table 15 shown below:

Symbol	**Parameter**	**Max**
ILO_{pd}	Output leakage current: DQ are disabled: VOUT=VCCQ;	**7uA**[1]
ILO_{pu}	Output leakage current: DQ are disabled: VOUT=0V; ODT disabled	**7uA**[1]
NOTE: 1. Absolute leakage value per DQ pin per NAND die. The following signals are required to meet output leakage (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c)		

Table 15 Output Leakage

Modify Section 4.10.3 "Package Electrical Specifications and Pad Capacitance", Table 46 shown below:

Symbol	Parameter	<=400 MT/s		533 MT/s		667 MT/s		800 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
C_{IO}	Input/Output Capacitance	-	2.5	-	2.5	-	2.5	-	2.5	pF
C_{ZQ}	ZQ capacitance	-	2.875	-	2.875	-	2.875	-	2.875	pF
$D\ C_{IO\ DQS}$	Delta Input/Output Capacitance DQS_t and DQS_c	0	0.2	0	0.2	0	0.2	0	0.2	pF
$D\ C_{IO\ RE}$	Delta Input/Output Capacitance for RE_t and RE_c	0	0.2	0	0.2	0	0.2	0	0.2	pF

NOTE:

1. These parameters are not subject to a production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with Vcc, VccQ, Vss, and VssQ applied and all other pins floating (accept the pin under test). ~~VDD =~~ VccQ = 1.2V, VBIAS = VccQ/2 and on-die termination off.
2. These parameters apply to monolithic die, obtained by de-embedding the package L & C parasitic.
3. Delta for DQS is the absolute value of CIO(DQS_t) - CIO(DQS_c)
4. Delta for RE is the absolute value of CIO(RE_t) - CIO(RE_c)

Table 1 Pad Input/Output Capacitance

Disposition log

12/23/2014	Erratum captured.
1/26/2015	Updated TBD values for ILO
2/3/2015	Fixed Errors in regards to Tables referenced

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