ONFI Technical Errata

Errata ID	**016**
Affected Spec Ver.	**ONFI 3.0, 3.1, 3.2, 4.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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This Errata adds Capacitance and Electrical Package Characteristic changes for packages with unequally loaded channels (i.e. packages with different number of LUNs per x8 data bus).

Description of the specification change

Modify Section 4.10.1 shown below:

The requirements in this section apply to legacy devices that support the NV-DDR or NV-DDR2 data interfaces. For NV-DDR3 devices and NV-DDR2 devices that support speeds faster than 533 MT/s, the Package Electrical Specification and Pad Capacitance (section 4.10.3) shall be used for device capacitance requirements.

The input capacitance requirements are defined in Table 42. The testing conditions that shall be used to verify the input capacitance requirements are: temperature of 25 degrees Celsius, VccQ=1.2V, V_{BIAS} = VccQ/2, and a frequency of 100 MHz.

The capacitance delta values measure the pin-to-pin capacitance for all LUNs within a package, including across data buses if the package has the same number of LUNs per x8 data bus (i.e. package channel). The capacitance delta values are not measured across data buses if the package has a different number of LUNs per x8 data bus. The capacitance delta values change based on the number of LUNs per x8 data bus.

The variance from the Typical capacitance is the maximum capacitance or minimum capacitance any pin in a signal group may have relative to the Typical value for that signal group. The variance is symmetrically offset from the Typical reported value and bounds the absolute maximum and minimum capacitance values.

Modify Section 4.10.2 shown below:

For each signal group, a typical capacitance value is defined and reported for each NAND Target within a package. The signal groups include all signal group pins in a single package even if the pins belong to separate I/O channels unless the package has a different number of LUNs per x8 data bus. If the package has a different number of LUNs per x8 data bus than the signal group pins are separated per each x8 data bus.

There are two key parameters that define how much capacitance may vary within a package. The *delta* defines the maximum pin-to-pin capacitance difference within a signal group in a single package. Specifically, the delta within a signal group is the difference between the pin with the maximum capacitance and the pin with the minimum capacitance within the signal group. The *variance* is the maximum capacitance or minimum capacitance any pin in a signal group may have relative to the typical value for that signal group. The variance is symmetrically offset from the typical reported value and bounds the absolute maximum and minimum capacitance values. The delta may be asymmetrical from the typical value; i.e. the minimum capacitance may be closer or further away from the typical value than the maximum capacitance for that signal group. The “delta window” always falls within the “variance window”, and thus the delta is always smaller than the variance multiplied by two.

Modify Section 4.10.3 shown below:

ZIO and TdIO apply to DQ[7:0], DQS_t, DQS_c, RE_t and RE_c. TdIOMismatch applies to DQ[7:0], DQS_t and DQS_c. Mismatch and Delta values are required to be met across same data bus on given package (i.e. package channel), but not required across all channels on a given package. All other pins only need meet requirements described in section 4.10.1. The DQ[7:0], DQS_t, DQS_c, RE_t and RE_c pins only need to meet the requirements in this section 4.10.3.

Pad capacitances apply to DQ[7:0]. DQS_t, DQS_c, RE_t and RE_c. All other pins only need meet requirements described in section 4.10.1. The DQ[7:0], DQS_t, DQS_c, RE_t and RE_c pins only need to meet the requirements in this section 4.10.3.

Disposition log

4/5/2016	Erratum captured.

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