ONFI Technical Errata

Errata ID	**002**
Affected Spec Ver.	**ONFI 2.0, 2.1, 2.2, 3.0, 3.1, 3.2, 4.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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The erratum clarifies the maximum capacitance for the CE_n and WP_n input pins. The original intent was to have CE_n and WP_n capacitance not exceed the higher of either the CLK or input pin maximums. The current specification is not clear on this intent, so the erratum clarifies.

Description of the specification change

Modify Section 4.10.1 Table 42 shown below:

4.10.1 Legacy Capacitance Requirements

Parameter	Number of LUNs per x8 Data Bus				Unit
	1	2	4	8	
Variance from Typical	± 1.0	± 1.5	± 2.0	± 4.0	pF
Delta	1.4	1.7	2.0	4.0	pF

NOTE:

1. Typical capacitance values for pin groups CCK, CIN, and CIO are specified in the parameter page. The allowable range for Typical capacitance values is specified in Table 43 for CLK and input pins and Table 44 for I/O pins.
2. Input capacitance for CE_n and WP_n shall not exceed the higher of either the CLK or input pin maximums. ~~maximum capacitance value of either the CLK and input pins.~~ However, CE_n and WP_n are not required to meet delta or variance requirements. For example, if maximum capacitance (typical capacitance plus variance from typical) for CLK is 5.0pf and maximum capacitance for the input pins is 5.5pf, the maximum capacitance for CE_n and WP_n is 5.5pf.

Table 1 Input Capacitance Delta and Variance

Disposition log

6/18/2014	Erratum captured.

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