ONFI Technical Errata

Errata ID	**018**
Affected Spec Ver.	**ONFI 3.0, 3.1, 3.2, 4.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
Terry Grunzke	Micron	4/5/16

This errata uses the case that when data eye training is performed tDVW is really what is most important for output timing. Since users, especially at faster I/O speeds, “train” the data eye vs. DQS, the data valid window is centered at the controller (opposite side of the channel from the NAND). NAND Vendors are currently required to meet both the tQH and tDQSQ parameter values when in reality due to the data eye training only tDVW is required for sufficient data capture.

Description of the specification change

Modify 4.18.3 shown below:

The following requirements apply to the timing parameter values:

1. tCHZ and tCLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
2. The parameters tRC(avg) and tDSC(avg) are the average over any 200 consecutive periods and tRC(avg)/tDSC(avg) min are the smallest rates allowed, with the exception of a deviation due to tJITper.
3. Input jitter is allowed provided it does not exceed values specified.
4. tREH(avg) and RP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter, Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter (tJITper) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter (tJITcc) is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed tJITper. As long as the absolute minimum half period tRP(abs), tREH(abs), tDQSH or tDQSL is not less than 43 percent of the average cycle.
8. When the device is operated with input RE_n (RE_t/RE_c) jitter, tQSL, tQSH, and tQH need to be derated by the actual input duty cycle jitter beyond 0.45 * tRC(avg) but not exceeding 0.43 * tRC(avg). Output deratings are relative to the device input RE_n pulse that generated the DQS pulse.
9. Minimizing the amount of duty cycle jitter to more than 45% of the average cycle provides a larger tQH, which in turn provides a larger data valid window. The device shall provide a minimum of 0.5% of larger data valid window for each 1% improvement in duty cycle jitter. For example, if the host provides a tREH(abs) of 0.49 * tRC(avg) then the device shall provide at least a tQH of 0.39 * tRC(avg).
10. The tDS and tDH times listed are based on an input slew rate of 1 V/ns. If the input slew rate is not 1 V/ns, then the derating methodology shall be used.
11. The parameter tDIPW is defined as the pulse width of the input signal between the first crossing of VREFQ(DC) and the consecutive crossing of VREFQ(DC).
12. Parameters tDQSQ, and tQH are used to calculate overall tDVW (tDVW = tQH - tDQSQ). Since data eye training to optimize strobe placement is expected at high I/O speeds (>=533 MT/s), tDQSQ and tQH may borrow time from each other without changing tDVW. For example, if there exists X ps of margin on tDQSQ then tQH can be provided with an additional X ps without changing the value of tDVW. When timing margin is borrowed from tDQSQ to provide additional timing for tQH, the same amount of timing margin can be used for additional timing for tQSL/H.

Disposition log

4/5/2016	Erratum captured.

Technical input submitted to the ONFI Workgroup is subject to the terms of the ONFI contributor's agreement.