ONFI Technical Errata

Errata ID	**005**
Affected Spec Ver.	**ONFI 3.0, 3.1, 3.2, 4.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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The erratum adds the tCS3 (SDR, NV-DDR, and NV-DDR2/3) and tCDQSH (NV-DDR2/3) timing parameters.

During ONFI 4.0 development the parameter tCR2 was added to alleviate strain on NAND design, as some components may be powered down during standby when CE_n is high for long periods. The tCR2 parameter covers the case for data output when CE_n is high for a long period, but the case of for data input was not covered. The tCS3 parameter adds coverage for data input.

The parameter tCDQSH is added to provide industry interoperability when ending a data input burst in the NV-DDR2/3 interfaces.

Description of the specification change

Modify Section 4.17 "Timing Parameters", 4.17.2 "SDR" Table 80 shown below:

Parameter	Description
tALH	ALE hold time
tALS	ALE setup time
tAR	ALE to RE_n delay
tCEA	CE_n access time
tCHZ[1]	CE_n high to output hi-Z
tCLH	CLE hold time
tCLR	CLE to RE_n delay
tCLS	CLE setup time
tCOH	CE_n high to output hold
tCR	CE_n to RE_n low
tCR2	CE_n to RE_n low after CE_n has been high for greater than 1us
tCS3	CE_n setup time for data input after CE_n has been high for greater than 1us
tIR[1]	Output hi-Z to RE_n low
tRC	RE_n cycle time
tREA	RE_n access time
tREH	RE_n high hold time
tRHOH	RE_n high to output hold
tRHW	RE_n high to WE_n low
tRHZ[1]	RE_n high to output hi-Z
tRLOH	RE_n low to output hold
tRP	RE_n pulse width
tWC	WE_n cycle time
tWH	WE_n high hold time
tWP	WE_n pulse width
NOTE: 1. Refer to Appendix E for measurement technique.	

Table 1 SDR Timing Parameter Descriptions

Modify Section 4.17 "Timing Parameters", 4.17.3 "NV-DDR" Table 81 shown below:

Parameter	Description
tAC	Access window of DQ[7:0] from CLK
tCADf, tCADs	Command, Address, Data delay (command to command, address to address, command to address, address to command, command/address to start of data)
tCAH	Command/address DQ hold time
tCALH	W/R_n, CLE and ALE hold time
tCALS	W/R_n, CLE and ALE setup time
tCAS	Command/address DQ setup time
tCK(avg)[1]	Average clock cycle time, also known as tCK
tCK(abs)	Absolute clock period, measured from rising edge to the next consecutive rising edge
tCKH(abs)[2]	Clock cycle high
tCKL(abs)[2]	Clock cycle low
tCKWR	Data output end to W/R_n high
tCS3	CE_n setup time for data input and data output after CE_n has been high for greater than 1us
tDPZ	Data input pause setup time
tDQSCK	Access window of DQS from CLK
tDQSD[3]	W/R_n low to DQS/DQ driven by device
tDQSH	DQS input high pulse width
tDQSHZ[3]	W/R_n high to DQS/DQ tri-state by device
tDQSL	DQS input low pulse width
tDQSQ	DQS-DQ skew, DQS to last DQ valid, per access
tDQSS	Data input to first DQS latching transition
tDSC	DQS cycle time
tDSH	DQS falling edge to CLK rising – hold time
tDSS	DQS falling edge to CLK rising – setup time
tDVW	Output data valid window
tHP	Half-clock period
tJIT(per)	The deviation of a given tCK(abs) from tCK(avg)
tQH	DQ-DQS hold, DQS to first DQ to go non-valid, per access
tQHS	Data hold skew factor
tRHW	Data output cycle to command, address, or data input cycle
tWPRE	DQS write preamble
tWPST	DQS write postamble
tWRCK	W/R_n low to data output cycle

NOTE:
1. tCK(avg) is the average clock period over any consecutive 200 cycle window.
2. tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.
3. Refer to Appendix E for measurement technique.

Table 2 NV-DDR Timing Parameter Descriptions

Modify Section 4.17 "Timing Parameters", 4.17.4 "NV-DDR2/NV-DDR3" Table 82 shown below:

Parameter	Description
tAC	Access window of DQ[7:0] from RE_n (RE_t/RE_c crosspoint)
tAR	ALE to (RE_n low or RE_t/RE_c crosspoint)
tCAH	Command/address DQ hold time
tCALH	CLE and ALE hold time
tCALS	CLE and ALE setup time
tCALS2	CLE and ALE setup time when ODT is enabled
tCAS	Command/address DQ setup time
tCHZ[1]	CE_n high to output Hi-Z
tCLHZ[1]	CLE high to output Hi-Z
tCLR	CLE to (RE_n low or RE_t/RE_c crosspoint)
tCR	CE_n to (RE_n low or RE_t/RE_c crosspoint)
tCR2	CE_n to (RE_n low or RE_t/RE_c crosspoint) after CE_n has been high for greater than 1us
tCS1	CE_n setup time for data burst with ODT disabled
tCS2	CE_n setup time with DQS/DQ[7:0] ODT enabled
tCS3	CE_n setup time with for data burst after CE_n has been high for greater than 1us
tCSD	ALE, CLE, WE_n hold time from CE_n high
tCDQSS	DQS setup time for data input start
tCDQSH	DQS hold time for data input burst end
tDBS	DQS (DQS_t) high and RE_n (RE_t) high setup to ALE, CLE and CE_n low during data burst
tDH_relaxed	Data DQ hold time relaxed timing
tDH_tight	Data DQ hold time tight timing
tDIPW	DQ input pulse width
tDQSD	(RE_n low or RE_t/RE_c crosspoint) to DQS/DQ driven by device
tDQSH	DQS high level width
tDQSL	DQS low level width
…	…
…	…

Table 3 NV-DDR2/NV-DDR3 Timing Parameter Descriptions

Modify Section 4.18 "Timing Modes", 4.18.1 "SDR" Tables 83 and 84 shown below:

Parameter	Mode 0		Mode 1		Mode 2		Unit
	100		50		35		ns
	Min	Max	Min	Max	Min	Max	
tCS3	100	—	100	—	100	—	ns

Table 4 SDR Timing Modes 0, 1, and 2

Parameter	Mode 3		Mode 4		Mode 4		Unit
	30		25		20		ns
	Min	Max	Min	Max	Min	Max	
tCS3	100	—	100	—	100	—	ns

Table 5 SDR Timing Modes 3, 4, and 5

Modify Section 4.18 "Timing Modes", 4.18.2 "NV-DDR" Table 85 shown below:

Parameter	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit
	50		30		20		15		12		10		ns
	20		~33		50		~66		~83		100		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tCS3	75	—	75	—	75	—	75	—	75	—	75	—	ns

Table 6 NV-DDR Timing Modes

Modify Section 4.18 "Timing Modes", 4.18.3 "NV-DDR2/3" Tables 88 shown below:

Constant Timing Parameter Values			
	Min	Max	Unit
tCS3	100	—	ns
tCDQSH	100	—	ns

Table 7 NV-DDR2 / NV-DDR3 Timing Parameter Values: Data Input

Modify Section 4.19 "Diagrams", 4.19.3 "NV-DDR2 and NV-DDR3", 4.19.3.3 "Data Input Cycle Timings" Figure 71 shown below:

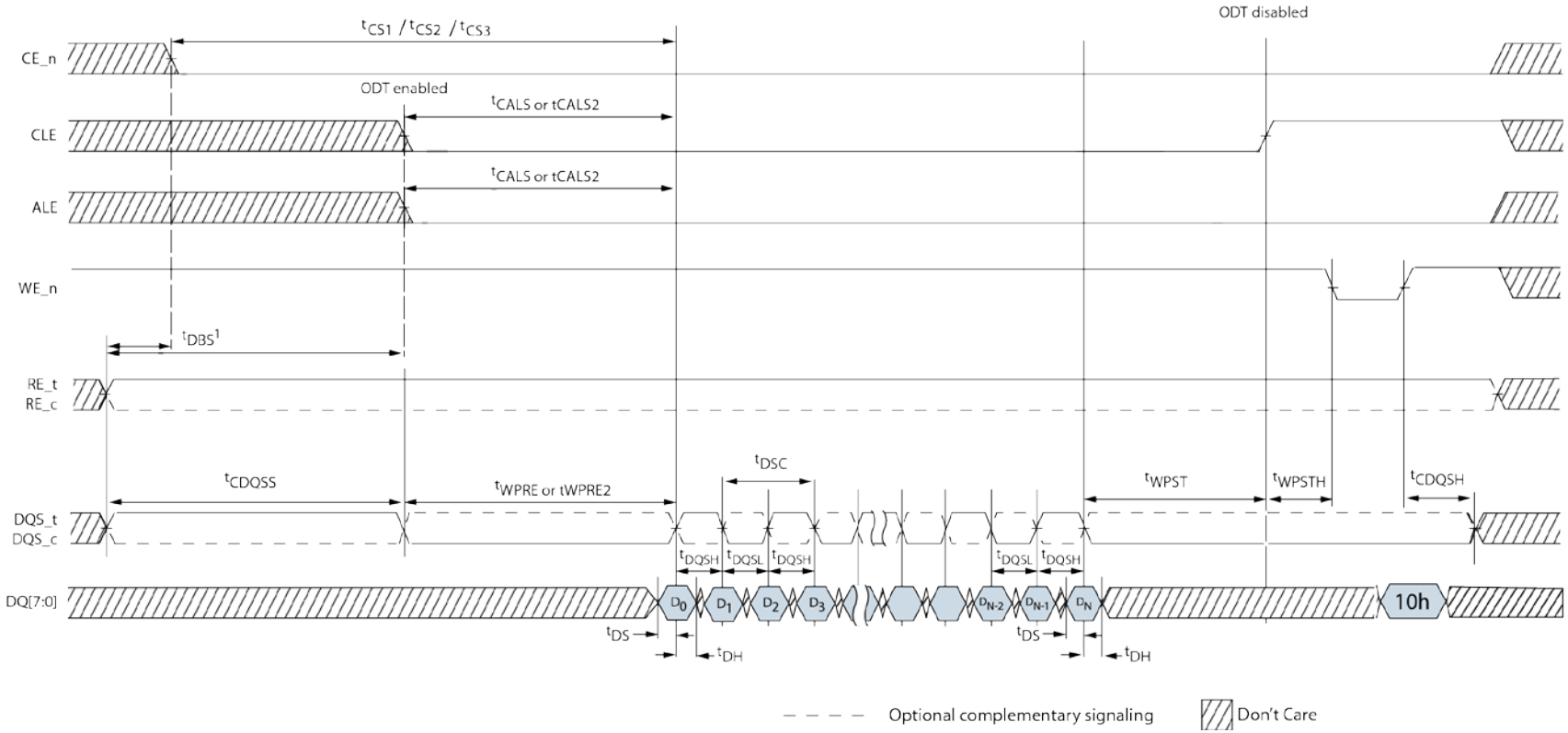

Figure 1 Data input cycle timing

Disposition log

8/22/2014	Erratum captured.

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