ONFI Technical Errata

Errata ID	**001**
Affected Spec Ver.	**ONFI 3.0, 3.1, 3.2, 4.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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The erratum clarifies R/B_n signal use per CE_n signal for all package configurations. This ensures hardware interoperability between vendors. The erratum also clarifies R/B_n and the shared LUNs' SR[6] relationship when there are multiple CE_n signals that share the same R/B_n.

Description of the specification change

Modify Section 2.16 shown below:

2.16 Independent Data Buses

There may be two independent 8-bit data buses in some ONFI packages (i.e. the LGA and the 100-ball BGA package). There may be four independent 8-bit data buses in some ONFI packages (i.e. the BGA-316 and BGA-272 packages). For packages that support either two independent data buses or a single data bus (e.g. LGA-52) then CE0_n and CE2_n shall use the same pins as the first data bus CE_n pins (marked as CE0_0_n and CE1_0_n) and CE1_n and CE3_n shall use the same pins as the second data bus CE_n pins (marked as CE0_1_n and CE1_1_n). Note that CE0_n, CE1_n, CE2_n, and CE3_n may all use the first data bus and the first set of control signals (RE0_n, CLE0_n, ALE0_n, WE0_n, and WP0_n) if the device does not support independent data buses.

Any signal with a channel (i.e. 8-bit data bus) designator (for example, "x" for CE0_x_n) could not be used by another channel. For example, CE0_0 cannot be used on any channel other than channel 0 or R/B0_1 cannot be used for any channel other than channel 1.

~~In the 152-ball BGA, there are eight CE_n signals and only four R/B_n signals. Table 18 describes the R/B_n signal that each CE_n uses in this case.~~

In some package configurations, there are multiple CE_n signals per R/B_n signal. Table 18 describes the R/B_n signal that each CE_n uses in the case when there are two R/B_n signals and more than one CE_n per 8-bit data bus. Table 19 describes the R/B_n signal that each CE_n uses in the case when there is a single R/B_n signal per 8-bit data bus. Table 3 provides the case when there is a single CE_n and two R/B_n signals per 8-bit data bus. For packages that only support two 8-bit data buses, R/B0_2_n, R/B1_2_n, R/B0_3_n and R/B1_3_n shall be ignored.

~~Signal Name~~	~~CE_n~~
~~R/B0_0_n~~	~~CE0_0_n, CE2_0_n~~
~~R/B0_1_n~~	~~CE0_1_n, CE2_1_n~~
~~R/B1_0_n~~	~~CE1_0_n, CE3_0_n~~
~~R/B1_1_n~~	~~CE1_1_n, CE3_1_n~~

~~**Table 1 R/B_n Signal Use Per CE_n**~~

Signal Name	CE_n
R/B0_0_n	CE0_0_n, CE2_0_n, CE4_0_n, CE6_0_n
R/B0_1_n	CE0_1_n, CE2_1_n, CE4_1_n, CE6_1_n
R/B0_2_n	CE0_2_n, CE2_2_n, CE4_2_n, CE6_2_n
R/B0_3_n	CE0_3_n, CE2_3_n, CE4_3_n, CE6_3_n
R/B1_0_n	CE1_0_n, CE3_0_n, CE5_0_n, CE7_0_n
R/B1_1_n	CE1_1_n, CE3_1_n, CE5_1_n, CE7_1_n
R/B1_2_n	CE1_2_n, CE3_2_n, CE5_2_n, CE7_2_n
R/B1_3_n	CE1_3_n, CE3_3_n, CE5_3_n, CE7_3_n

Table 18 R/B_n Signal Use Per CE_n with two R/B_n signals per channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n, CE1_0_n, CE2_0_n, CE3_0_n, CE4_0_n, CE5_0_n, CE6_0_n, CE7_0_n
R/B0_1_n	CE0_1_n, CE1_1_n, CE2_1_n, CE3_1_n, CE4_1_n, CE5_1_n, CE6_1_n, CE7_1_n
R/B0_2_n	CE0_2_n, CE1_2_n, CE3_2_n, CE3_2_n, CE4_2_n, CE5_2_n, CE6_2_n, CE7_2_n
R/B0_3_n	CE0_3_n, CE1_3_n, CE3_3_n, CE3_3_n, CE4_3_n, CE5_3_n, CE6_3_n, CE7_3_n

Table 19 R/B_n Signal Use Per CE_n with a single R/B_n signal per channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n
R/B0_1_n	CE0_1_n
R/B0_2_n	CE0_2_n
R/B0_3_n	CE0_3_n
R/B1_0_n	CE0_0_n
R/B1_1_n	CE0_1_n
R/B1_2_n	CE0_2_n
R/B1_3_n	CE0_3_n

Table 20 R/B_n Signal Use Per CE_n with a two R/B_n signals per channel and one CE_n per channel

Modify Section 2.18.2 shown below:

2.18.2 R/B_n and SR[6] Relationship

~~R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs on the corresponding NAND Target or Volume. For example, R/B3_n is the logical AND of the SR[6] values for all LUNs on CE3_n. Thus, R/B_n reflects whether any LUN is busy on a particular NAND Target.~~

R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs on the corresponding NAND Target or Volume. In the case that more than one NAND target or Volume share an R/B_n signal, R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs connected to the shared R/B_n signal. For example, R/B0_0 is logical AND of the SR[6] values for all LUNs that share R/B0_0. Thus, R/B_n reflects whether any LUN is busy on a particular NAND Target or if there are multiple NAND Targets that share R/B_n, R/B_n reflects whether any LUN is busy on any of the shared NAND Targets.

Disposition log

5/2/2014	Erratum captured.
5/13/2014	Minor changes to third paragraph to clarify that Table 18 describes the R/B_n signal that each CE_n uses in the case when there are two R/B_n signals and more than one CE_n per 8-bit data bus

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