ONFI Technical Errata

Errata ID	**011**
Affected Spec Ver.	**ONFI 3.0, 3.1, 3.2, 4.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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The erratum adds the tCD timing parameter for NV-DDR2/3. ONFI 4.0 ECN 005 added tCS3 parameter for SDR, NV-DDR and NV-DDR2/3. The tCD parameter replaces tCS3 for NV-DDR2/3. The tCD parameter is CE_n low to DQS (DQS_t) low when CE_n has been high for greater than 1us.

Description of the specification change

Modify Section 4.17 "Timing Parameters", 4.17.4 "NV-DDR2/NV-DDR3" Table 82 shown below:

Parameter	Description
tAC	Access window of DQ[7:0] from RE_n (RE_t/RE_c crosspoint)
tAR	ALE to (RE_n low or RE_t/RE_c crosspoint)
tCAH	Command/address DQ hold time
tCALH	CLE and ALE hold time
tCALS	CLE and ALE setup time
tCALS2	CLE and ALE setup time when ODT is enabled
tCAS	Command/address DQ setup time
tCHZ[1]	CE_n high to output Hi-Z
tCLHZ[1]	CLE high to output Hi-Z
tCLR	CLE to (RE_n low or RE_t/RE_c crosspoint)
tCR	CE_n to (RE_n low or RE_t/RE_c crosspoint)
tCR2	CE_n to (RE_n low or RE_t/RE_c crosspoint) after CE_n has been high for greater than 1us
tCS1	CE_n setup time for data burst with ODT disabled
tCS2	CE_n setup time with DQS/DQ[7:0] ODT enabled
~~tCS3~~	~~CE_n setup time with for data burst after CE_n has been high for greater than 1us~~
tCD	CE_n setup time to DQS (DQS_t) low after CE_n has been high for greater than 1us
tCSD	ALE, CLE, WE_n hold time from CE_n high
tCDQSS	DQS setup time for data input start
tCDQSH	DQS hold time for data input burst end
tDBS	DQS (DQS_t) high and RE_n (RE_t) high setup to ALE, CLE and CE_n low during data burst
tDH_relaxed	Data DQ hold time relaxed timing
tDH_tight	Data DQ hold time tight timing
tDIPW	DQ input pulse width
tDQSD	(RE_n low or RE_t/RE_c crosspoint) to DQS/DQ driven by device
tDQSH	DQS high level width
tDQSL	DQS low level width
…	…
…	…

Table 1 NV-DDR2/NV-DDR3 Timing Parameter Descriptions

Modify Section 4.18 "Timing Modes", 4.18.3 "NV-DDR2/3" Tables 88 shown below:

Constant Timing Parameter Values			
	Min	Max	Unit
~~tCS3~~	~~100~~	~~—~~	~~ns~~
tCD	100	—	ns

Table 2 NV-DDR2 / NV-DDR3 Timing Parameter Values: Data Input

Modify Section 4.19 "Diagrams", 4.19.3 "NV-DDR2 and NV-DDR3", 4.19.3.3 "Data Input Cycle Timings" Figure 71 shown below:

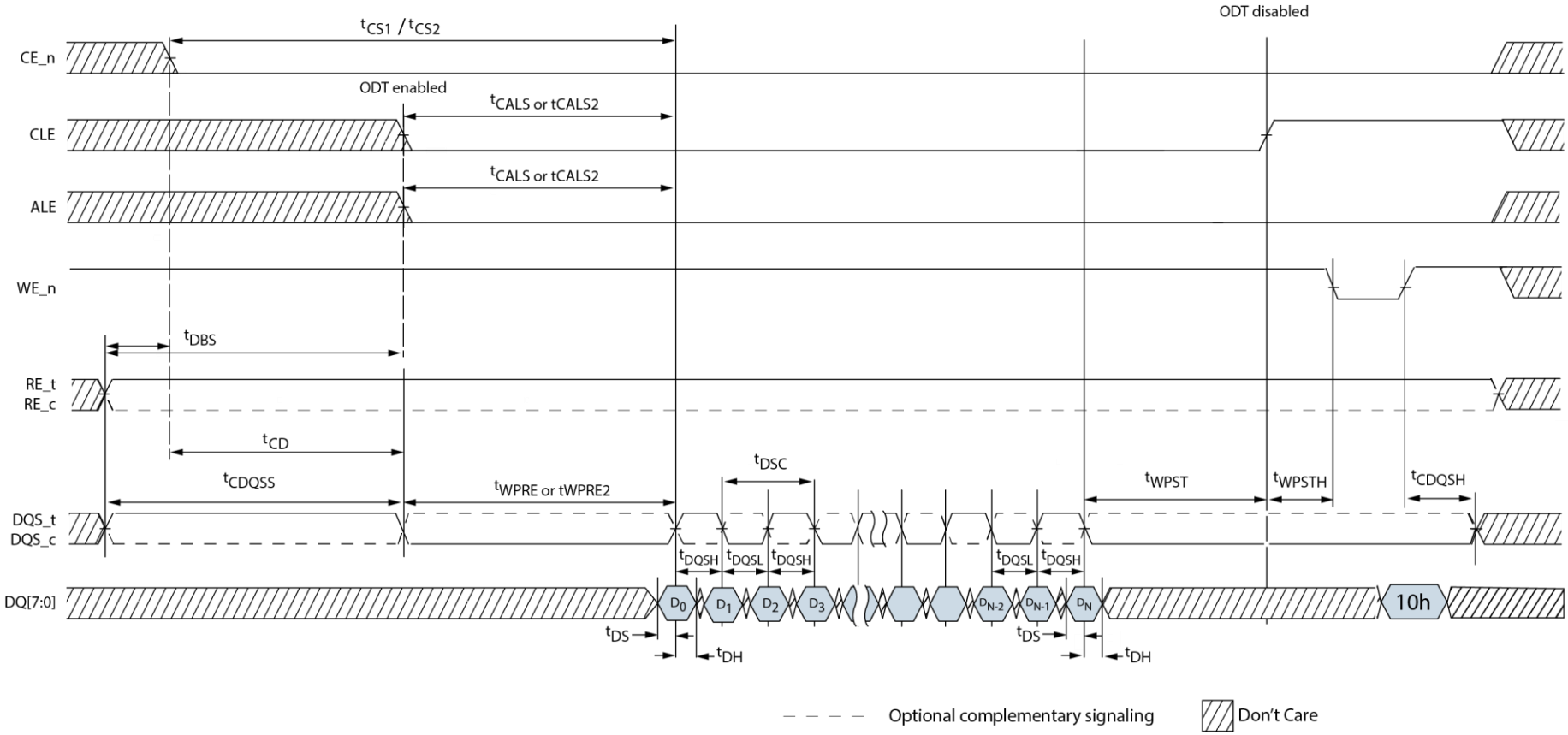

Figure 1 Data input cycle timing

Disposition log

2/24/2015	Erratum captured.

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