ONFI Technical Errata

Errata ID	**004**
Affected Spec Ver.	**ONFI 3.2**
Corrected Spec Ver.	

Submission info

Name	Company	Date
Terry Grunzke	Micron	09/23/13

The errata moves Parameter Page Byte 141, bit 6 from NV-DDR2 Timing Mode 8 supported to "Reserved" and moves NV-DDR2 Timing Mode 8 supported to Parameter Page Byte 162, bit 0. This provides flexibility for future expansion of NV-DDR2 Timing Modes in the Parameter Page.

Description of the specification change

Modify Section 5.7.1, Table 71 as shown below:

	Electrical parameters block	
141	O	NV-DDR~~/NV-DDR2~~ timing mode support 7 Reserved (0) 6 Obsolete ~~6 1 = supports NV-DDR2 timing mode 8~~ 5 1 = supports NV-DDR timing mode 5 4 1 = supports NV-DDR timing mode 4 3 1 = supports NV-DDR timing mode 3 2 1 = supports NV-DDR timing mode 2 1 1 = supports NV-DDR timing mode 1 0 1 = supports NV-DDR timing mode 0
162	O	NV-DDR2 timing mode support 1-7 Reserved (0) 0 1 = supports timing mode 8

Modify Section 5.7.1.9 as shown below:

Byte 141: NV-DDR~~/NV-DDR2~~ timing mode support

This field indicates the NV-DDR ~~and NV-DDR2~~ timing modes supported. If the NV-DDR data interface is supported by the target, at least one NV-DDR timing mode shall be supported. The target shall support an inclusive range of NV-DDR timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-DDR timing mode 0.

Bit 1 when set to one indicates that the target supports NV-DDR timing mode 1.

Bit 2 when set to one indicates that the target supports NV-DDR timing mode 2.

Bit 3 when set to one indicates that the target supports NV-DDR timing mode 3.

Bit 4 when set to one indicates that the target supports NV-DDR timing mode 4.

Bit 5 when set to one indicates that the target supports NV-DDR timing mode 5.

~~Bit 6 when set to one indicates that the target supports NV-DDR2 timing mode 8.~~

Bits 6-7 ~~is~~ are reserved and shall be cleared to zero

Byte 162: NV-DDR2 timing mode support

This field is a continuation of Byte 142. This field indicates the NV-DDR2 timing modes supported. If the NV-DDR2 data interface is supported by the target, at least one NV-DDR2 timing mode shall be supported. The target shall support an inclusive range of NV-DDR2 timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-DDR2 timing mode 8.

Bits 1-7 are reserved and shall be cleared to zero.

Disposition log

9/23/2013	Erratum captured.
10/15/2013	Minor edit
10/23/2013	Changed bit 6 of Byte 141 to be “obsolete” instead of reserved.

Technical input submitted to the ONFI Workgroup is subject to the terms of the ONFI contributor’s agreement.