ONFI Technical Errata

Errata ID	**006**
Affected Spec Ver.	**ONFI 2.0, 2.1, 2.2, 2.3, 3.0, 3.1, 3.2**
Corrected Spec Ver.	

Submission info

Name	Company	Date
Terry Grunzke	Micron	09/23/13

The erratum clarifies an inconsistency in the draft for Feature Address Timing Mode (01h) when a RESET (FFh) is issued to the NAND device. The Timing Number bits located in sub-feature parameter P1<3:0> are cleared to Timing Mode Number 0 when a RESET (FFh) is issued. This is consistent with the requirement that the host shall use SDR timing mode 0 after a RESET (FFh) is issued.

Description of the specification change

Modify Section 5.28.1 as shown below:

5.28.1. Timing Mode

This setting shall be supported if the target complies with ONFI specification revision 1.0.

The Data Interface setting and Timing Mode Number ~~is~~ are not retained across Reset (FFh); after a Reset (FFh) the Data Interface shall be SDR and Timing Mode Number 0. All other settings for the timing mode are retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands. If the Reset (FFh) command is issued when the Data Interface is configured as NV-DDR or NV DDR2, then the host shall use the SDR data interface with Timing Mode 0 until a new data interface and/or timing mode is selected with Set Features. Hosts shall only set a timing mode that is explicitly shown as supported in the Read Parameter Page.

Disposition log

11/15/2013	Erratum captured.

Technical input submitted to the ONFI Workgroup is subject to the terms of the ONFI contributor's agreement.