ONFI Technical Errata

Errata ID	**008**
Affected Spec Ver.	**ONFI 1.0 2.0, 2.1, 2.2, 2.3, 3.0, 3.1**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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This erratum defines tCR for SDR mode.
The erratum also fixes timing diagram for SDR & NV-DDR2.

Parameter	Description
tALH	ALE hold time
tALS	ALE setup time
tAR	ALE to RE_n delay
tCEA	CE_n access time
tCHZ[1]	CE_n high to output hi-Z
tCLH	CLE hold time
tCLR	CLE to RE_n delay
tCLS	CLE setup time
tCOH	CE_n high to output hold
tCR	CE_n to RE_n low
tIR[1]	Output hi-Z to RE_n low
tRC	RE_n cycle time
tREA	RE_n access time
tREH	RE_n high hold time
tRHOH	RE_n high to output hold
tRHW	RE_n high to WE_n low
tRHZ[1]	RE_n high to output hi-Z
tRLOH	RE_n low to output hold
tRP	RE_n pulse width
tWC	WE_n cycle time
tWH	WE_n high hold time
tWP	WE_n pulse width
NOTE: Refer to Appendix **Error! Reference source not found.** for measurement technique.	

Table 1 SDR Timing Parameter Descriptions

Parameter	Mode 0		Mode 1		Mode 2		Unit
	100		50		35		ns
	Min	Max	Min	Max	Min	Max	
tADL	200	—	100	—	100	—	ns
tALH	20	—	10	—	10	—	ns
tALS	50	—	25	—	15	—	ns
tAR	25	—	10	—	10	—	ns
tCEA	—	100	—	45	—	30	ns
tCEH	20	—	20	—	20	—	ns
tCH	20	—	10	—	10	—	ns
tCHZ	—	100	—	50	—	50	ns
tCLH	20	—	10	—	10	—	ns
tCLR	20	—	10	—	10	—	ns
tCLS	50	—	25	—	15	—	ns
tCOH	0	—	15	—	15	—	ns
tCR	10	—	10	—	10	—	ns
tCS	70	—	35	—	25	—	ns
tDH	20	—	10	—	5	—	ns
tDS	40	—	20	—	15	—	ns
tFEAT	—	1	—	1	—	1	µs
tIR	10	—	0	—	0	—	ns
tITC	—	1	—	1	—	1	µs
tRC	100	—	50	—	35	—	ns
tREA	—	40	—	30	—	25	ns
tREH	30	—	15	—	15	—	ns
tRHOH	0	—	15	—	15	—	ns
tRHW	200	—	100	—	100	—	ns
tRHZ	—	200	—	100	—	100	ns
tRLOH	0	—	0	—	0	—	ns
tRP	50	—	25	—	17	—	ns
tRR	40	—	20	—	20	—	ns
tRST (raw NAND)	—	5000	—	10/30/ 500	—	10/30/ 500	µs
tRST[2] (EZ NAND)	—	250000	—	150/ 150/ 500	—	150/ 150/ 500	µs
tWB	—	200	—	100	—	100	ns
tWC	100	—	45	—	35	—	ns
tWH	30	—	15	—	15	—	ns
tWHR	120	—	80	—	80	—	ns
tWP	50	—	25	—	17	—	ns
tWW	100	—	100	—	100	—	ns

NOTE:
1. To easily support EDO capable devices, tCHZ and tRHZ maximums are higher in modes 1, 2, and 3 than typically necessary for a non-EDO capable device.
2. If the reset is invoked using a Reset (FFh) command then the EZ NAND device has 250 ms to complete the reset operation regardless of the timing mode. If the reset is invoked using Reset LUN (FAh) command then the values are as shown.

Table 2 SDR Timing Modes 0, 1, and 2

Parameter	Mode 3		Mode 4 (EDO capable)		Mode 5 (EDO capable)		Unit
	30		25		20		ns
	Min	Max	Min	Max	Min	Max	
tADL	100	—	70	—	70	—	ns
tALH	5	—	5	—	5	—	ns
tALS	10	—	10	—	10	—	ns
tAR	10	—	10	—	10	—	ns
tCEA	—	25	—	25	—	25	ns
tCEH	20	—	20	—	20	—	ns
tCH	5	—	5	—	5	—	ns
tCHZ	—	50	—	30	—	30	ns
tCLH	5	—	5	—	5	—	ns
tCLR	10	—	10	—	10	—	ns
tCLS	10	—	10	—	10	—	ns
tCOH	15	—	15	—	15	—	ns
tCR	10	—	10	—	10	—	ns
tCS	25	—	20	—	15	—	ns
tDH	5	—	5	—	5	—	ns
tDS	10	—	10	—	7	—	ns
tFEAT	—	1	—	1	—	1	µs
tIR	0	—	0	—	0	—	ns
tITC	—	1	—	1	—	1	µs
tRC	30	—	25	—	20	—	ns
tREA	—	20	—	20	—	16	ns
tREH	10	—	10	—	7	—	ns
tRHOH	15	—	15	—	15	—	ns
tRHW	100	—	100	—	100	—	ns
tRHZ	—	100	—	100	—	100	ns
tRLOH	0	—	5	—	5	—	ns
tRP	15	—	12	—	10	—	ns
tRR	20	—	20	—	20	—	ns
tRST (raw NAND)	—	10/30/ 500	—	10/30/ 500	—	10/30/ 500	µs
tRST[2] (EZ NAND)	—	150/150/ 500	—	150/ 150/ 500	—	150/ 150/ 500	µs
tWB	—	100	—	100	—	100	ns
tWC	30	—	25	—	20	—	ns
tWH	10	—	10	—	7	—	ns
tWHR	80	—	80	—	80	—	ns
tWP	15	—	12	—	10	—	ns
tWW	100	—	100	—	100	—	ns

NOTE:
1. To easily support EDO capable devices, tCHZ and tRHZ maximums are higher in modes 1, 2, and 3 than typically necessary for a non-EDO capable device.
2. If the reset is invoked using a Reset (FFh) command then the EZ NAND device has 250 ms to complete the reset operation regardless of the timing mode. If the reset is invoked using Reset LUN (FAh) command then the values are as shown.

Table 3 SDR Timing Modes 3, 4, and 5

Description of the specification changes

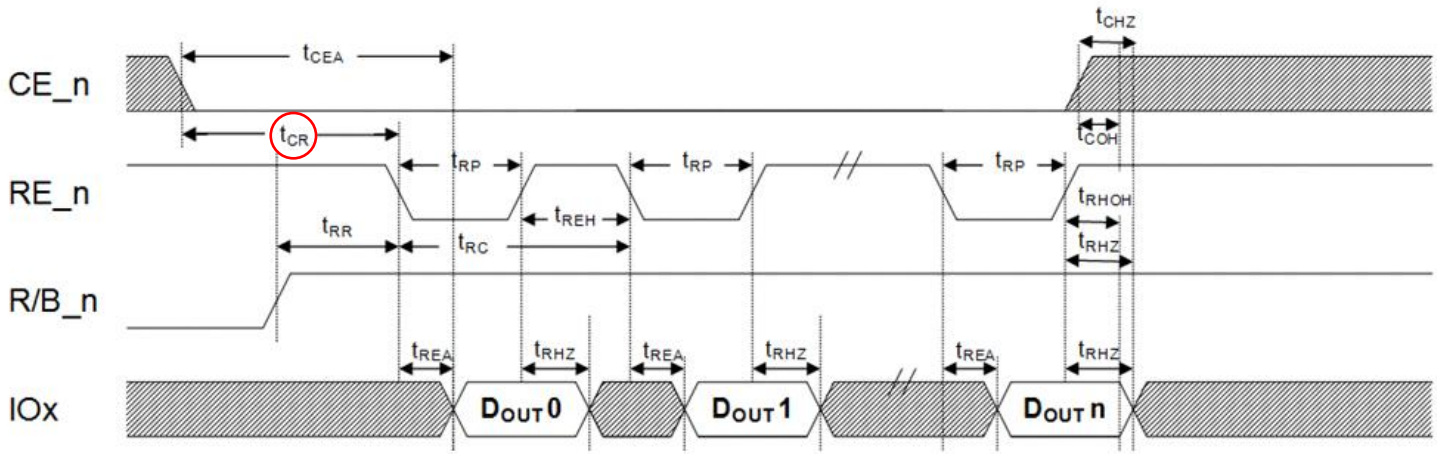

Figure 50 Data output cycle timings

Description of the specification changes

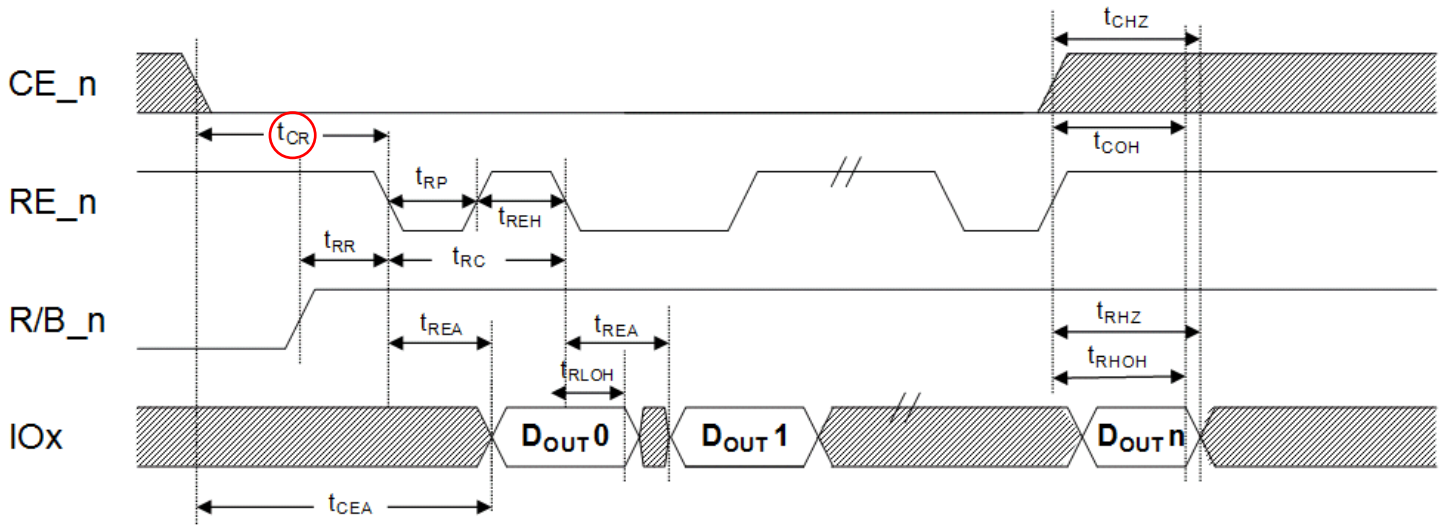

Figure 1 EDO data output cycle timings

Description of the specification changes

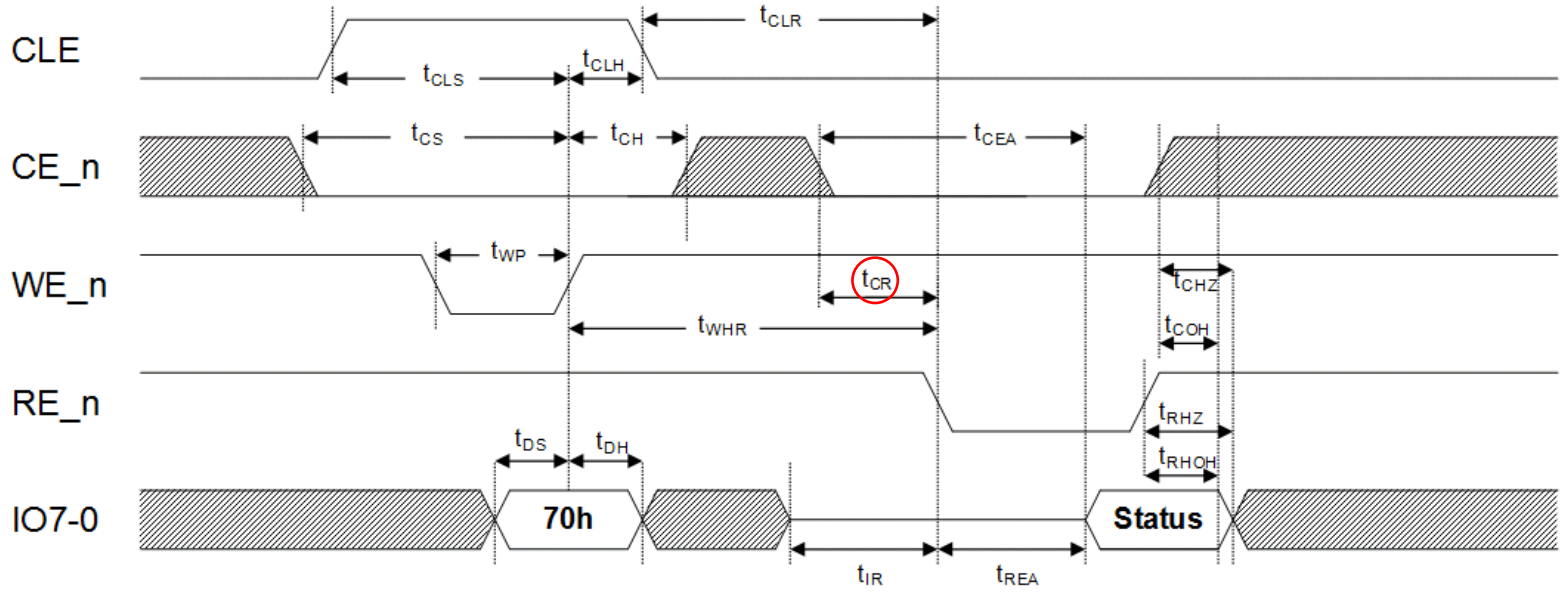

Figure 2 Read Status timings

Description of the specification changes

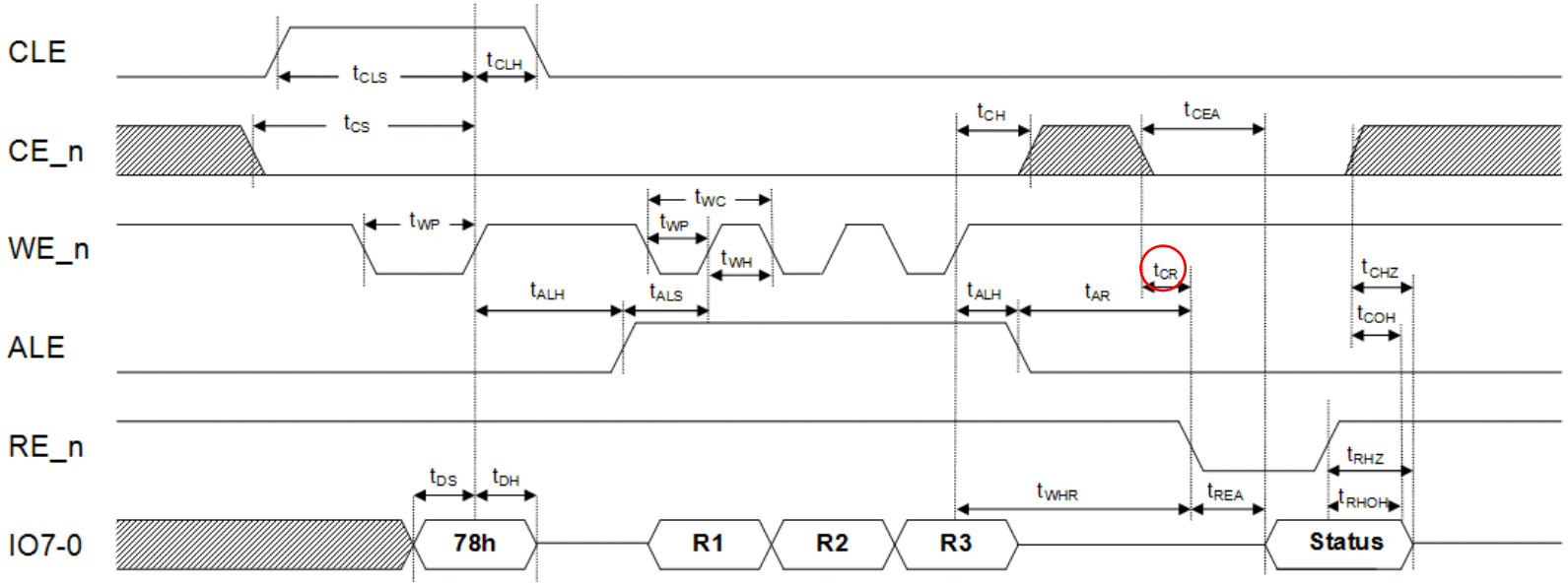

Figure 3 Read Status Enhanced timings

Description of the specification changes

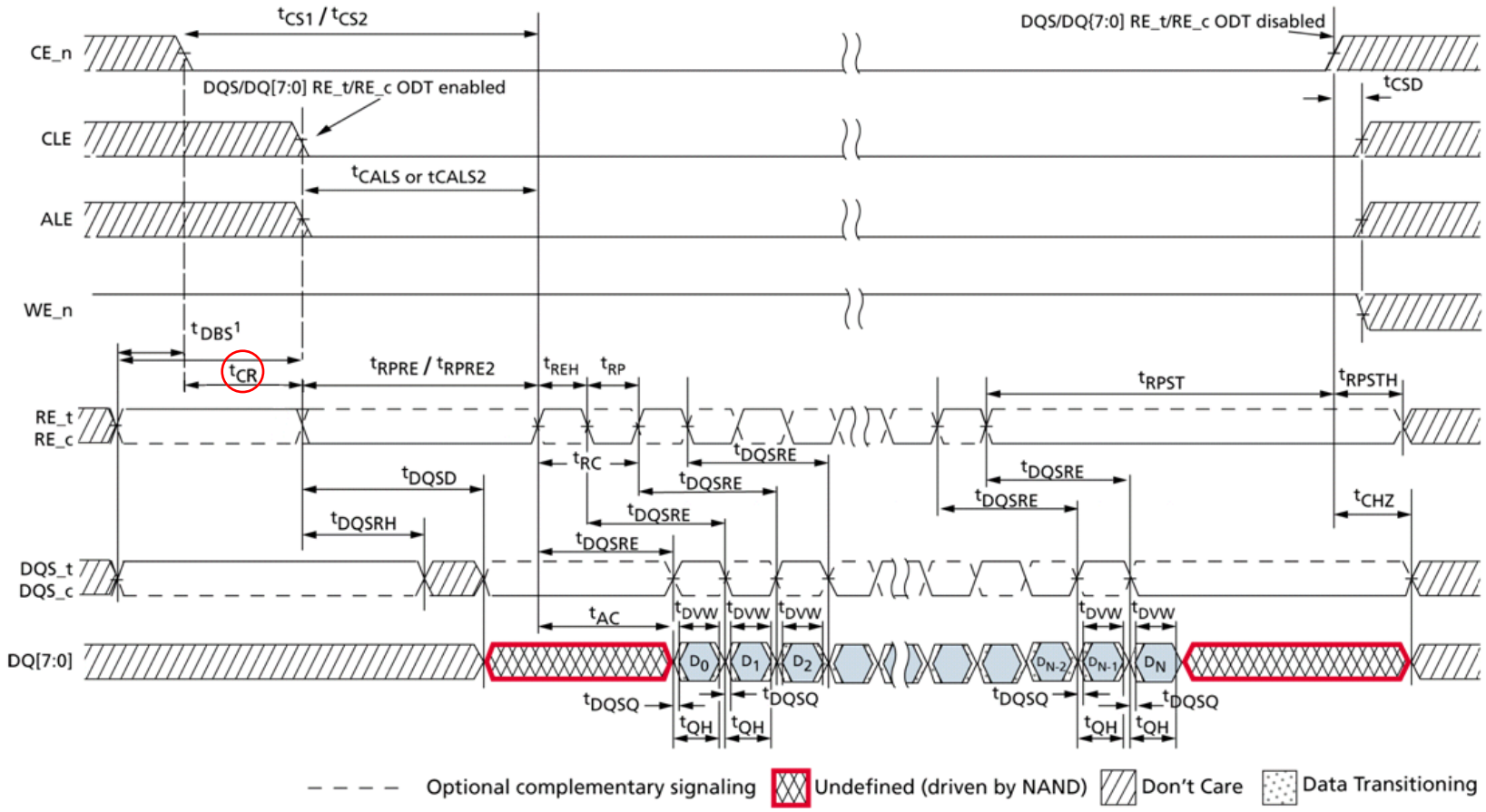

Figure 4 Data output cycle timing

Disposition log

2/2/2013	Erratum captured.
2/6/2013	Fixed description of tCR for SDR to not include differential signals RE_c and RE_t

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