ONFI Technical Errata

Errata ID	**003**
Affected Spec Ver.	**ONFI 3.0, 3.1**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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The ONFI specification describes idle state requirements for DQS during NV-DDR2 command and address cycles. The requirements for this, and the transition into a data cycle may be unclear to implementers. This erratum attempts to more clearly state the requirement for keeping DQS high during this time.

Description of the specification change

In the ONFI 3.1 specification, sections 4.17.3.1, 4.17.3.2, 5.2, 5.6, 5.10 (5 occurences), replace this text:

If ALE, CLE and CE_n are all low (i.e. Idle state) then DQS (DQS_t) shall be driven high by the host.

with this text:

When the bus state is not a data input or data output cycle, if ALE, CLE and CE_n are all low (i.e. Idle state) then DQS (DQS_t) shall be held high by the host to prevent the device from enabling ODT. If ODT is disabled, then DQS is a don't care during Idle states.

Disposition log

10/1/2012	Erratum captured.

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