ONFI Technical Errata

Errata ID	**004**
Affected Spec Ver.	**ONFI 1.0 2.0, 2.1, 2.2, 2.3, 3.0, 3.1**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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This erratum clarifies ICC4R and ICCQ4R test conditions to provide more accurate current measurements. The erratum adds ICC4QR that is not related to the load switching current (Iout = 0mA). For Icc4R, the data pattern is no longer static as this current is isolated from the load switching current. The erratum also adds ICCQ4W to the tables.
The erratum also changes the standby current (ISB) as NAND array and interface technology has advanced standby current has also increased.

Description of the specification change

In the ONFI 3.1 specification, Section 2.11, Table 8:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Array read current	ICC1	Refer to Appendix **Error! Reference source not found.**	-	-	50	mA
Array program current	ICC2		-	-	50	mA
Array erase current	ICC3		-	-	50	mA
I/O burst read current	$ICC4_R$ [~~4,~~5]		-	-	50 / 100 (Note 5)	mA
	$ICCQ4R$ [4,5]		-	-	50 / 100 (Note 5)	mA
I/O burst write current	$ICC4_W$ [5]		-	-	50 / 100 (Note 5)	mA
	$ICCQ4_W$ [5]		-	-	50 / 100 (Note 5)	mA
Bus idle current	ICC5		-	-	10	mA
Standby current~~, CMOS~~	ISB	CE_n=VccQ-0.2V, WP_n=0V/VccQ	-	-	~~50~~ 100	µA
Staggered power-up current	IST [1]	CE_n=VccQ-0.2V tRise = 1 ms cLine = 0.1 µF	-	-	10	mA
Vpp Idle current	IPP_I [6]	-	-	-	10	uA
Vpp Active current	IPP_A [6]	-	-	-	5	mA

NOTE:

1. Refer to Appendix **Error! Reference source not found.** for an exception to the IST current requirement.
2. ICC1, ICC2, and ICC3 as listed in this table are active current values. For details on how to calculate the active current from the measured values, refer to Appendix **Error! Reference source not found.**.
3. During cache operations, increased ICC current is allowed while data is being transferred on the bus and an array operation is ongoing. For a cached read this value is ICC1 + $ICC4_R$; for a cached write this value is ICC2(active) + $ICC4_W$.
4. For $ICCQ4_R$ the test conditions in Appendix **Error! Reference source not found.** specify IOUT = 0 mA ~~and requires static outputs with no output switching.~~ When ~~outputs are not static~~ Iout is not equal to 0mA, additional VccQ switching current will be drawn that is highly dependent on system configuration. IccQ due to loading without IOUT = 0mA may be calculated for each output pin assuming 50% data switching as (IccQ = 0.5 * C_L * VccQ * frequency), where C_L is the capacitive load.
5. When the data frequency is above 200 MT/s, then the LUN may consume 100 mA. When the data frequency is below or equal to 200 MT/s, then the LUN may consume 50 mA.
6. IPP Idle current is IPP current measured when Vpp is supplied and Vpp is not enabled via Set Feature. IPP Active current is IPP current measured when Vpp is supplied and Vpp is enabled via Set Feature.

Table 1 DC and Operating Conditions for raw NAND, measured on Vcc or VccQ rail

In the ONFI 3.1 specification, Section 2.11, Table 9:

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Array read current	ICC1	Refer to Appendix **Error! Reference source not found.**	Per LUN	-	-	85	mA
	ICCQ1		Controller	-	-	200	
	ICCQ1		Per LUN	-	-	15	
Array program current	ICC2		Per LUN	-	-	85	mA
	ICCQ2		Controller	-	-	75	
	ICCQ2		Per LUN	-	-	15	
Array erase current	ICC3		Per LUN	-	-	85	mA
	ICCQ3		Controller	-	-	75	
	ICCQ3		Per LUN	-	-	15	
I/O burst read current	$ICC4_R$[~~4,~~5]		LUN	-	-	50 / 100 (Note 5)	mA
	$ICCQ4_R$[4]		Controller/ Per LUN	-	-	~~100~~ 150/200 (Note 5)	
I/O burst write current	$ICC4_W$[5]		LUN	-	-	50 / 100 (Note 5)	mA
	$ICCQ4_W$		Controller/ Per LUN	-	-	~~100~~ 150/200 (Note 5)	
Bus idle current	ICC5		Per LUN	-	-	45	mA
	ICCQ5		Controller	-	-	50	
	ICCQ5		Per LUN	-	-	15	
Standby current~~, CMOS~~	ISB	CE_n=VccQ-0.2V, WP_n=0V/VccQ	Per LUN	-	-	~~50~~ 100	µA
	ISBQ		Controller	-	-	1000	
Staggered power-up current	IST[1,6]	CE_n=VccQ-0.2V tRise = 1 ms cLine = 0.1 µF	Per LUN	-	-	10	mA
	ISTQ[6]		Controller	-	-	20	

NOTE:

1. Refer to Appendix **Error! Reference source not found.** for an exception to the IST current requirement.
2. ICC1, ICC2, and ICC3 as listed in this table are active current values. For details on how to calculate the active current from the measured values, refer to Appendix **Error! Reference source not found.**.
3. During cache operations, increased ICC current is allowed while data is being transferred on the bus and an array operation is ongoing. For a cached read this value is ICC1 + $ICC4_R$ on Vcc and ICCQ1 on VccQ; for a cached write this value is ICC2(active) + $ICC4_W$ on Vcc, and ICCQ2 on VccQ.
4. For $ICCQ4_R$ the test conditions in Appendix **Error! Reference source not found.** specify IOUT = 0 mA ~~and requires static outputs with no output switching.~~ When ~~outputs are not static~~ Iout is not equal to 0mA, additional VccQ switching current will be drawn that is highly dependent on system configuration. IccQ due to loading without IOUT = 0mA may be calculated for each output pin assuming 50% data switching as (IccQ = 0.5 * C_L * VccQ * frequency), where C_L is the capacitive load.
5. When the data frequency is above 200 MT/s, then the LUN may consume 100 mA. When the data frequency is below or equal to 200 MT/s, then the LUN may consume 50 mA.
6. When bypass capacitors are included inside the package, the IST and ISTQ values do not include the current required to charge the capacitors.

Table 3 DC and Operating Conditions for EZ NAND, measured on Vcc or VccQ rail

In the ONFI 3.1 specification, Appendix D, Table 83 and Figure 126:

Parameter	SDR	NV-DDR	NV-DDR2
AC Timing Parameters	tWC = tWC(min) tRC = tRC(min) tADL = ~tADL(min) tCCS = ~tCCS(min) tRHW = ~tRHW(min)	tCK = tCK(avg) tADL =~tADL(min) tCCS = ~tCCS(min) tRHW = ~tRHW(min)	tWC = tWC(min) tRC = tRC(avg) tDSC = tDSC(avg) tADL = ~tADL(min) tCCS = ~tCCS(min)
Bus idle data pattern	IO[7:0] = FFh IO[15:0] = FFFFh	DQ[7:0] = FFh	DQ[7:0] = FFh
Repeated data pattern (Used for ICC2, ICC4R, ICCQ4R, ICCQ4W and ICC4W)	IO[7:0] = A5h, AAh, 5Ah, 55h IO[15:0] = A5A5h, AAAAh, 5A5Ah, 5555h	DQ[7:0] = A5h, AAh, 5Ah, 55h	DQ[7:0] = A5h, AAh, 5Ah, 55h
~~Array preconditioning for ICC4R~~	~~The array is preconditioned to match the following repeating data pattern:~~ ~~IO[7:0] = A5h~~ ~~IO[15:8] = A5A5h~~	~~The array is preconditioned to match the following repeating data pattern:~~ ~~DQ[7:0] = A5h~~	~~The array is preconditioned to match the following repeating data pattern:~~ ~~DQ[7:0] = A5h~~

NOTES:
1. The value of tCK(avg), tRC(avg), and tDSC(avg) used should be the minimum value of the timing modes supported for the device. The NV-DDR and NV-DDR2 timing modes supported by the device are indicated in the parameter page.
2. ICCQ4R testing is performed with 35 ohm drive strength setting.

Table 3 Data Interface Specific Testing Conditions for ICC

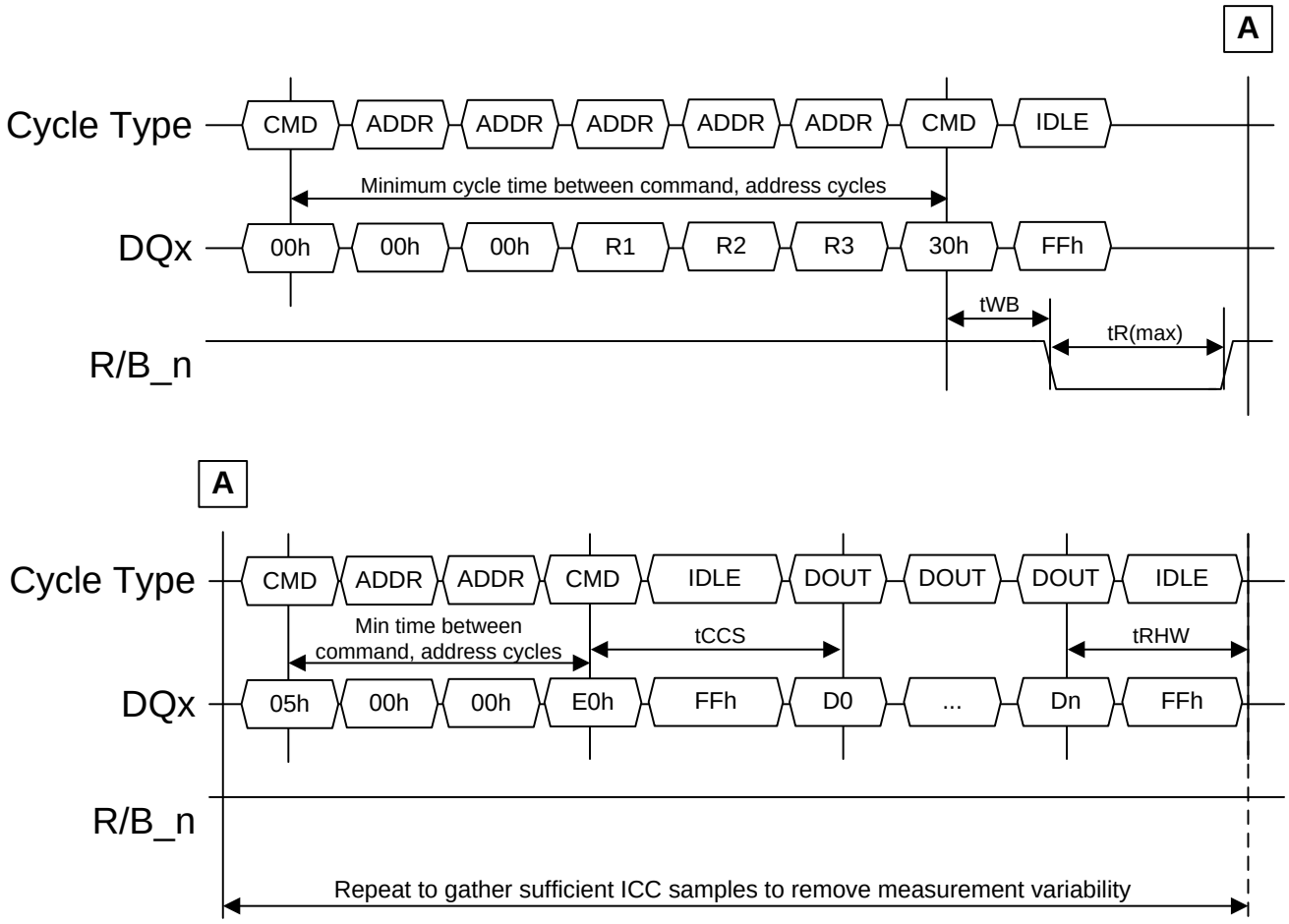

Figure 1 ICC4R and ICCO4R measurement procedure

Disposition log

11/7/2012	Erratum captured.
12/21/2012	Added ICCQ4W to Tables 8, 9, and 83
1/04/2012	Specified ICCQ4R test condition with 35 ohm drive strength setting

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