ONFI Technical Errata

Errata ID	**005**
Affected Spec Ver.	**ONFI 3.0, 3.1**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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This erratum clarifies data burst pause, exit, and end for NV-DDR2 interface.

The erratum also clarifies “recommended” and “normative” for 50 ohm output drive setting output slew rate.

Description of the specification change

In the ONFI 3.1 specification, Section 1.4.1:

1.4.1.5 data burst

A data burst is a continuous set of data input or data output cycles without a pause. Specifically, there is not more than a data cycle time of pause within the data sequence.

1.4.1.5 data burst end

The host issues a new command after exiting the data burst. This exits NAND read mode and ends the data burst.

1.4.1.5 data burst exit

The host brings CE_n, ALE or CLE high during the data burst. ODT is off (if enabled) when in exit state and warmup cycles are re-issued (if enabled) if the data burst is continued after exit.

1.4.1.5 data burst pause

The host stops DQS (input burst) or RE (output burst) during data burst. ODT (if enabled) stays enabled the entire pause time and warmup cycles (if enabled) are not re-issued when continuing the data burst from pause.

In the ONFI 3.1 specification, Section 4.3.4:

Pausing Data Input/Output

The host may pause data input or data output by entering the Idle state when using any data interface.

In the SDR data interface, pausing data input or data output is done by maintaining WE_n or RE_n at a value of one, respectively.

In the NV-DDR data interface, pausing data input or data output is done by clearing ALE and CLE both to zero. The host may continue data transfer by setting ALE and CLE both to one after the applicable tCAD time has passed.

In the NV-DDR2 data interface, pausing data input or data output may be done by placing the bus in an Idle ~~or Standby~~ state. The pausing of data output may also be done by pausing RE_n (RE_t/RE_c) and holding the signal(s) static high or low until the data burst is resumed. The pausing of data input may also be done by pausing DQS (DQS_t/DQS_c) and holding the signal(s) static high or low until the data burst is resumed. WE_n shall be held high during data input and output burst pause time. ODT (if enabled) stays ON the entire pause time and warmup cycles (if enabled) are not re-issued when re-starting a data burst from pause. The host is required to exit the data burst if it wishes to disable ODT or re-issue warmup cycles when re-starting. If warmup cycles are required, refer to section **Error! Reference source not found.** for details on re-issuing warmup cycles when ~~pausing~~ exiting and re-starting data bursts. If the host desires to end the data burst, after exiting the data burst, a new command is issued.

In the ONFI 3.1 specification, Section 4.13 (no changes, but added for clarity):

Warmup cycles are optional for both data output and data input, and if used, do not need to be configured to the same value. Warmup cycles apply to all commands, including SDR commands (refer to section **Error! Reference source not found.**). The warmup cycles shall be initiated at the start of each data burst when warmup cycles are enabled for that data transfer type. If the host pauses and then resumes a data transfer without exiting and re-entering the data burst, then the host shall not issue additional warmup cycles. Exiting and re-entering the data burst shall be performed by bringing ALE, CLE or CE_n high without latching with WE_n. In the case of not re-issuing warmup cycles, the host should take care to avoid signal integrity issues due to pausing the data transfer and resuming without warmup cycles.

In the ONFI 3.1 specification, Section 4.17.3.3:

Data Input Cycle Timings

NOTE:
1. tDBS references the last falling edge of either CLE, ALE or CE_n.
2. To ~~end~~ exit the data burst, either CE_n, ALE, or CLE is set to one by the host.

In the ONFI 3.1 specification, Section 4.17.3.4:

Data Output Cycle Timings

NOTE:
1. tDBS references the last falling edge of either CLE, ALE or CE_n.
2. To ~~end~~ exit the data burst, either CE_n, ALE, or CLE is set to one by the host. tCHZ only applies when CE_n is used to end the data burst.

In the ONFI 3.1 specification, Section 4.8:

The output slew rate requirements that the device shall comply with are defined in **Error! Reference source not found.**, **Error! Reference source not found.**, and **Error! Reference source not found.** for a single LUN per 8-bit data bus. The 18 Ohms, 25 Ohms, and 35 Ohms driver strengths output slew rate requirements are normative and shall be supported by the device; the host may choose whether to use those settings based on topology. The testing conditions that shall be used to verify the output slew rate are listed in **Error! Reference source not found.**

Disposition log

11/7/2012	Erratum captured.
1/9/2013	Added data burst end, exit and pause definitions.
1/23/2013	Minor editorial changes

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