ONFI Technical Errata

Errata ID	**007**
Affected Spec Ver.	**ONFI 2.1**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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This erratum clarifies the delta pin capacitance when multiple LUNs share a data bus.

Description of the specification technical flaw

Update Table 33 and preceding paragraph in section 4.2.3 as shown:

The input capacitance requirements are defined in Table 33. The testing conditions that shall be used to verify the input capacitance requirements are: temperature of 25 degrees Celsius, V_{IN} = 0V, and a CLK frequency of 100 MHz. The capacitance delta values measure the pin-to-pin capacitance for ~~the same LUN within a Target~~ all LUNs within a package. The capacitance delta values change based on the number of LUNs per x8 data bus.

Parameter	Symbol	Source Synchronous Timing Modes 0-5		Unit
		Min	Max	
Input capacitance, CLK	CCK	Typical - (# of LUNs per x8 data bus * 0.5 pF)	Typical + (# of LUNs per x8 data bus * 0.5 pF)	pF
Input capacitance delta, CLK	DCCK	x	0.25 * # of LUNs per x8 data bus	pF
Input capacitance, inputs	CIN	Typical - (# of LUNs per x8 data bus * 0.5 pF)	Typical + (# of LUNs per x8 data bus * 0.5 pF)	pF
Input capacitance delta, inputs	DCIN	x	0.5 * # of LUNs per x8 data bus	pF
Input capacitance, I/O	CIO	Typical - (# of LUNs per x8 data bus * 0.5 pF)	Typical + (# of LUNs per x8 data bus * 0.5 pF)	pF
Input capacitance delta, I/O	DCIO	x	0.5 * # of LUNs per x8 data bus	pF
Input capacitance, CE#, WP#	COTHER	x	5.0 * # of LUNs per x8 data bus	pF

NOTE:

1. Typical capacitance values for CCK, CIN, and CIO are specified in the parameter page. The allowable range for Typical capacitance values is specified in Table 34 for CLK and input pins and Table 35 for I/O pins.

Table 33 Input Capacitance, Minimum and Maximums

Disposition log

4/23/2009	Erratum captured.
6/17/2009	Erratum ratified.

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