ONFI Technical Errata

Errata ID	**013**
Affected Spec Ver.	**ONFI 1.0, 2.0 and 2.1**
Corrected Spec Ver.	

Submission info

Name	Company	Date
Amber Huffman	Intel	09/07/2009

Table 13 describes the asynchronous bus state based on the value of ALE and CLE. The RE# and WE# signals are shown to provide additional context regarding the direction of the data transfer. It is imprecise for command, address, data input, and data output cycles to indicate a static value for RE# and WE#. Rather, these cycles are defined by RE# or WE#, respectively, transitioning from zero to one. This erratum makes the description in Table 13 more precise.

Description of the specification technical flaw

Modify section 4.1.2 as shown, inserting the symbol showing transition from 0 to 1:

4.1.2 Bus State

ALE and CLE are used to determine the current bus state in asynchronous and source synchronous data interfaces. Table 13 describes the bus state for asynchronous. Note that in asynchronous the value 11b for ALE/CLE is undefined.

CE#	ALE	CLE	WE#	RE#	Asynchronous Bus State
1	X	X	X	X	Standby
0	0	0	1	1	Idle
0	0	1	~~0~~ ↑	1	Command cycle
0	1	0	~~0~~ ↑	1	Address cycle
0	0	0	~~0~~ ↑	1	Data input cycle
0	0	0	1	~~0~~ ↓	Data output cycle
0	1	1	X	X	Undefined

Table 13 ALE/CLE value and asynchronous bus state

Disposition log

9/7/2009	Erratum captured.
10/20/2009	Erratum ratified.

Technical input submitted to the ONFI Workgroup is subject to the terms of the ONFI contributor's agreement.