ONFI Technical Errata

Errata ID	**003**
Affected Spec Ver.	**ONFI 2.1**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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Description of the specification technical flaw (add space as needed)

In the command cycle timing diagram for the source synchronous data interface, the cycle that tCAD is measured from is shown as an idle cycle. However, as long as tCAD requirements are met, the preceding bus cycle may be an idle, command, address, or data cycle. This erratum makes that clarification.

Description of the correction

Add the note below Figure 29 in section 4.3.2.1 on Command Cycle Timings as shown:

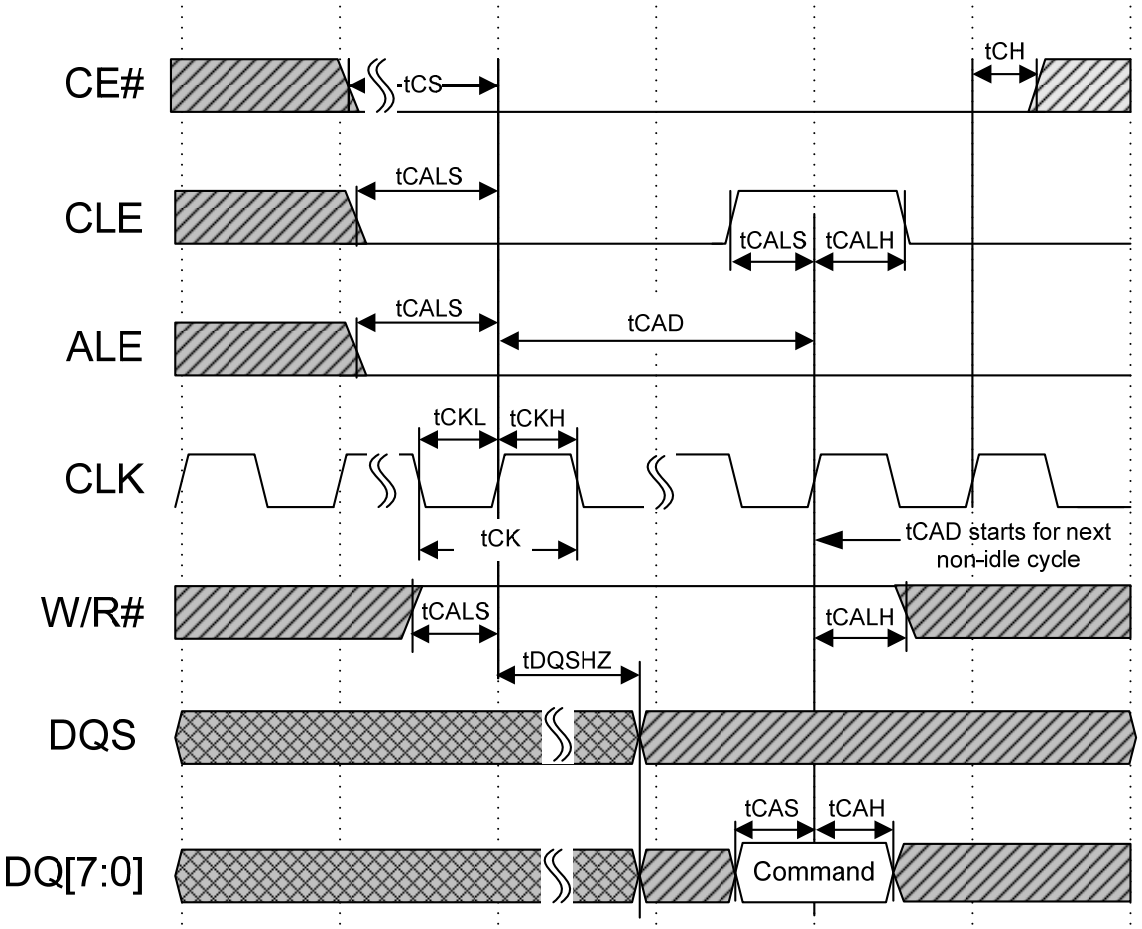

Figure 29 Command cycle timings

Note: The cycle that tCAD is measured from may be an idle cycle (as shown), another command cycle, an address cycle, or a data cycle. The idle cycle is shown in this diagram for simplicity.

Disposition log

2/18/2009	Erratum captured.
5/5/2009	Erratum ratified.

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