ONFI Technical Errata

Errata ID	**008**
Affected Spec Ver.	**ONFI 1.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
Amber Huffman	Intel	6/3/2007

Description of the specification technical flaw (add space as needed)

R/B# is required to be valid within 10 microseconds after Vcc reaches its minimum value. The issue is that if Vcc ramps very quickly (within a few microseconds for example), this requirement is difficult to meet. Hosts tend to ramp Vcc at a reasonable rate, so burdening the NAND to meet this requirement when the ramp rate is very fast does not make sense. Therefore, this erratum establishes a minimum amount of time from when Vcc starts to ramp before R/B# is considered valid.

Description of the correction

Modify section 2.13.1 as shown, including updates to Figure 8:

Once V_{CC} reaches the V_{CC} minimum value listed in Table 5 and power is stable, the R/B# signal shall be valid after 10 µs and shall be set to one (Ready) within 1 ms. This requirement assumes a reasonable Vcc ramp rate. R/B# is undefined until 50 µs has elapsed after V_{CC} has started to ramp. The R/B# signal is not valid until both of these conditions are met.

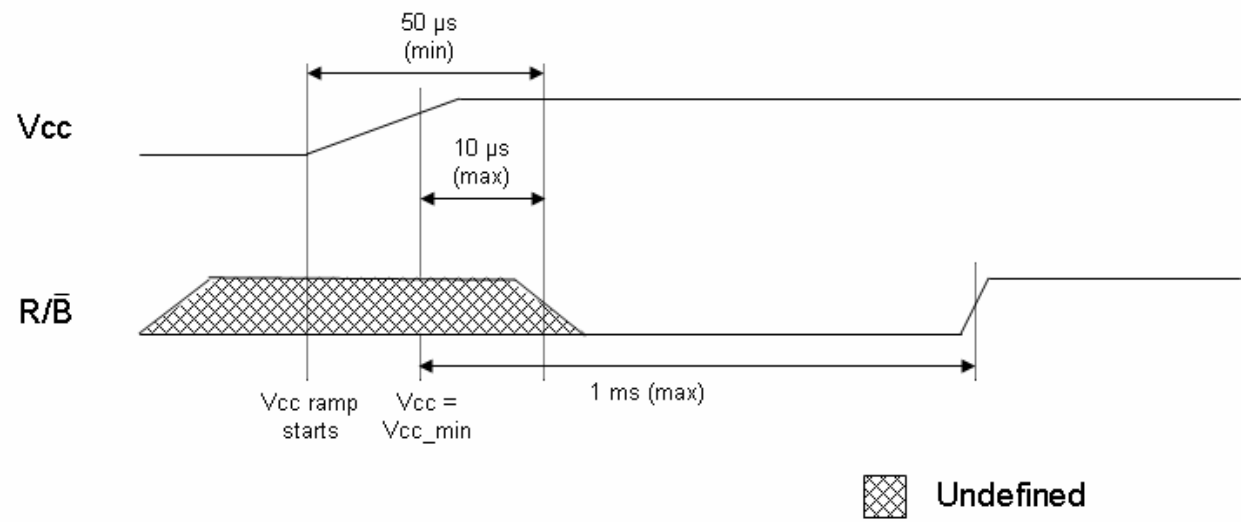

Figure 8 R/B# Power-On Behavior

Ready/Busy is implemented as an open drain circuit, thus a pull-up resistor shall be used for termination. The combination of the pull-up resistor and the capacitive loading of the R/B# circuit determines the rise time of R/B#.

Disposition log

6/3/2007	Erratum captured.
8/2/2007	Erratum ratified.

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