ONFI Technical Errata

Errata ID	**003**
Affected Spec Ver.	**ONFI 1.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
Amber Huffman	Intel	1/26/2007

Description of the specification technical flaw (add space as needed)

This erratum addresses four minor issues in the specification.

The first issue is that the 0Ch opcode is not specified for any use, nor marked as Vendor Specific, Future Standardization or Reserved. This erratum marks the 0Ch opcode as reserved.

The second issue is that the CRC example code in Appendix A does not include declarations for two variables. One line of code is added to declare these variables.

The third issue is that for the reported block endurance, it is not specified how to report values that could be reported in multiple formats. This issue is addressed by requiring the “value” field to be the smallest possible.

The fourth issue is that the definition of Reset implies that no feature settings are retained across a Reset command. This issue is addressed by clarifying the definition of Reset.

Description of the correction

Update Table 15 in section 5.1 to insert opcode 0Ch as shown:

Type	Opcode
Vendor Specific	02h – 04h, 08h, 16h – 17h, 19h, 1Dh, 20h – 22h, 25h – 29h, 2Bh, 2Dh – 2Fh, 33h, 36h – 3Eh, 40h – 41h, 48h, 4Ch, 53h – 55h, 68h, 72h – 75h, 84h, 87h – 89h, 91h – BFh, CFh, F1-F4h
Future Standardization	06h, 23h – 24h, 2Ah, 2Ch, 32h, 34h, 65h, 71h, 79h – 7Bh, 81h
Reserved	01h, 07h, ~~09h – 0Bh, 0Dh – 0Fh,~~ 09h – 0Fh, 12h-14h, 18h, 1Ah – 1Ch, 1Eh – 1Fh, 42h – 47h, 49h – 4Bh, 4Dh – 52h, 56h – 5Fh, 61h – 64h, 66h – 67h, 69h – 6Fh, 76h – 77h, 7Ch – 7Fh, 82h – 83h, 86h, 8Ah – 8Fh, C0h – CEh, D2h –DFh, E1h – EBh, F0h, F5h – FEh

Modify the CRC function in Appendix A as shown:

```
int main(int argc, char* argv[])
{
      // Bit by bit algorithm without augmented zero bytes
      const unsigned long crcinit = 0x4F4E;     // Initial CRC value in the
                                                // shift register
      const int order = 16;                     // Order of the CRC-16
      const unsigned long polynom = 0x8005;     // Polynomial
      unsigned long i, j, c, bit;
      unsigned long crc = crcinit;              // Initialize the shift
                                                // register with 0x4F4E
      unsigned long data_in;
      int dataByteCount = 0;
      unsigned long crcmask, crchighbit;
      crcmask = ((((unsigned long)1<<(order-1))-1)<<1)|1;
      crchighbit = (unsigned long)1<<(order-1);
```

< AS SPECIFIED IN APPENDIX A>

Modify the third paragraph of section 5.4.1.19 as shown:

The block endurance is reported in terms of a value and a multiplier according to the following equation: value x $10^{multiplier}$. Byte 105 comprises the value. Byte 106 comprises the multiplier. For example, a target with an endurance of 75,000 cycles would report this as a value of 75 and a multiplier of 3 (75 x 10^3). For a write once device, the target shall report a value of 1 and a multiplier of 0. For a read-only device, the target shall report a value of 0. The value field shall be the smallest possible; for example 100,000 shall be reported as a value of 1 and a multiplier of 5 (1 x 10^5).

Modify the first paragraph of section 5.2 as shown:

The Reset function puts the target in its default power-up state. Note that some feature settings are retained across Reset commands (as specified in section 5.20). As part of the Reset command, all LUNs are also reset. The command may be executed with the target in any state. **Error! Reference source not found.** defines the Reset behavior and timings.

Disposition log

1/26/2007	Erratum captured
2/4/2007	Added Reset item to the errata.
4/6/2007	Ratified.

Technical input submitted to the ONFI Workgroup is subject to the terms of the ONFI contributor's agreement.