ONFI Technical Errata

Errata ID	**007**
Affected Spec Ver.	**ONFI 1.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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Description of the specification technical flaw (add space as needed)

In a copyback operation, the behavioral flow does not correctly transition back to T_RD_Copyback after going through T_Idle_RB_Transition. This erratum causes transitions through T_Idle_RB_Transition to always return to the calling state.

In a Read operation, the tbChgCol variable is not being set to TRUE. This erratum ensures tbChgCol is set to TRUE when a new Read operation is issued.

The tbStatusOut variable is not always set to FALSE as it should be in several command flows. To correct this, the erratum sets the tbStatusOut variable to FALSE uniformly in T_Cmd_Decode and removes this setting from individual command states.

The specification does not show tADL in the definition of Set Features. This erratum adds the tADL parameter to the Set Features diagram.

The specification allows sequential Read Cache (31h) commands to cross block boundaries within a LUN. Due to wear leveling and block management algorithms, crossing block boundaries is infrequent. To simplify NAND design and to conform to what is more common in the industry, this capability is being removed.

Description of the correction

Modify state T_Idle_RB_Transition in section 7.1.2 as shown:

T_Idle_RB_Transition	R/B# is set to the AND of all LUN status register SR[6] values.[1]		
	1. Unconditional	→	tReturnState
	~~1. State entered from T_Idle_Rd~~	~~→~~	~~T_Idle_Rd~~
	~~2. Else~~	~~→~~	~~T_Idle~~
	NOTE: 1. R/B# may transition to a new value prior to the Target re-entering an idle condition when LUN level commands are in the process of being issued.		

Modify state T_RD_AddrWait in section 7.1.10 as shown:

T_RD_AddrWait	tLastCmd set to 00h. Set tbChgCol to TRUE. If R/B# is cleared to zero, then tbStatus78hReq is set to TRUE. Wait for an address cycle.		
	1. Address cycle received	→	T_RD_Addr

Modify state T_Cmd_Decode in section 7.1.2 as shown:

T_Cmd_Decode[1]	Decode command received. tbStatusOut is set to FALSE. If R/B# is set to one and command received is not 70h (Read Status), then tbStatus78hReq is set to FALSE.		
	1. (Command 80h (Page Program) or command 60h (Block Erase) decoded) and WP# is low	→	T_Idle
	2. Command FFh (Reset) decoded	→	T_RST_Execute
	3. Command 90h (Read ID) decoded	→	T_RID_Execute
	4. Command ECh (Read Parameter Page) decoded	→	T_RPP_Execute
	5. Command EDh (Read Unique ID) decoded	→	T_RU_Execute
	6. Command 80h (Page Program) decoded and WP# is high	→	T_PP_Execute
	7. Command 60h (Block Erase) decoded and WP# is high	→	T_BE_Execute
	8. Command 00h (Read) decoded	→	T_RD_Execute
	9. Command EFh (Set Features) decoded	→	T_SF_Execute
	10. Command EEh (Get Features) decoded	→	T_GF_Execute
	11. Command 70h (Read Status) decoded	→	T_RS_Execute
	12. Command 78h (Read Status Enhanced) decoded	→	T_RSE_Execute
	NOTE: 1. The host shall ensure R/B# is set to one before issuing Target level commands (Reset, Read ID, Read Parameter Page, Read Unique ID, Set Features, Get Features).		

Modify state T_RST_Execute in section 7.1.4 as shown:

T_RST_Execute[1]	The target performs the following actions: 1. tLastCmd set to FFh. ~~2. tbStatusOut is set to FALSE.~~ 2. The target sends a Reset request to each LUN. 3. Set tbChgCol to FALSE. 4. Request all LUNs invalidate page register(s).		
	1. Unconditional	→	T_RST_Perform
	NOTE: 1. This state is entered asynchronously as a result of receiving a Reset (FFh) command, except if this is the first Reset after power-on.		

Modify state T_RPP_Execute in section 7.1.6 as shown:

T_RPP_Execute	The target performs the following actions: 1. tLastCmd set to ECh. ~~2. Set tbStatusOut to FALSE.~~ 2. Set tbChgCol to TRUE. 3. Wait for an address cycle. 4. Request all LUNs invalidate page register(s). 5. Target selects LUN to execute parameter page read, sets tLunSelected to the address of this LUN.		
	1. Address cycle of 00h received	→	T_RPP_ReadParams

Modify state T_RU_Execute in section 7.1.7 as shown:

T_RU_Execute	The target performs the following actions: 1. tLastCmd set to EDh. ~~2. Set tbStatusOut to FALSE.~~ 2. Set tbChgCol to TRUE. 3. Request all LUNs invalidate page register(s). 4. Wait for an address cycle. 5. Target selects LUN to execute unique ID read, sets tLunSelected to the address of this LUN.		
	1. Address cycle of 00h received	→	T_RU_ReadUid

Modify state T_BE_Execute in section 7.1.9 as shown:

T_BE_Execute	The target performs the following actions: 1. tLastCmd set to 60h. ~~2. tbStatusOut set to FALSE.~~ 2. If R/B# is cleared to zero, then tbStatus78hReq is set to TRUE. 3. Wait for a row address cycle.		
	1. Address cycle received	→	T_BE_Addr

Modify state T_GF_Execute in section 7.1.12 as shown:

T_GF_Execute	The target performs the following actions: 1. tLastCmd set to EEh. 2. Request all LUNs invalidate page register(s). 3. Set tbChgCol to FALSE. ~~4. Set tbStatusOut to FALSE.~~ 4. Wait for an address cycle.		
1. Address cycle received		→	T_GF_Addr

Update Figure 40 to specify tADL as shown:

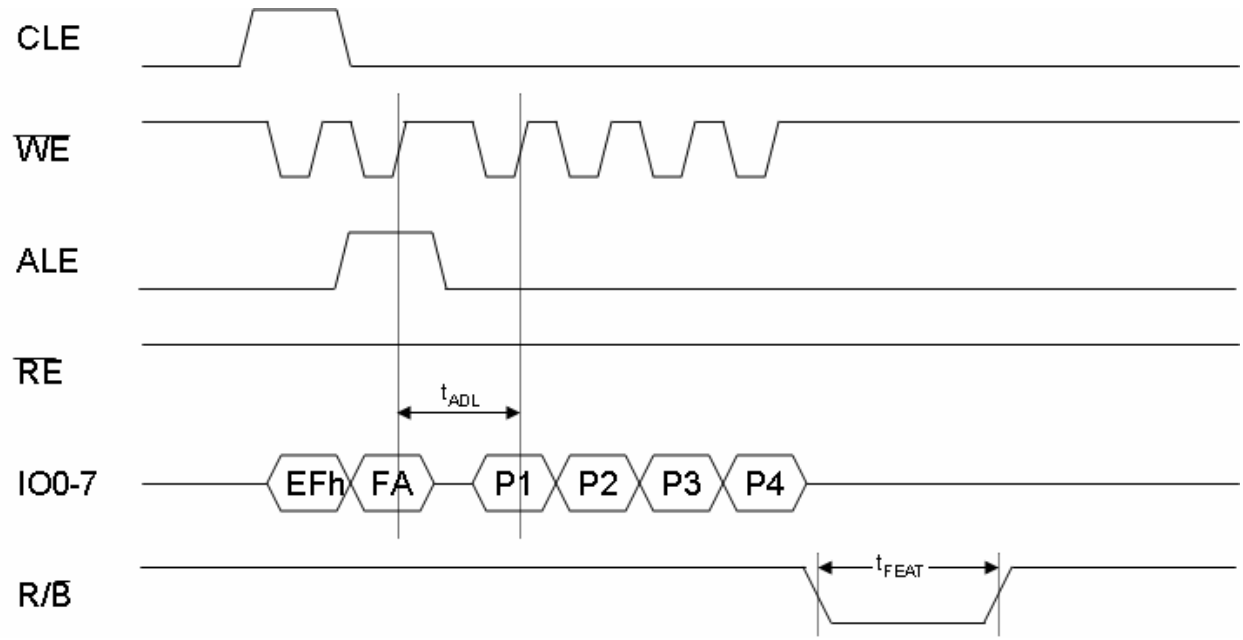

Figure 40 Set Features timing

Modify the third paragraph of section 5.12 as shown:

The host shall not issue a sequential Read Cache (31h) command after the last page of a block ~~the LUN~~ is read. If commands are issued to multiple LUNs at the same time, the host shall execute a Read Status Enhanced (78h) command to select the LUN prior to issuing a sequential Read Cache (31h) or Read Cache End (3Fh) command for that LUN.

Disposition log

5/18/2007	Erratum captured.
5/24/2007	Added sequential Read Cache clarification.
7/23/2007	Erratum ratified.

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