Discover Your Memory System's Signaling Margin Without Test Equipment

Memory products are the core of all electronic innovations. This industry pairs very high-performance standards with rapid new technology introductions. For example, Micron's DRAM process nodes deliver memory benefits ranging from more speed and lower latencies — saving money and enabling a competitive cost structure — to electronic devices and systems.

But the market continues to demand even faster cycle times. Growth and diversification stress memory interface design in high-volume manufacturing and challenge traditional methods of qualifying signal integrity in end systems.

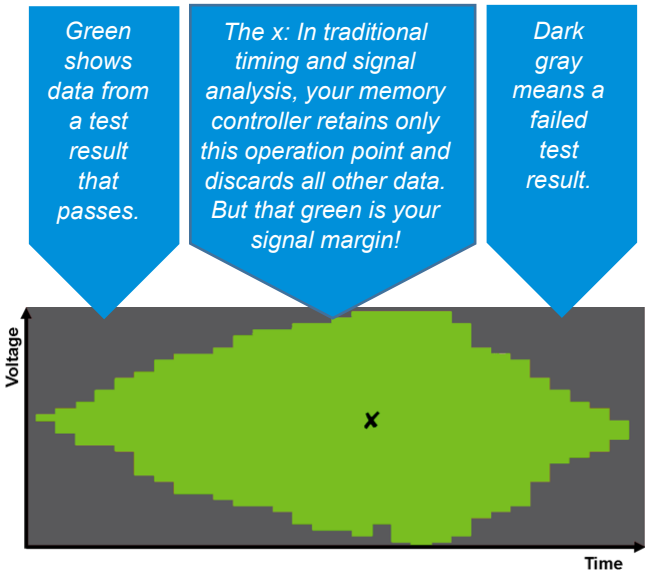


Figure 1: Memory Timing and Signal Analysis Test Results Plotted in Typical "Data Eye" (x-axis = time; y-axis = voltage)

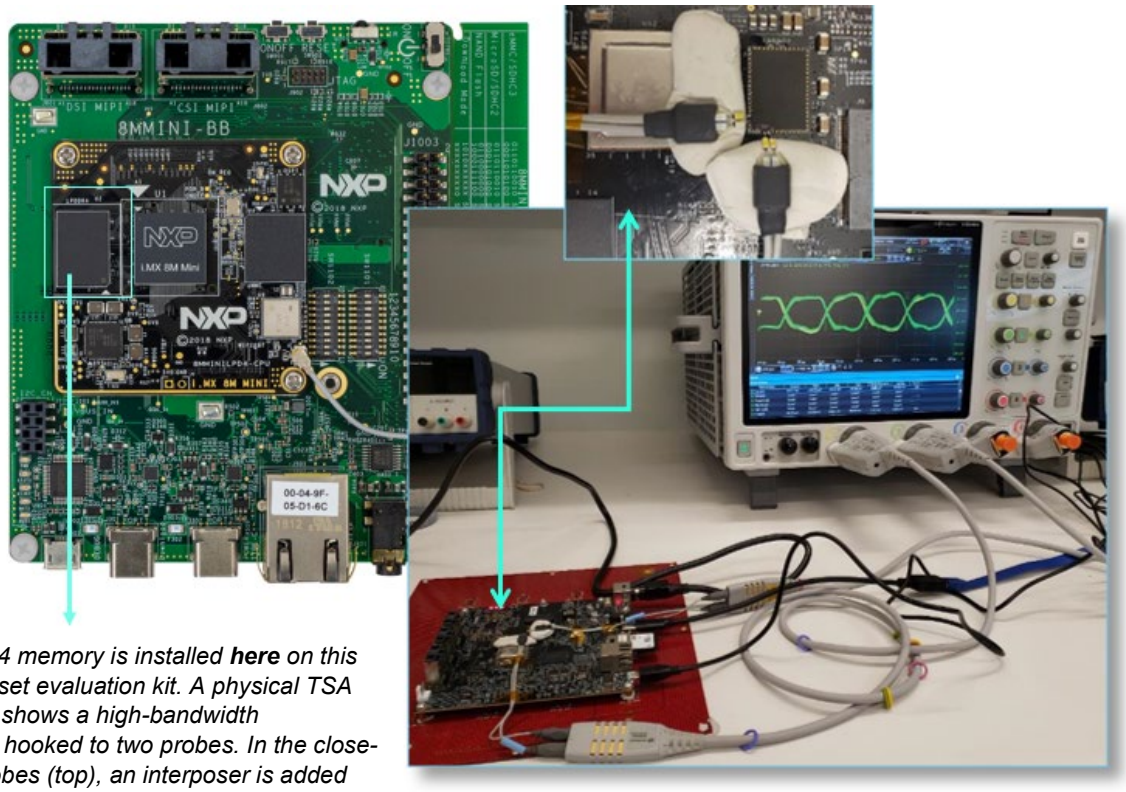
Introducing Virtual Timing and Signal Analysis (vTSA)

Testing the memory interfaces helps determine that a manufactured printed circuit board (PCB) will operate as expected over its useful life. Signal margin measurement is one way to predict whether your system can handle the use conditions you plan for it. Physical TSA (pTSA) connects probes and expensive testing equipment to a PCB to check its signal margin and critical timing, power supply levels, and configuration settings.

The vTSA approach enables accurate characterization of the entire memory interface quickly and easily and without requiring testing equipment (Table 1). And while vTSA is a software approach, it's not a simulation. It leverages margin analysis that the memory controller already performs to determine operation points. Most of that data is traditionally discarded (Figure 1). By adding software code to the chipset, that data can be retained.

Table 1: Side-by-Side Comparison of Memory Timing and Signal Analysis (TSA) Approaches

Topic	With Traditional Physical TSA	With Micron Virtual TSA
Equipment required	High-bandwidth oscilloscope, logic analyzer, probes, interposers, sockets	None
Accuracy	• Affected by test hardware • Usually measured at memory interface only	• No test hardware needed • Measurements at memory and memory controller interface
Statistical significance	Sampled signals	Full interface
Risk	Rework may damage system	Low risk of damage since no rework
Completion time	Weeks	Days



*Micron DDR4 memory is installed **here** on this popular chipset evaluation kit. A physical TSA setup (right) shows a high-bandwidth oscilloscope hooked to two probes. In the close-up of the probes (top), an interposer is added between the DRAM device and the PCB for testing, so rework is required.*

Figure 2: Testing Equipment in Traditional Timing and Signal Analysis of Memory Devices

Understanding Traditional Physical Testing and Signal Analysis (pTSA)

Historically, pTSA is done by using probes to connect test equipment to a subset of the DRAM or other memory interface and taking measurements with a high-bandwidth oscilloscope (Figure 2). The memory device of interest is often removed, the board cleaned, interposers inserted between the system and device, and all are soldered back together There are several pitfalls to this approach:

- Test equipment is expensive. High-bandwidth oscilloscopes currently cost US$300,000 to $500,000.
- Test equipment affects signal path. By inserting test equipment, you affect the signaling itself just to observe it. Even with interposers and sockets as transparent as possible, they still have some impact.
- Getting test equipment hooked up and soldered requires rework. The rework process always comes with the risk of damaging the system or the memory device.
- It's unfeasible to measure the entire interface because the process is very time-consuming to take measurements in a pTSA. Just taking measurements on a subset (as in Figure 2) of the interface is a long process, so it takes two to six weeks or more across the entire memory interface. Most testing focuses on subsets of the board.

These pTSA pitfalls hinder design cycle time and quality as system speeds accelerate. In the early days of memory design, only a few of the most important, or highest speed, signals needed detailed analysis or design. In modern (as in, faster than 100 MHz) circuit designs, essentially all chips and memory devices must be designed and qualified with signal integrity in mind.

Advancing Efficient Signal Analysis With vTSA

To operate modern memory devices, memory controllers must be able to shift the delivery of signals, shift strobes, alter timings, change voltage references, and do much more for incoming and outgoing signals to determine the best operating points for the system. This characterization, both in the time and voltage domain, can be used to understand the size and shape of the data eye. When the data signals, as DQ0, DQ1, and so on, are delivered by the memory device, both negative and positive results show up on the x-axis. The controller also changes the reference voltage, which is shown on the y-axis. These test results paint the data eye, as in Figure 1, where green indicates expected data and dark gray means a failed signal. The traditional memory controller determines its reference point, the black x in the center of the eye, and drops the rest of the data.

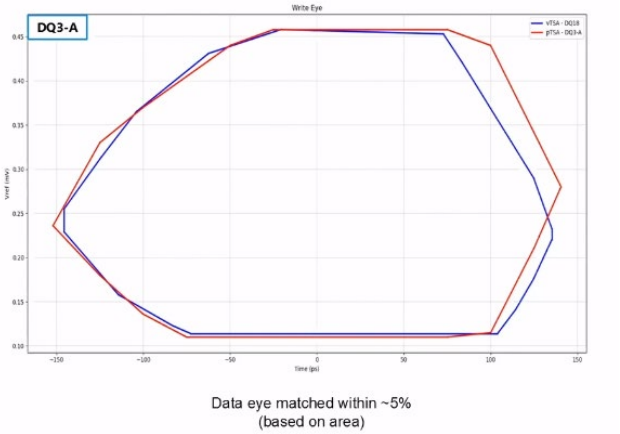


Figure 3: Comparison of vTSA (Blue) and pTSA (Red) Data Eye Results on an MX8M Mini EVK (When Mapped, Area Measurements Varied by Only About 5%)

To set up vTSA, Micron helps chipset manufacturers identify some minor software updates to their manufacturing code base. These enable the memory controller to retain the full margin-testing information and make it available for download and analysis. vTSA provides the results as tables and a data eye. Though vTSA delivers results faster, easier and with less risk, those results are extremely close to those from pTSA (Figure 3).

Recognizing the Merits of vTSA

As you saw in Table 1 and in Figures 1-3, vTSA has several advantages over pTSA:

- vTSA delivers data in a matter of minutes that physical testing might take weeks to do.
- vTSA avoids possible signal impact from physically testing the PCB.
- vTSA reduces risk since no rework, probes or interposers are required.
- vTSA collects data across the entire memory interface, including every DQ and every command/address line.
- vTSA eliminates the need for expensive testing equipment.

Switching to the vTSA Approach

vTSA is an important tool that can give you access to the information you need quickly to shorten your learning cycles. This quick turnaround allows you to discover whether you have marginalities early on and address those before they become a bigger problem. Reducing time and risk, vTSA helps accelerate qualification of memory devices to ensure quality and performance while speeding systems to market. Sound useful? Make it a requirement of your SoC vendors to enable vTSA capability in their chipsets and provide the toolsets to use it.

Get Involved

For more information, visit micron.com/vtsa. Contact us at vtsa@micron.com if you are a **board designer** or **system architect** and want to find vTSA-aligned ecosystem connections for your future products. Or, if you are a **SoC/memory controller vendor** and want to help your customers to achieve more robust systems, we can help.

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