Technical Note

Power Supply Electrical Requirements for Micron's 2100AI/AT PCIe NVMe BGA SSD

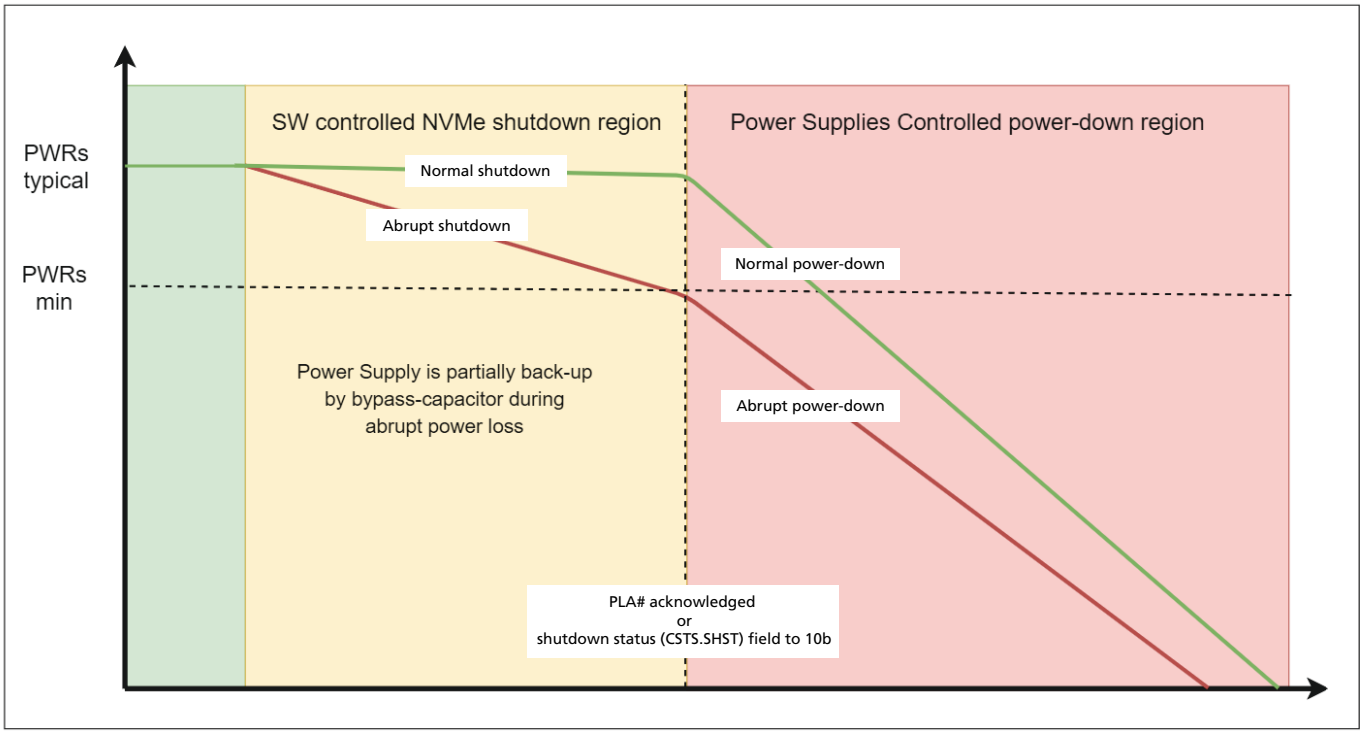
Introduction

This technical note summarizes the power supply electrical requirements for Micron's 2100AI/AT PCIe NVMe SSDs, including:

- Component electrical characteristics
- Voltage supply power-on sequencing
- Voltage supply power-off sequencing
- Power ramp timing
- Power rail slew rate
- Power-up timing

This technical note covers the power-down phase during voltage supply power-off sequencing, which is represented by the red area in the figure below. To properly design your system to manage the NVMe shutdown phase, which is represented by yellow in the figure below, refer primarily to Micron's Technical Notes, "TN-FD-57 2100AI/AT NVMe Shutdown" and "TN-FD-54 2100AI/AT PLN#/PLA#."

Figure 1: Shutdown and Power-Down Regions



Component Electrical Characteristics

Environmental conditions beyond those listed may cause device instability. Design attention should be given to guarantee power stability of SSD, especially in case of transition from idle/low power state to active read/write operations.

BGA Type

Table 1: Operating and Extended Ratings

Parameter Symbol	Condition	Value	Unit
PWR_1	Max	3.63	V
	Nominal	3.3	V
	Min	2.97[1, 5]	V
	Voltage Fall Threshold (VFR_PWR_1) [2]	2.7 [4]	V
PWR_2	Max	1.26	V
	Nominal	1.2	V
	Min	1.14[5]	V
	Voltage Fall Threshold (VFR_PWR_2) [2]	1.05 [4]	V
PWR_3	Max	0.945	V
	Nominal	0.9	V
	Min	0.860[5]	V
	Voltage Fall Threshold (VFR_PWR_3) [2,3]	0.72 [4]	V
	Voltage Rise Threshold (VRR_PWR_3) [3]	0.76 [4]	V
Power-On minimum time (all PWRs) after NVMe initialization	Min	1	s
Power-Off minimum time (all PWRs)	Min	1 [6]	s

Notes: 1. SSD FW Enter in pause mode, it will resume once power recover.
2. FW will drive NAND WP# low aborting any on going operation; in flight data will be lost. Any host command will time out. SSD remains unresponsive until PCIe bus reset is triggered by the host.
3. VFR refers to high to low voltage transition like during voltage drops; if VFR is reached, SSD controller will perform Power On Reset making the drive unresponsive for the time necessary for the operation to complete. Conversely VRR refers to low to high voltage transition like during system power up phase; SSD controller logic voltage is in reset state until PWR_3 crosses The PWR_3 lock-out circuit is designed to include some hysteresis and a delay (about 6.8µs) to minimize spurious Power On Reset.
4. Threshold voltage values are guaranteed by design and they have been characterized on limited samples. Power supplies must rise or fall monotonically once the VRR/VRF are respectively crossed.
5. Operating the device below minimum time or minimum voltage can harm the device.
6. Each power supply must remain below 100mV for at least 1s (PCI-SIG specifies 1ms) before the next power-on sequence.

Power-Up Characteristics

Voltage Supply Power-On Sequencing

Voltage Power-On sequencing according to PCI-SIG specification is here below presented.

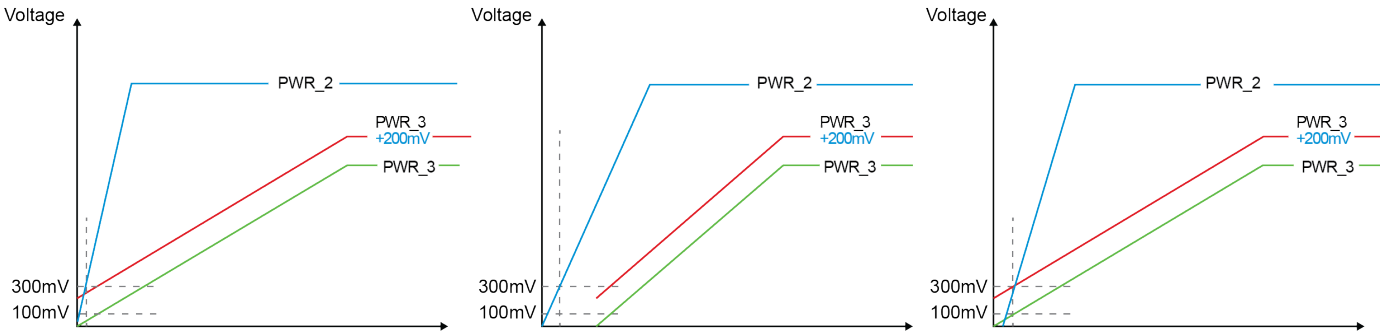
During power on, the host should apply the following recommendations for sequencing the voltages on the PWR_1 supply, PWR_2 supply, and PWR_3 supply:

- After the voltage on the PWR_2 supply or the voltage on PWR_3 supply reach 300mV, the voltage on PWR_2 must remain greater than the voltage on PWR_3 by at least 200mV.
- Voltage on the PWR_1 supply has no timing relationship relative to the voltage on the PWR_3 or PWR_2 supply.

If the power-on sequencing recommendations are not followed, the device may not power on correctly or may be damaged. Results are vendor-specific, and implications may not be seen immediately.

The figure below shows three valid power-on ramp examples for the case where each of the power rails is assigned a different voltage. The first example shows PWR_2 reaching 300mV before PWR_3 reaches 100mV. The second example shows PWR_2 well above 300mV by the time PWR_3 reaches 100mV. The third case is similar to the first case with PWR_3 being at 100mV when PWR_2 reaches 300mV. Note that the PWR_1 rail is not shown since it has no timing relationship to the other rails.

Figure 2: Power-On Ramp Examples



Power Ramp Timing

Power ramp timing is defined as the time the power supply needs to ramp to a valid voltage (shown in the Operating and Extended Ratings table above). This timing is recommended for power-on only.

Table 2: Power Ramp Timing

Supply Voltage	Max
PWR_1	35ms
PWR_2	20ms
PWR_3	20ms

Notes: 1. The minimum timing may be calculated from the maximum slew rate recommendation in

Power Rail Slew Rate

The maximum power rail slew rate is shown below. These values are only defined for ESD protection purposes. In general, these values are not meant for inrush current control, even considering that inrush current does not apply to any soldered components.

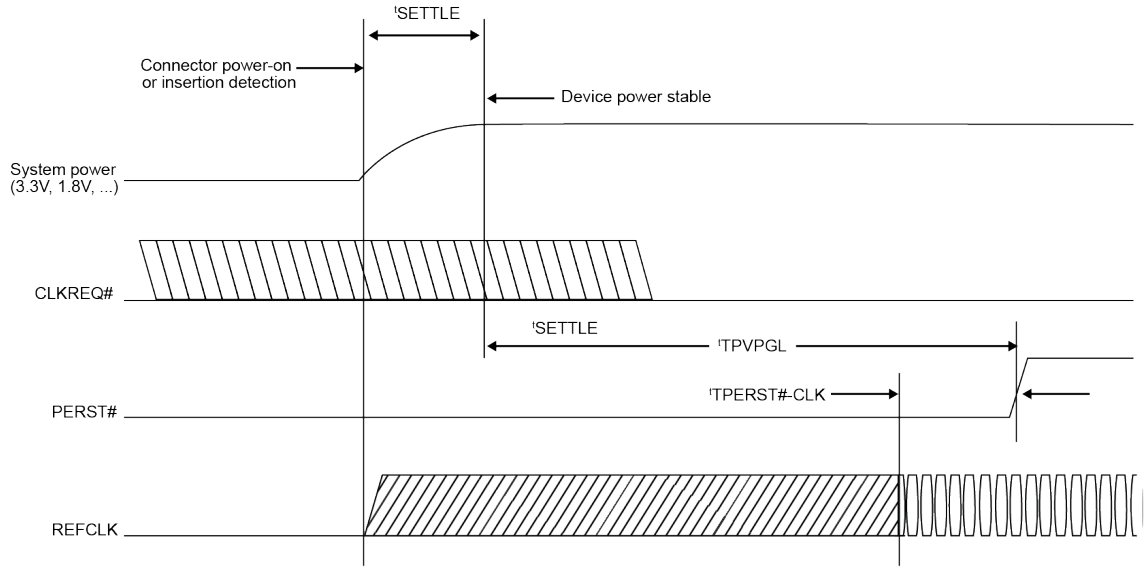
Table 3: Power Rail Slew Rate

Symbol	Parameter	Max	Condition
TSLEW_PWR_1	Voltage slew rate of the PWR_1 rail	100 kV/s	No load
TSLEW_PWR_2	Voltage slew rate of the PWR_2 rail	100 kV/s	No load
TSEWL_PWR_3	Voltage slew rate of the PWR_3 rail	100 kV/s	No load

Power-Up Timing

The figure below shows an overview of the power-up sequence for BGAs powered from the system power rail. The table lists the power-up timing variable values.

Figure 3: Power-Up Sequence



Notes: 1. ^{t}SETTLE is the time it takes all power rails to reach their minimum operating voltage that is from all power rails at 0V to the last power rail to reach its minimum valid operating voltage. All other PCI Express-related timing events begin after all power rails reach their minimum operating voltage.
2. System power (3.3V, 1.8V,..) waveform is simplified for both M.2 and BGA form factors. For detailed BGA supply power-on requirements, refers to the Voltage Supply Power-On Sequencing section.

Table 4: Power-Up Timing

Symbol	Parameter	Min	Max	Units
^{t}PVPGL	Power valid to PERST# input inactive (see note above).	Implementation-specific; 50ms recommended		ms
^{t}PERST#-CLK	REFCLK stable before PERST# inactive	100		µs

Notes: 1. Power valid when all voltage supply rails reach their respective V_{MIN}.

Power-Down Characteristics

Voltage Supply Power-Off Sequencing

This section examines the voltage power-off sequencing according to the PCI-SIG specification. During power off, the host should apply the following recommendations for sequencing the voltages on the PWR_1 supply, PWR_2 supply, and PWR_3 supply:

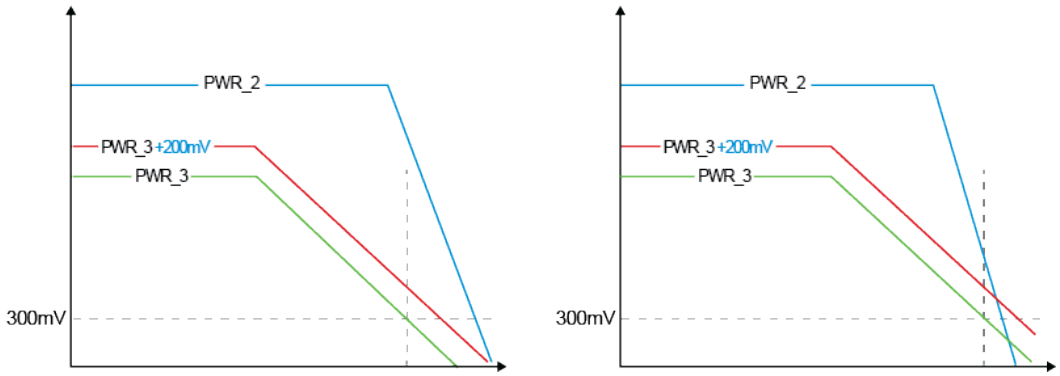
- Before the voltage on the PWR_3 supply and PWR_2 supply reaches 300mV, the voltage on PWR_2 must remain greater than the voltage on PWR_3 by 200mV.
- After the voltage on both the PWR_2 supply and the PWR_3 supply is below 300mV, there is no specified relationship between the two supplies.
- The voltage on all supplies must remain below 100mV for at least 1s (PCI-SIG specifies 1ms) before the power-on sequence is restarted.

If the power-off sequencing recommendations are not followed, the device may not power on correctly or may be damaged.

The figure below shows two valid power-off ramp examples where each power rail is assigned a different voltage.

Note:

Figure 4: Power-Off Ramp Examples



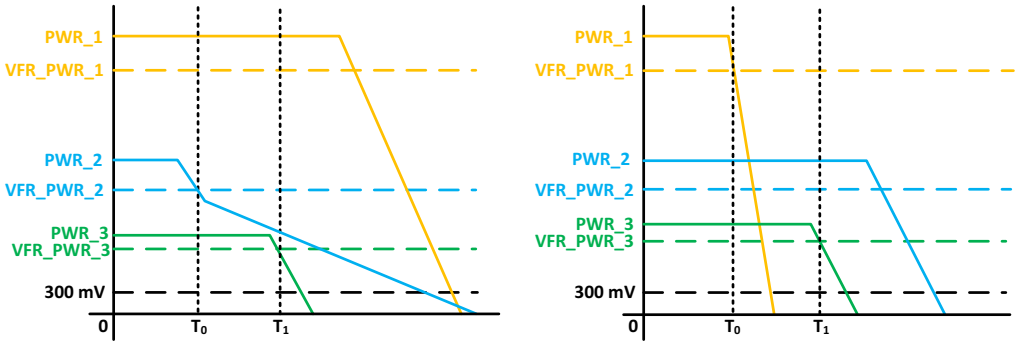
Note: 1. PWR_1 rail is not shown because it has no timing relationship to the other rails according to the PCI-SIG specification. However, a proper PWR_1 ramp down may increase system reliability when abrupt power loss occurs as explained in the next section below.

Additional Recommendations for 2100AI/AT

Implementing the recommended device shutdown sequence provides additional reliability in the case of an abrupt power-down scenario:

- Prior to the power-down voltage sequence, the host ensures an orderly shutdown of the NVMe controller by following the normal NVMe shutdown procedure. Alternatively, in case of an emergency shutdown, the host performs the abrupt NVMe shutdown procedure. Both procedures should be implemented as per NVMe specification. If your system design implements both normal NVMe shutdown and abrupt NVMe shutdown or PLN#/PLA#-based shutdown (including 2s PWRs hold time) the next two recommendations do not strictly apply. Refer to Micron's Technical Note, "TN-FD-57 2100AI/AT NVMeShutdown," for more information.
- PWR_2 crosses the VFR_PWR_2 threshold first, then after a delay of T1-T0 ≥ 550µs, the PWR_3 crosses the VFR_PWR_3 threshold while PWR_1 remains stable for longer using back-up capacitors. Alternatively, first PWR_1 shall cross VFR_PWR_1 threshold, then after a delay of T1-T0 ≥ 550µs, the PWR_2 and PWR_3 ramp down as described in the Voltage Supply Power-Off Sequencing section above. When PWR2 / PWR1 voltage crosses VFR_PWR_2 / VFR_PWR_1 threshold respectively, the SSD micro-controller asserts the NAND write protect signal (WP#), which protects the medium from any further inadvertent PROGRAM and ERASE operations and triggering ongoing operations to be properly suspended and aborted.
- The power sequence must be guaranteed in any power-off scenario, including power cut and power loss. It is assumed that the power-down ramps are monotonic at least until 300mV is reached.

Figure 5: Recommended Power-Off Ramp Examples



References

- Micron 2100AT PCIe NVMe SSD datasheet and 2100AI PCIe NVMe SSD datasheet
- Micron TN-FD-57 2100AI/AT NVMeShutdown
- Micron TN-FD-54 2100AI/ATPLN#/PLA#
- Supporting PCIe and SATA BGA form factor for SSDs ECN, Nov 10 2015 from PCI-SIG adapted for 1.2V and 0.9V BGA voltage
- PCI Express Electromechanical Specification, PCI Express M.2 Specification Revision 3.0, Version 1.2 June 26 2019
- NVM Express, Revision 1.3c

Revision History

Rev. C – 04/2021

- Removed Maximum Current per Power Rail table. Refer to the product data sheet instead.
- Clarified delay definition during ramp down of power rails in the Additional Recommendations for 2100AI/ATsection.
- Added a note into the Power-Up Sequence figure.
- Updated the Introduction to clarify the difference between NVMe shutdown and voltage supply power-off.
- Updated Operating and Extended Ratings table. Added system reliability recommendation for 1s minimum power-on time after NVMe initialization to prevent fast cycling scenario.
- Corrected typo in Power Ramp Timing table: 20ms instead of 25ms for PWR_2.

Rev. B – 04/2020

- Updated Table 2. Added lockout voltage levels for PWR_1, PWR_2 and PWR_3.
- Updated Voltage Supply Power-Off Sequencing.

Rev. A – 10/2019

- Initial release

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