Technical Note

Maximize SPI Flash Memory Design Flexibility With a Single Package

Introduction

This technical note discusses how a single 24-ball BGA package (6 x 8mm) can support a variety of flash products, enabling designers to offer a range of densities, features and performance levels simply by replacing the installed flash device. The included details enable designers to develop a common hardware platform that can support these products:

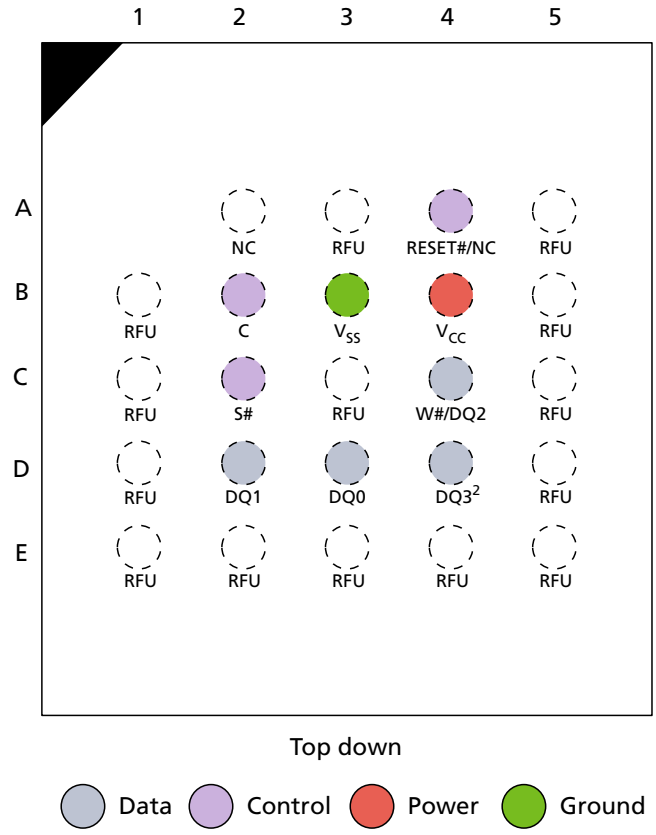
- **Quad SPI NOR flash**: Includes legacy modes of single- or dual-bit data interface.
- **Twin-quad SPI NOR flash**: Doubles the performance and density of a traditional quad SPI device.
- **Xccela™ flash**: An octal SPI NOR flash device that enables designers to achieve up to 400 MB/s.
- **Quad SPI NAND flash**: Similar to Quad SPI NOR flash from an interface-perspective; storage cell is NAND, which requires ECC (and which is on-die and built in these devices), and it comes in higher-density options. Applies to M7xA family.

This document shows the standard Quad SPI footprint and highlights the incremental changes to support all of the above devices. The end result is a single PCB footprint, capable of supporting all devices mentioned in this technical note.

Quad SPI NOR Flash

Traditional SPI flash devices can support read data widths of one, two or four bits with each clock. The figure below shows the basic footprint for a 6 x 8mm, 24-ball BGA package. The reserved for future use (RFU) balls on the perimeter of the package support forward migration to higher-performance devices. Other than the optional RESET#, all of the perimeter connections are available for expansion.

Figure 1: Quad SPI NOR Flash Package



Note:

1. See part number ordering information in the product data sheet for complete package names and details.
2. Depending on the selected device, DQ3 = DQ3/RESET or DQ3/HOLD. See part number ordering information in the product data sheet for details.

Table 1: Ball Descriptions

Name	Description
RESET# (optional)	Used to reset the device
Ground	Common reference for all signals

Table 1: Ball Descriptions (Continued)

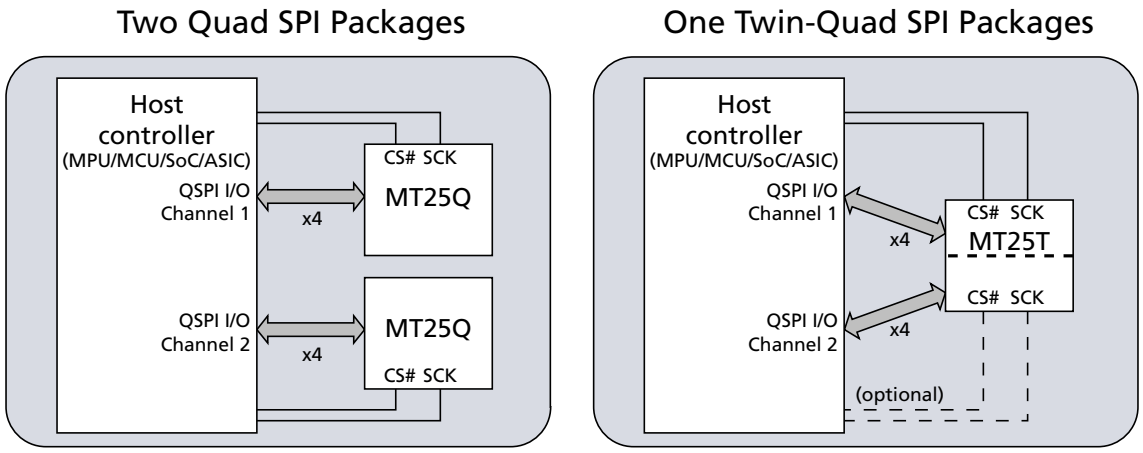
Name	Description
Power	Supports either 1.8V or 3.3V
Control	The SPI interface has clock (C) and chip select (S#). The SPI protocol basic serial interface sends commands, addresses and data serially to and from the device synchronously with the clock. Operations occur only when the specific device is selected (S# is LOW). This enables designs to support multiple devices using multiple chip selects, although only one device is enabled at a time.
Data	MT25Q SPI NOR flash devices range from 128Mb up to 2Gb. All of Micron's quad SPI NOR flash support the legacy data widths of x2 or x1. Typical performance of these devices is up to 166 MHz. Using the 166 MHz clock, STR example, and four data bit reads, a maximum of 83 MB/s performance can be achieved. If only two data bit reads are used, the maximum performance drops to 50% or 41.5 MB/s. If only a single data bit is used, the maximum read performance drops by another 50% or 21 MB/s. In addition to supporting the modes mentioned above, Micron's MT25Q quad SPI NOR flash devices feature the ability to support DTR, enabling data to be transferred on both the rising and falling edges of the clock, which is generally twice the throughput of STR.

Twin-Quad SPI NOR Flash

Twin-quad SPI devices save significant board space because only one 6 x 8mm package is required with the MT25T family versus two with the MT25Q family.

The figure below compares system implementations, with the left side showing an example using two discrete MT25Q devices and the right side showing an example using a single MT25T device.

Figure 2: Quad SPI vs. Twin-Quad SPI Comparison



Micron offers two versions of the MT25T device: a single-clock (C)/single-chip select (S#), and a dual-clock/dual-chip select. The dual-clock/dual-chip select device may be the most straightforward choice when interfacing with truly independent host controllers. An example of this is when the two host controllers are operating completely separately, and the host is a multicore processor with each of the clocks operating in separate clock domains with separate controllers connected or two separate host controllers. The dual-clock/dual-chip select device may also be used in place of the single-clock/single-chip select device by tying the two signals together in the PCB (which is done internally on the single-clock single/chip-select device).

Figure 3 shows the single-clock/single-chip select 24-ball BGA ball assignments and routing. For ease of identification, heavy, solid black circles are drawn around the connections that are new to this particular implementation. In this case, seven new connections have been added to support the twin-quad over the original quad SPI device.

Four of the new connections are additional DQ; the others are two additional ground connections and an additional power connection. The last three connections make the device more robust and improve power distribution.

Figure 3: MT25T – 24-Ball BGA Package, Single-Clock/Single-Chip Select

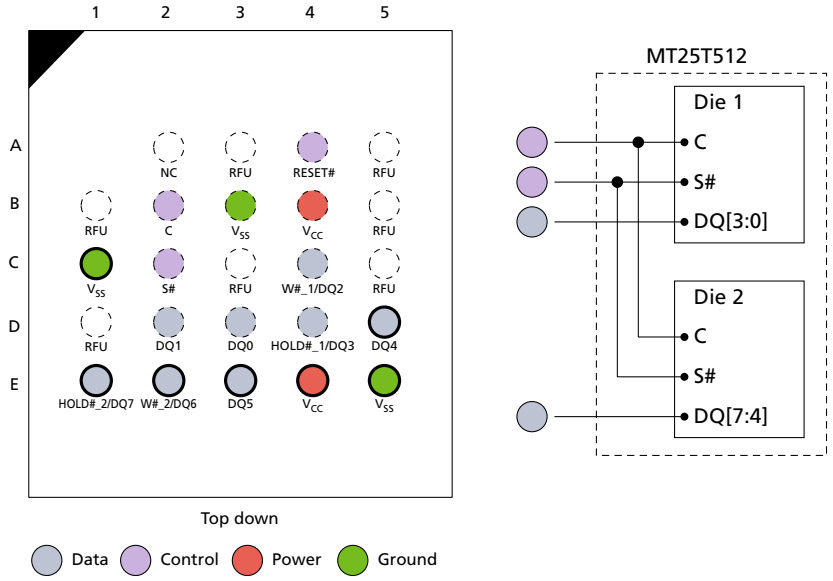
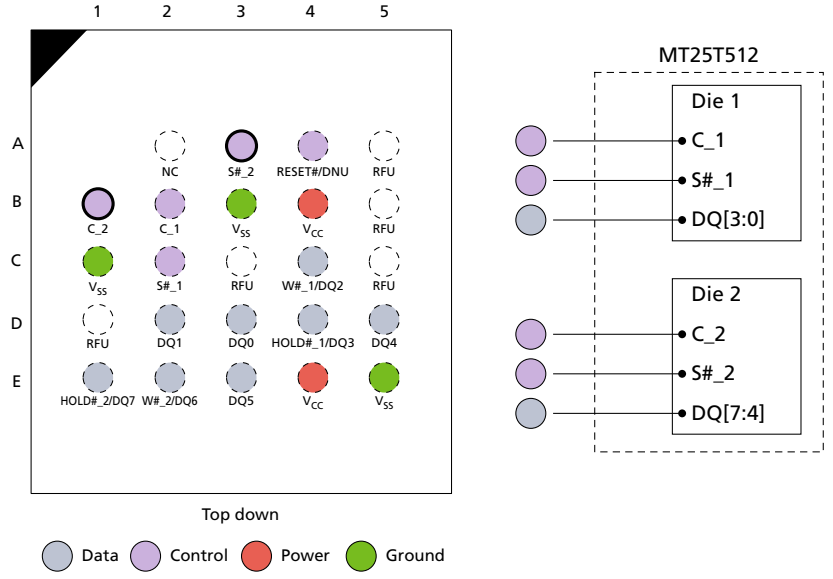


Figure 4 shows the two additional connections for the dual-clock/dual-chip select implementation.

Figure 4: MT25T – 24-Ball BGA Package, Dual-Clock/Dual-Chip Select



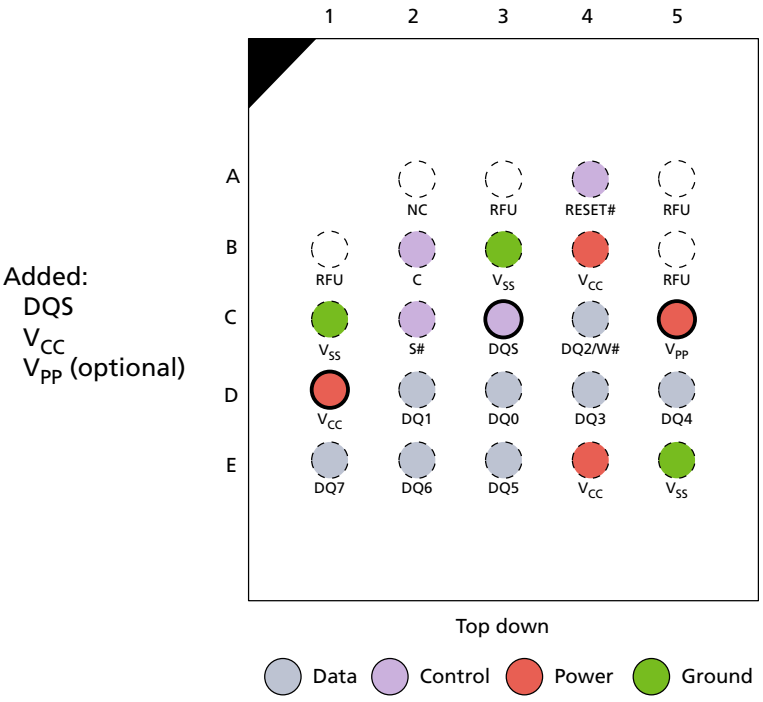
Xccela Flash (Octal SPI NOR Flash)

The MT35X Xccela flash is Micron's much-anticipated octal SPI device. The figure below shows the additional connections required to achieve the Xccela flash device's impressive performance of up to 400 MB/s. While data rates of 400 MB/s are not overly impressive by today's standards, achieving these data rates with only 11 signals (DQ[7:0], C, S# and DQS) is impressive.

The key to performance improvement is the addition of a single strobe signal, DQS, which makes it a source-synchronous interface. The addition of a DQS signal is similar to what was done in the evolution of mobile DRAM, from low-power single data rate (LPSDR) to low-power double data rate (LPDDR) devices. Like Xccela flash, LPDDR also supports a 200 MHz clock and 400 MT/s.

Adding DQS to the interface makes the design of the host controller more straight-forward by simplifying the controller's task of finding the data eye.

Figure 5: MT35X – 24-Ball BGA Package



Xccela Consortium

Micron understands the importance of having multiple vendors offer compatible products. To address this, Micron has formed the Xccela Consortium and has opened the specification up to other vendors. In addition, Micron is actively working with controller IP companies. This provides an alternative for companies that want to make use of Xccela flash components but might not have the resources to develop or modify their own controller.

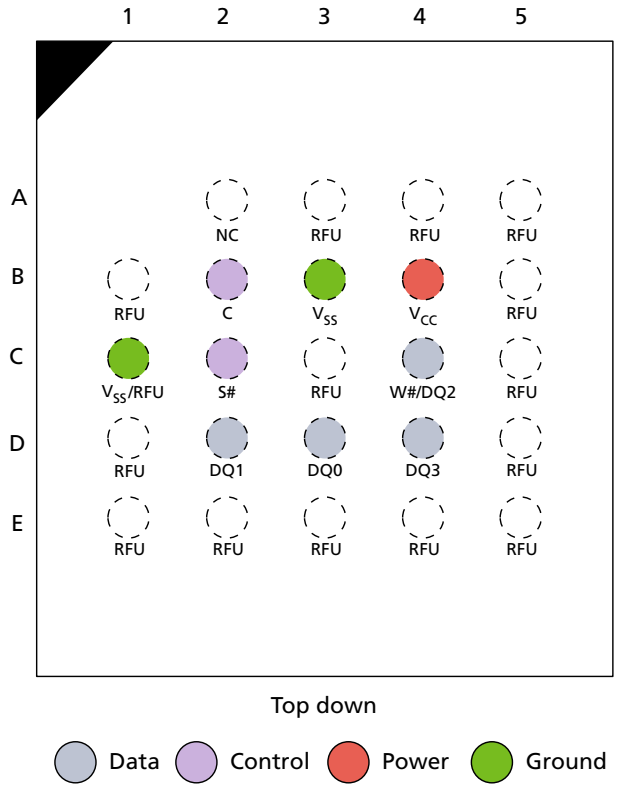
Quad SPI NAND Flash

Traditional SPI flash devices can support read data widths of one, two or four bits with each clock. The figure below shows the basic footprint for a 6 x 8mm, 24-ball BGA package. The reserved for future use (RFU) balls on the perimeter of the package support forward migration to higher-performance devices. With the exception of ball C1 (labeled as V_{SS} or NC), most of the perimeter connections are available for expansion, and are used in the Xccela footprint as shown in Figure 5.

Micron offers SPI NAND flash devices in 1Gb, 2Gb, 4Gb and 8Gb densities, making it ideal for embedded designs in need of low-cost boot or storage memory. On-die ECC means that the SPI NAND can often be supported with a standard SPI controller.

Challenges for interfacing with SPI NAND often have to do with a flexible controller; with this device, the SPI controller must have the ability to support NAND commands as well as up to 5 bytes of NAND address. It must also accommodate the page size. Additionally, depending on the application, flash file system software may be required.

Figure 6: Quad SPI NAND Flash Package

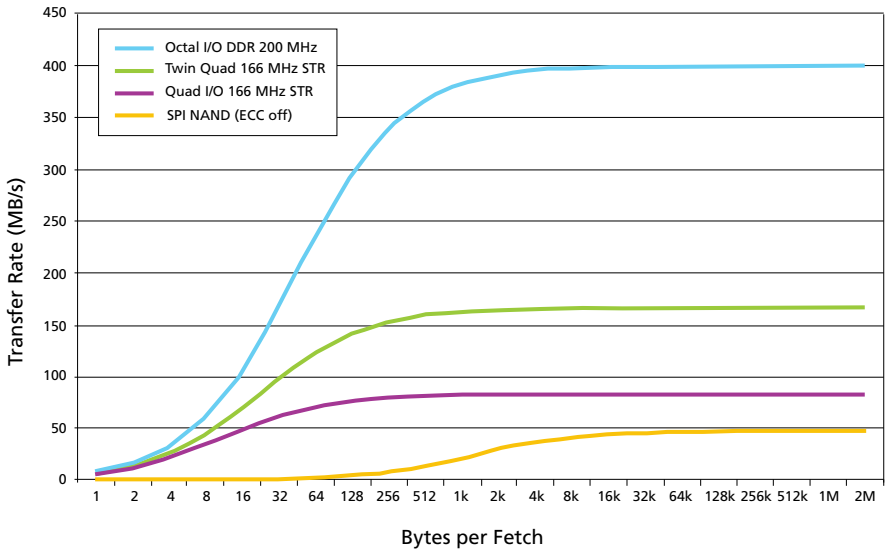


Performance

The figure below charts the performance levels of all of the SPI flash devices discussed in this technical note. Because performance is based on serial interfaces, the performance for smaller payloads is a fraction of the performance for larger payloads. This is because of the overhead that is required to input a command and three or four bytes of address for every payload. Note that random access for data sizes under eight bytes can result in unimpressive performance. But for payloads of 32 bytes or more, all of the devices discussed start to break the 50 MB/s floor, which makes implementing a cache or a buffering scheme critical to improve performance.

- **Quad SPI NOR flash** achieves a maximum of ~90 MB/s. As shown below, these devices use a total of only six signals to achieve ~90 MB/s.
- **Twin-quad SPI NOR flash** achieves ~180 MB/s or double that of the single quad SPI device. As shown below, as few as four additional signals (10 signals total) would be required to achieve~180 MB/s.
- **Xccela flash** achieves ~400 MB/s, or over double that of the twin-quad SPI device, by adding only a single DQS signal. This type of performance has generated interest in using Xccela flash as a low-pin count, execute-in-place (XIP) memory solution. Further improving on the XIP concept, Xccela flash can be used as a high-speed, nonvolatile memory that interfaces directly with the cache and memory subsystems. Assuming a 32-byte cache line, a cache line fill can be completed in about 160ns. If the cache line was 64 bytes, a line fill could be accomplished in about 240ns.
- **Quad SPI NAND flash** has a maximum read performance of 48 MB/s and supports clock frequencies of up to 133 MHz. The latest 4Gb and 8Gb devices offer a continuous read feature that is attractive for applications requiring large amounts of data to be read (like initial boot or downloading logged data). For flash densities exceeding the NOR sweet spot of under 512Mb, Micron's SPI NAND can offer lower cost, higher density solutions.

Figure 7: Random Read Access Performance vs. Data Size



Conclusion

Micron's quad SPI NOR, twin-quad SPI NOR, Xccela (octal SPI) NOR and Quad SPI NAND flash devices are offered in a single 24-ball BGA (6 x 8mm) package, which gives designers a variety of technologies, densities, features and performance options in one PCB footprint — making migration between these products relatively easy.

Figure 5 shows the superset ballout that enables your PCB to support all of the devices mentioned in this tech note.

Micron has a full line of DRAM and flash devices that are qualified to industrial and automotive temperature and quality specifications. Contact Micron for additional details on these or any other memory needs.

Revision History

Rev. C – 9/17

- Added quad SPI NAND.

Rev. B – 2/17

- Updated XTRMFlash product name to Xccela flash.

Rev. A – 10/15

- Initial release

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