Technical Note

Reset Configurations for MT25Q, MT25T, and N25Q Flash Memory Devices

Introduction

This technical note provides a list of the reset configurations available for the MT25Q, MT25T, and N25Q family of Flash memory devices:

- Hardware reset
- Software reset
- XIP reset
- Protocol reset

For detailed information on the RESET operation and each reset configuration, see the MT25Q, MT25T, and N25Q discrete data sheets.

Operating Conditions Requiring a Reset

A reset is required after a power loss or when the device and controller are out of synchronization.

Reset When Device and Controller Are Not Synchronized

If at any time during the life of the application the system controller is reset without the device being reset, the controller and device can become out of synchronization. If this occurs, the two possible solutions are to perform a hardware reset or a software reset.

After a hardware or software RESET operation, the following can be expected to occur:

- The device is set to the power-up state
- All volatile registers are reset
- Nonvolatile registers are not affected by reset

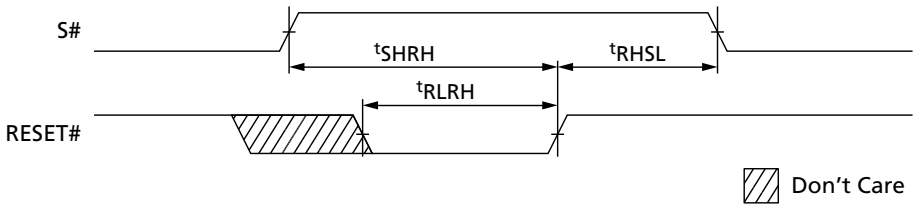
Hardware Reset

To perform a hardware reset, the controller resets the device to power-on reset if the device has reset functionality. (Reset functionality is determined by part number. See the component data sheet for details.) In this case, it is necessary to recover memory sector under erase or programming if the device was busy during the CPU reset.

Hardware reset is determined by placing a specific pin LOW:

- For devices with part numbers MT25Qxxxxxxx8Exx-xxx and MT25Txxxxxxx8Exx-xxx: The HOLD# and RESET# pins are separated. To perform a hardware reset, assert RESET# pin LOW (for SO16W and T-PBGA packages only). In this case, the reset pin is independent by the use of protocol.
- For devices with part number N25QXXXA3xxx: The reset pin is placed LOW. The pin is the same as DQ3. If the device is operating in quad mode, the reset pin is active only if S# is HIGH.
- For devices with part number N25Q256A8xxx or N25Q512A8xxx: The hold and reset pins are separated. To perform a hardware reset, hold RESET# LOW (for SO16W and T-PBGA packages only). In this case, the reset pin is independent by the use of protocol reset.

Figure 1: Hardware Reset Timing



Software Reset

Software reset depends on dedicated commands RESET ENABLE (66h) and RESET MEMORY (99h). The commands must be issued in accordance with the protocol in use.

Figure 2: Software Reset Timing

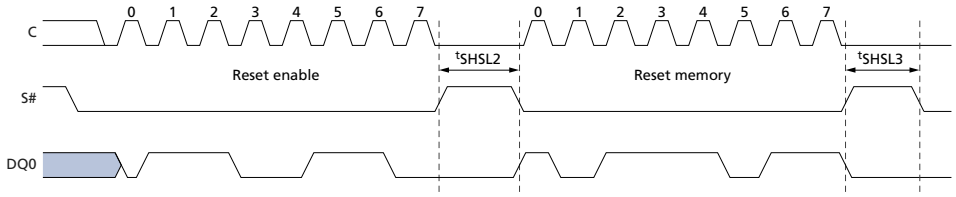
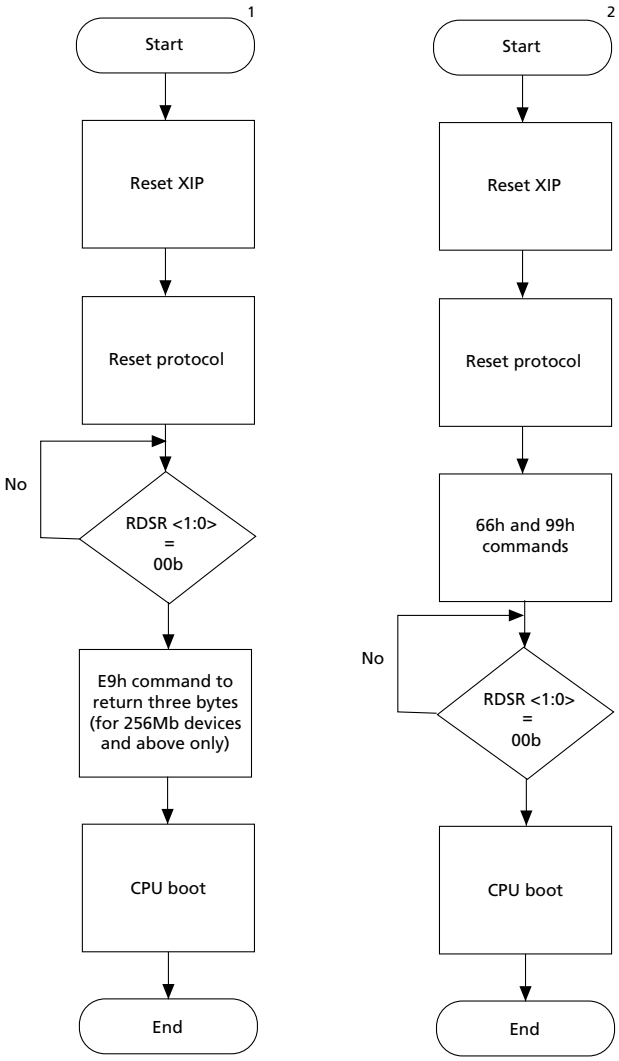


Figure 3: Software Reset Flowchart



Notes:
1. Device does not support software reset functionality.
2. Device supports software reset functionality (it is necessary to recover memory sector under erase or programming if the device was busy during CPU reset).

Reset After a Power Loss

If a power loss occurs during a WRITE NONVOLATILE CONFIGURATION REGISTER command, the device may start in an undetermined state (XIP mode or unnecessary protocol) at the next power-on. If this occurs, until the next power-up, a recovery sequence must be issued to reset the device to a fixed state (extended SPI protocol without XIP). After the recovery sequence, run the WRITE NONVOLATILE CONFIGURATION REGISTER command again.

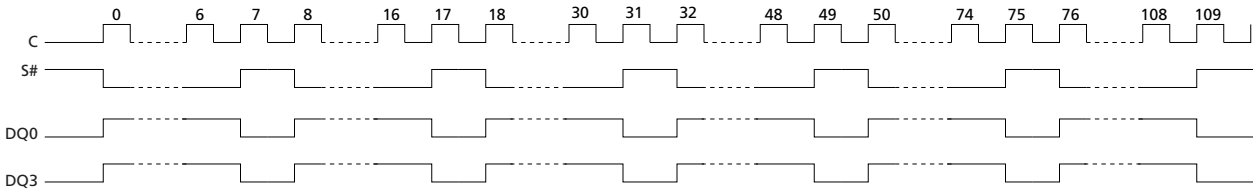
The recovery sequence consists of two steps that must be performed in the following order:

1. XIP reset
2. Protocol reset

During the entire sequence, ^{t}SHSL2 must be at least 50ns.

XIP Reset

Figure 4: Reset sequence for all XIP configurations—Quad I/O, Dual I/O, Fast Read



Note: 1. For applications using two or more dummy clock cycles, the first sequence can also be executed with eight clocks.

Protocol Reset

Figure 5: Exit from Dual or Quad SPI Protocol Using FFh Sequence

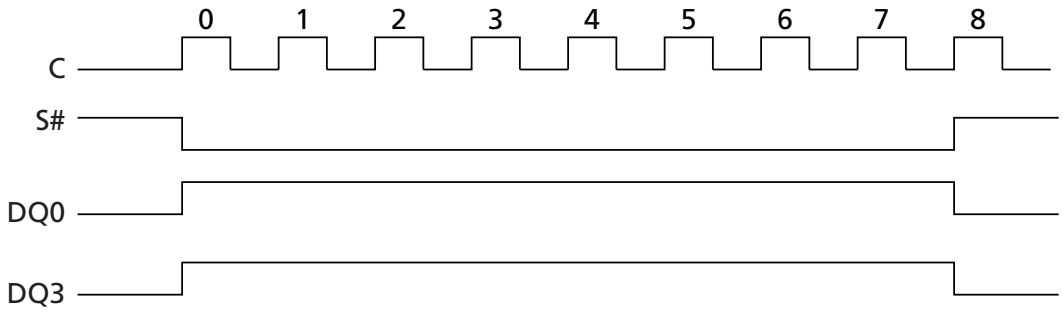
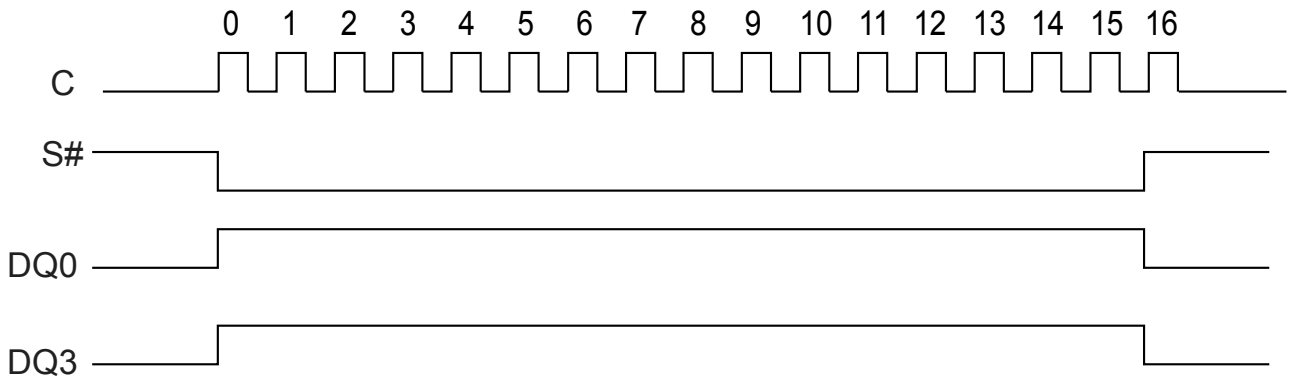


Figure 6: Exit from DTR Protocol



Notes:
1. DQ0 should be driven to 1 on both edges of clock for 16 cycles with S# LOW.
2. The Exit from DTR Protocol sequence is mandatory only for MT25Q and MT25T and is not necessary for N25Q.

Revision History

Rev. E – 03/18

- Added figure for Exit from DTR protocol

Rev. D – 01/17

- Added MT25Q and MT25T
- Removed N25W

Rev. C – 09/13

- Updated Hardware Reset description

Rev. B – 06/13

- Added N25W to titles and introduction
- Added note under XIP Reset figure

Rev. A – 05/13

- Initial Release

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