Introduction

Quad-level cell (QLC) NAND is the next significant step in NAND device offerings, building on the previous triple-level cell (TLC) NAND and multi-level cell (MLC) NAND iterations.

QLC NAND offers three primary benefits over TLC NAND:

• Lower cost per NAND storage bit
• Smaller physical footprint for same density storage
• Ability to lower total cost of ownership (TCO) of a system

These benefits potentially make QLC NAND a viable memory storage option for applications in which previous TLC NAND devices were not a good fit.

Although QLC NAND benefits are attractive, some key items should be considered to fully determine if QLC NAND is suitable for an application and meets needed system requirements.

This paper outlines some of the key considerations to help determine if QLC NAND is suitable for use in an application.
Benefits of QLC NAND

Before explaining some of the key considerations with transitioning to QLC NAND, it is important to briefly expand on the three primary benefits of QLC NAND as compared to TLC NAND.

Lower NAND Storage Bit Costs

QLC NAND technology stores more bits per NAND cell compared to TLC NAND, resulting in a trend that will push the cost per NAND bit lower for QLC versus TLC NAND.

This trend has two primary benefits: (1) Systems for which previous NAND technologies were considered too expensive may now have an option to use QLC NAND, and (2) For systems that already use TLC NAND, a transition to QLC NAND could improve the cost structure of those systems and/or offer an opportunity to increase storage density offerings because QLC NAND provides 33% more bit storage than TLC NAND.

Smaller Physical Footprint for the Same Amount of Storage

Because QLC NAND provides more storage per NAND cell as compared to TLC NAND, QLC NAND can more easily offer higher storage density, which can translate to a lower number of QLC devices needed to reach the same storage density as achieved with TLC NAND. Additionally, fewer QLC NAND devices take up less physical space in a system—space that can be used for either reuse or possible physical size reduction (for example, reducing the size of the PCB).

<table>
<thead>
<tr>
<th>Total NAND System Density</th>
<th>NAND Technology</th>
<th>Number of NAND LUN/Die</th>
<th>Number of QLC LUN/Die Reduction vs. TLC</th>
</tr>
</thead>
<tbody>
<tr>
<td>2TB</td>
<td>QLC — 1Tb LUN-die</td>
<td>16</td>
<td>50%</td>
</tr>
<tr>
<td>2TB</td>
<td>TLC — 512Gb LUN die</td>
<td>32</td>
<td>-</td>
</tr>
</tbody>
</table>

Alternatively, if a system does not reduce the number of NAND LUN/die from a TLC NAND solution to a QLC NAND solution, there is a potential to increase storage density without a change in form factor or physical footprint of the system.
Lower Total Cost of Ownership

Cost plays a significant role in the success of a product, and methods to reduce a system’s total cost of ownership (TCO) while still meeting system requirements is beneficial. Due to the lower cost per bit of QLC NAND, the NAND storage portion of a system’s bill of materials (BOM) can be reduced for those systems transitioning from higher cost-per-bit NAND storage (TLC NAND) to QLC NAND.

In addition to reducing NAND storage cost, there is a potential secondary cost reduction benefit: power savings. NAND devices, whether in active use or not, consume power which becomes part of the system’s total power budget. A lower number of QLC NAND devices consumes less power for a given density versus TLC NAND devices for the same density.

Reduction in the number of NAND devices reduces the total power needed by the system, which can translate to additional cost savings, including:

• Reduced costs of power expenses for system operation
• Reduced thermal considerations needed for the system by less heat generation
• Smaller delivery power generation ICs for the system
• Any combination of the above
QLC NAND Considerations

With the primary benefits of QLC NAND explained, it is important to note the considerations that need to be understood before transitioning from TLC NAND to QLC NAND.

Endurance

As those familiar with NAND technology and number of bits per NAND cell are aware, endurance (or program/erase cycles) generally decreases when the number of bits per NAND cell increases. QLC NAND is no exception, and because of this, the endurance of QLC NAND is less than that of TLC NAND.

Compared to a similar TLC NAND device type, QLC NAND has approximately 75% the specified endurance of TLC NAND.

This reduction in endurance is a characteristic that needs to be accounted for by a system considering a transition from TLC NAND to QLC NAND. As a comparison point, for TLC and QLC NAND devices with the same density, a reduction in QLC endurance translates relative to TLC endurance, which results in a reduction in total bytes written (TBW).

A subset of the TBW topic, write amplification operations of a system to NAND storage, is also an element that must be reviewed and vetted in a transition to QLC NAND usage. Because endurance for QLC NAND is less than TLC NAND, there is less NAND endurance budget for QLC NAND for use in write amplification actions.

Figure 2: Relative Endurance

Read and Program Performance

Another consideration is array read and program performance on QLC NAND and how it affects a system’s performance. At the QLC NAND array level of operations, both read and program operations are significantly slower than TLC NAND.

Compared to maximum TLC NAND read and program array events, maximum QLC read events can be approximately 2X longer and maximum QLC program events can be approximately 3.5X longer. These are significant increases in busy time events for QLC operations.
Because QLC NAND array read and program events can be significantly slower than that of TLC NAND does not mean a system transitioning to QLC NAND from TLC NAND can’t be successful. Although QLC NAND has slower performance for read and program operations, it is possible for QLC NAND to be successful in a system that used TLC NAND because:

- TLC NAND provided greater read/program performance than the system required, and QLC NAND can meet those system read/program requirements.
- Non-NAND system bottlenecks/operations mask (or limit) the impact of slower QLC NAND array read/program performance.
- Improved host system utilization of QLC NAND read/program operations to reduce or close the gap of decreased QLC NAND array performance that may not have been optimized with TLC NAND.
- Improved use of NAND SLC caching schemes to assist in making up for the reduced QLC operation performance.

To best determine if QLC array read and program performance can meet your system requirements, calculate QLC array read and program performance for your application taking into consideration the above bullet points.

**Maximum QLC Array Program Time**

Although not applicable for every system, maximum array program time is a consideration both for system maximum program latency requirements and potential backup power supply needs to the NAND in the case of power loss during a NAND array program operation.

The maximum array program time for QLC NAND is approximately 3.5X longer than that of TLC NAND. A system’s quality of service (QoS) requirements, abilities to interrupt NAND array operations, and the occurrence rate of maximum array program time events need to be understood to determine if the maximum array program time of QLC NAND will meet system requirements.

Related to maximum array program time, a system that has backup power (for example, bulk capacitance storage tied to NAND) to successfully complete the longest NAND array program operation in the event of a power loss may need to review array program time design requirements. As maximum QLC NAND array program times are longer
than those for TLC NAND, a host system that designed-in backup power to cover TLC NAND program operation should consider the following:

- An increase to the backup power design to accommodate longer maximum array QLC NAND program time.
- System modifications (for example, less NAND operations in flight, change to workload conditions, etc.) that a current backup power design would be sufficient to cover without change.
- System modifications to utilize more power-efficient NAND operations (for example, use of power-efficient program operations, use of NAND power savings features, etc.) to reduce NAND total power consumption.

**Error Rates and Trigger Rates**

One of QLC NAND’s most attractive benefits—33% more bit storage per NAND cell versus TLC NAND—is achieved by doubling the number of logical states stored per NAND cell.

**Figure 4: NAND Logical States — TLC vs. QLC NAND**

![Illustration of NAND logical states — TLC vs. QLC](image)

However, by doubling the logical states per NAND cell, there is an increased chance of shifts in those states, resulting in an increase in raw bit error rate (RBER), error trigger rates for correction routines, or a combination thereof.

Because NAND error and trigger rates are influenced by a system's workload, system proactive/reactive error management routines, and operational environment, each system must perform analysis as to how QLC NAND error characteristics will manifest to understand and weigh their significance.

An increase of these characteristics in QLC NAND does not mean a system cannot migrate to QLC NAND from TLC NAND. Increased error rates and trigger rates related to error correction are characteristics a system considering migrating to QLC NAND needs to fully understand to determine if QLC NAND meets system requirements. Some example methods for determining if QLC error rates and trigger rates are appropriate for your system are:

- Review system testing and characterization with QLC NAND within all system use conditions with sufficient volume of QLC NAND.
• Review system workload profiles (for example, mix of read/program operations) and how they relate to NAND error management.
• Analyze and optimize system proactive and reactive error management routines as they relate to QLC NAND.
• Consider other conditions as determined by the system.

Conclusion

QLC NAND represents the next transition milestone in NAND device offerings, bringing with it significant benefits for those systems able to capitalize on QLC NAND’s lower cost per storage bit, reduced physical footprint, and lower TCO characteristics.

The benefits of QLC NAND do not come without considerations that need to be properly examined by a system considering transitioning to QLC NAND. Properly vetted, elements of each item discussed in this document can be minimized or mitigated by a host system with proper action.

QLC NAND’s potential benefits make it an attractive transition consideration for most systems using TLC NAND. QLC NAND can not only benefit systems that already use NAND technology, but it can also provide the opportunity to expand to systems that have not yet utilized NAND technology as a viable storage solution.
Revision History

Rev. A – 9/19

- Initial release