Technical Note

RLDRAM 3 Design Guide

Introduction

RLDRAM 3 is a high-performance memory that effectively meets the needs of systems requiring high bandwidth and low latency. This design guide contains practical recommendations that enable board designers to develop a high-performance memory subsystem while ensuring stability for long-term reliable operation of the device.

The first part of this guide contains recommendations for board-level hardware design. The intent is that board designers will use these recommendations to develop a set of general rules and then, through simulation, verify the functionality and stability of the RLDRAM 3 sub-system. The remainder of the guide details the RLDRAM 3 timing specifications that are relevant for designers to develop an accurate data capture timing budget. Properly accounting for the RLDRAM 3 portion of the timing budget enables designers to take full advantage of the margin remaining for controller and board-level effects.

Definitions

Throughout this guide, V_{SS} and V_{SSQ} are assumed to be identical. V_{SSQ}, the I/O ground voltage, is separated from V_{SS} on the RLDRAM 3 for noise immunity; however, each set of balls are typically referenced to the same board plane. For the sake of simplicity, only V_{SS} is referenced in the remainder of this document.

References to CK, DQ, DK, QK, DM, and QVLD are to be interpreted as each group collectively, unless specifically stated otherwise. This includes true and complement signals of differential signals.

Board Design Recommendations

RLDRAM 3 Power Supplies

RLDRAM 3 has four separate voltage inputs as show in Table 1.

Table 1: RLDRAM 3 Voltage Inputs

Parameter	Purpose	Minimum	Nominal	Maximum	Units
V_{DD}	DRAM core	1.28	1.35	1.42	V
V_{DDQ}	I/O	1.14	1.2	1.26	V
V_{EXT}	Array-based row drivers	2.38	2.5	2.63	V
V_{REF}	Differential input buffer reference	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V

If the command and address bus are externally terminated, an additional voltage source, V_{TT}, would also be required at the RLDRAM 3 interface. The value of V_{TT} would track V_{REF}.

V_{REF} Recommendations

V_{REF} requires a voltage of $V_{DDQ}/2$ with a ±1% DC tolerance. Because V_{REF} is an input to a differential pair, common-source amplifier, there is no significant current draw. V_{REF} can be generated using a simple resistor divider with 1% or better accuracy. V_{REF} must track $V_{DDQ}/2$ over voltage, temperature, and noise. Up to ±2% DC peak-to-peak noise and ±2% AC peak-to-peak noise is allowed on the V_{REF} supply. DC peak-to-peak noise is defined as values less than 20 MHz. Thus, from $V_{DDQ}/2$, V_{REF} is allowed ±2% $V_{DDQ}/2$ for DC error and an additional ±2% $V_{DDQ}/2$ for AC noise. This measurement should be taken at the nearest V_{REF} bypass capacitor. To ensure a robust RLDRAM 3 design, it is imperative that V_{REF} noise, including crosstalk, is kept to a minimum.

When designing for V_{REF}, consider the following:

- Place a 0.1uF decoupling capacitor as close as possible to each of the two V_{REF} balls on the RLDRAM 3 package. Place this capacitor between V_{REF} and whichever plane the input signals are referenced to. The V_{REF} trace between the decoupling capacitor and the RLDRAM 3 ball should maintain a consistent reference for lowest inductance.
- Design traces as short and wide as possible between the decoupling capacitor and the V_{REF} ball at the RLDRAM 3. Doing this provides the lowest possible inductance and subsequently minimizes noise.
- Maintain at least a 15–25 mil clearance from V_{REF} to adjacent traces to reduce coupling.

V_{TT} Recommendations

This section is relevant only if the address and command bus is terminated (see "Command and Address Signals" on page 7 for recommendations).

Note that V_{TT} is not an input to the RLDRAM 3 device. V_{TT} should have a nominal value of $V_{DDQ}/2$ and also track variations in V_{REF} over voltage, temperature, and noise. V_{TT} must be generated by a regulator that is able to sink and source reasonable amounts of current while still maintaining tight voltage regulation.

Micron offers the following recommendations for decoupling the V_{TT} plane:

- Follow the regulator vendor's recommendations for capacitor placement and values to ensure stability of the regulator.
- Place a 1.0uF decoupling capacitor for every four signals terminated to V_{TT}. Adjacent groups comprised of four signals terminated to V_{TT} (for example, resistor packs) can share a decoupling capacitor. If the regulator is within 1 inch of these capacitors, they may be considered as part of the decoupling recommended by the regulator vendor.
- Place the decoupling capacitor between V_{TT} and whichever plane the input signals are referenced to. Decoupling to both V_{DDQ} and V_{SS} is not a requirement but will not have any negative effects on performance.
- Place the decoupling capacitor as close as possible to the terminating resistors to minimize inductance.
- V_{TT} island surface trace length should be at least 150 mil, but 250 mil is preferred.

Decoupling V_{DD}, V_{DDQ}, and V_{EXT}

As on-board power supplies are typically switching regulators that include a large amount of bulk capacitance, additional low-frequency decoupling typically isn't required. A case in which it could be warranted is if the supply is a long distance from the RLDRAM 3 device. The board designer can perform a first-order estimate what the inductance of a plane is with the following equation:

$$L = 31.9 \times D \times H/W \quad \text{(EQ 1)}$$

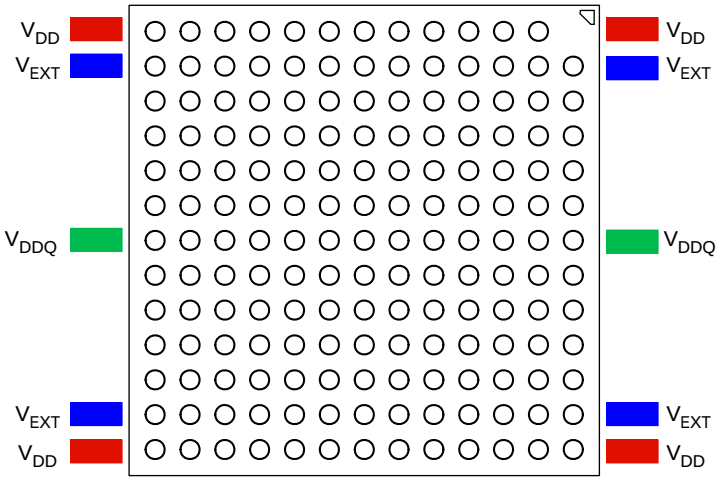
- L = inductance in nH
- D = length of plane in inches
- H = separation of power and ground planes in inches
- W = width of plane in inches

Note that Equation 1 is a simple approximation; simulation is recommended to achieve a more accurate assessment.

Additional local bulk capacitance may be required if the power distribution plane inductance is large enough to cause unacceptable droops in the supply voltages. Refer to Technical Note TN-00-06: Bypass Capacitor Selection for tips on choosing appropriately sized bulk capacitors.

To decouple higher frequency power-supply noise, Micron recommends placing a 0.2uF to 1uF capacitor at each corner of the RLDRAM 3 device. Placing the caps in the suggested locations minimizes the distance to the die and the associated inductance.

Figure 1: Decoupling Capacitors for V_{DD}, V_{EXT} and V_{DDQ}



Board Layout and Routing Design Guidelines

To help ensure good signaling, consider the following general board design guidelines:

- Avoid crossing splits (return path discontinuities) in reference planes.
- Minimize intersymbol interference (ISI) by keeping impedances matched.
- Minimize crosstalk by isolating sensitive bits, such as strobes. See "Interpair and Intrapair Spacing" on page 4 for more details.
- Maintain references for a given signal, whether it is V_{DD}, V_{DDQ}, or V_{SS}.

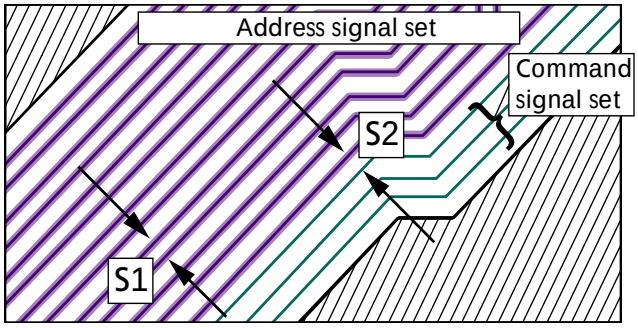
Interpair and Intrapair Spacing

Two types of trace spacing affects signal integrity: interpair spacing and intrapair spacing.

Interpair spacing (S1) is the distance between two adjacent traces within a related set of signals with similar or equivalent functionality. The command signals, clocks, address bus, data bus, and strobes are all unique signal sets.

Intrapair spacing (S2) is the distance between the two outermost signals of different signal sets. For example, if the command signal set is routed adjacent to the address signal set, intrapair spacing is the distance between the two individual signals from command and address sets that are closest together.

Figure 2: Interpair and Intrapair Spacing



Many variables other than spacing can cause crosstalk in a board layout, such stripline vs. microstrip routing, slew rates, and termination scheme. To take into account other system variables that impact signal integrity, the spacing recommendations in Table 2 on page 4 should be used as a starting reference point before fine-tuning with simulation.

Table 2: Spacing Recommendations

Signal Set	Signals	Spacing Type	Spacing	Units
Data/data strobes	DQ to DQ	S1	8	mil
	DQ to DK	S2	8	mil
	DQ to QK	S2	8	mil
	QK to DK	S2	8	mil
	DQ to DM	S2	8	mil
Address	Adjacent address lines	S1	6	mil
	Address lines	S2	6	mil
Command	CS#, WE#, REF#	S1	6	mil
Clock	CK to CK#	S1	4	mil
	Differential pair (CK, CK#) to any other signal	S2	8	mil

Notes: 1. Minimum trace width recommendation is 4 mil for all signals.

Miscellaneous Routing Recommendations

Differences in trace length within a group of signals or between groups can cause a significant amount of skew. For example, a 400 mil trace length difference between signals within a signal group equates to approximately 72ps of skew (assuming propaga-

tion delay of 180 ps/in of an inner layer FR4 PCB trace). Development of a data capture timing budget gives the board designer the understanding of how much board level skew can be tolerated without causing bus contention or violating any AC timing parameters.

All signal groups must be properly referenced to a solid V_{SS} or power plane (V_{DD} or V_{DDQ}) to provide a low impedance return path. Special attention should be paid to the CK pair, input and output data strobes, and DQ and DM signals because they operate at twice the speed of the other signal groups. These signals are best referenced to V_{SS}. If a V_{SS} layer is not easily accessible, address and command signals can reference a V_{DD} layer.

Differential Clock Routing

All differential signals (CK, DK, and QK) should be routed as differential pairs. Differentially routed signals may have different propagation times than single-ended signals. Board designers should keep the following in mind:

- Nets routed as stripline (internal) will have matched propagation whether single-ended or differential.
- Single-ended nets and differential nets on outer layers will have different propagation times from each other.
- Nets routed on outer layers will have a different propagation time from nets on inner layers.
- It is preferable to route differential clock pairs on the same layer.

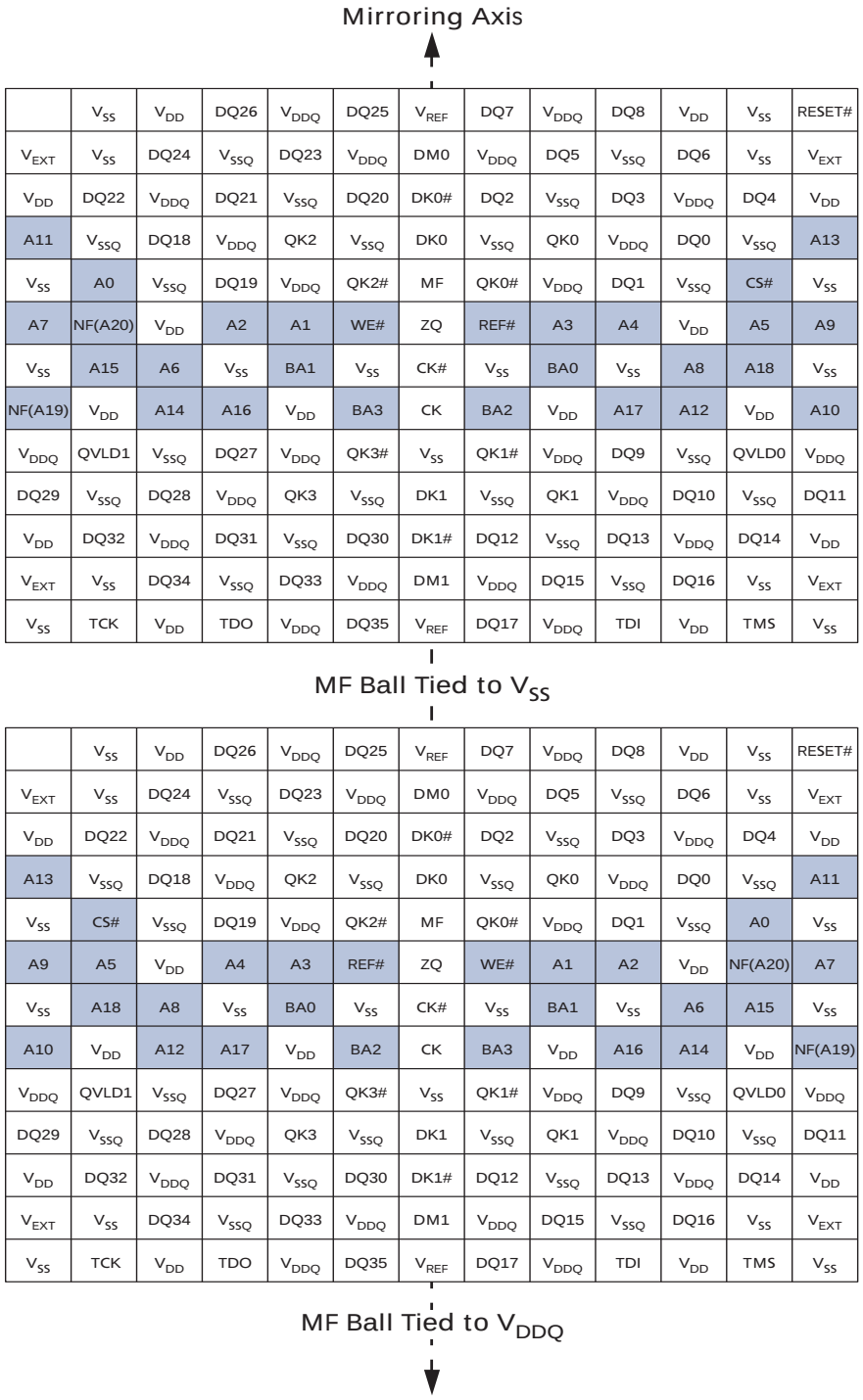
If a board's routing includes signals on both inner and outer layers or if there are differential and single-ended nets on the outer layers, simulation should be performed to determined what is required to match propagation delays between relevant signals. Differences in propagation delay can be as high as 20%.

Clamshell Topologies

RLDRAM 3 enables simplified routing of a clamshell topology (two devices mounted in alignment on opposite sides of a PCB) with its mirror function (MF) ball. The MF ball is a DC input signal used to enable a mirrored ballout of the command and address signals. If the ball is tied to V_{SS}, the address and command balls are in their true layout. If it is tied to V_{DDQ}, they are mirrored across the central y-axis. See Figure 3 on page 6 for the ball assignment in each state. MF must be tied HIGH or LOW and cannot be left floating.

The mirror function used in a clamshell topology allows the address and command signals to be shared between the two devices simply through a via across the PCB. This alleviates cumbersome routing schemes and complications of the initialization routine as a result of sharing different address signals.

Figure 3: Ball Assignments with Mirror Function in Opposite States



	V_{SS}	V_{DD}	DQ26	V_{DDQ}	DQ25	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
V_{EXT}	V_{SS}	DQ24	V_{SSQ}	DQ23	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
V_{DD}	DQ22	V_{DDQ}	DQ21	V_{SSQ}	DQ20	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
A11	V_{SSQ}	DQ18	V_{DDQ}	QK2	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A13
V_{SS}	A0	V_{SSQ}	DQ19	V_{DDQ}	QK2#	MF	QK0#	V_{DDQ}	DQ1	V_{SSQ}	CS#	V_{SS}
A7	NF(A20)	V_{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V_{DD}	A5	A9
V_{SS}	A15	A6	V_{SS}	BA1	V_{SS}	CK#	V_{SS}	BA0	V_{SS}	A8	A18	V_{SS}
NF(A19)	V_{DD}	A14	A16	V_{DD}	BA3	CK	BA2	V_{DD}	A17	A12	V_{DD}	A10
V_{DDQ}	QVLD1	V_{SSQ}	DQ27	V_{DDQ}	QK3#	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD0	V_{DDQ}
DQ29	V_{SSQ}	DQ28	V_{DDQ}	QK3	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
V_{DD}	DQ32	V_{DDQ}	DQ31	V_{SSQ}	DQ30	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
V_{EXT}	V_{SS}	DQ34	V_{SSQ}	DQ33	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	DQ35	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

	V_{SS}	V_{DD}	DQ26	V_{DDQ}	DQ25	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
V_{EXT}	V_{SS}	DQ24	V_{SSQ}	DQ23	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
V_{DD}	DQ22	V_{DDQ}	DQ21	V_{SSQ}	DQ20	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
A13	V_{SSQ}	DQ18	V_{DDQ}	QK2	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A11
V_{SS}	CS#	V_{SSQ}	DQ19	V_{DDQ}	QK2#	MF	QK0#	V_{DDQ}	DQ1	V_{SSQ}	A0	V_{SS}
A9	A5	V_{DD}	A4	A3	REF#	ZQ	WE#	A1	A2	V_{DD}	NF(A20)	A7
V_{SS}	A18	A8	V_{SS}	BA0	V_{SS}	CK#	V_{SS}	BA1	V_{SS}	A6	A15	V_{SS}
A10	V_{DD}	A12	A17	V_{DD}	BA2	CK	BA3	V_{DD}	A16	A14	V_{DD}	NF(A19)
V_{DDQ}	QVLD1	V_{SSQ}	DQ27	V_{DDQ}	QK3#	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD0	V_{DDQ}
DQ29	V_{SSQ}	DQ28	V_{DDQ}	QK3	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
V_{DD}	DQ32	V_{DDQ}	DQ31	V_{SSQ}	DQ30	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
V_{EXT}	V_{SS}	DQ34	V_{SSQ}	DQ33	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	DQ35	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

Notes: 1. Shaded cells are the balls that are mirrored.

Signaling Specifications and Considerations

The RLDRAM 3 signaling specifications are very similar to other well-known standards, such as SSTL_18 and HSTL_15. With the exception of the RESET# and MF signals, the input buffers of an RLDRAM 3 are differential receivers that operate at 1.2V. For the single-ended inputs (such as command, address, DQ), one leg of the receiver is tied to V_{REF} The fast-switching requirements of the RLDRAM 3 underscore the need to supply a clean V_{REF} input as discussed earlier in this guide. The input clocks (CK and DK) are true differential inputs that rely on complementary inputs to operate. The output data strobes, QK and QK#, are single-ended drivers that are designed to be 180' out of phase.

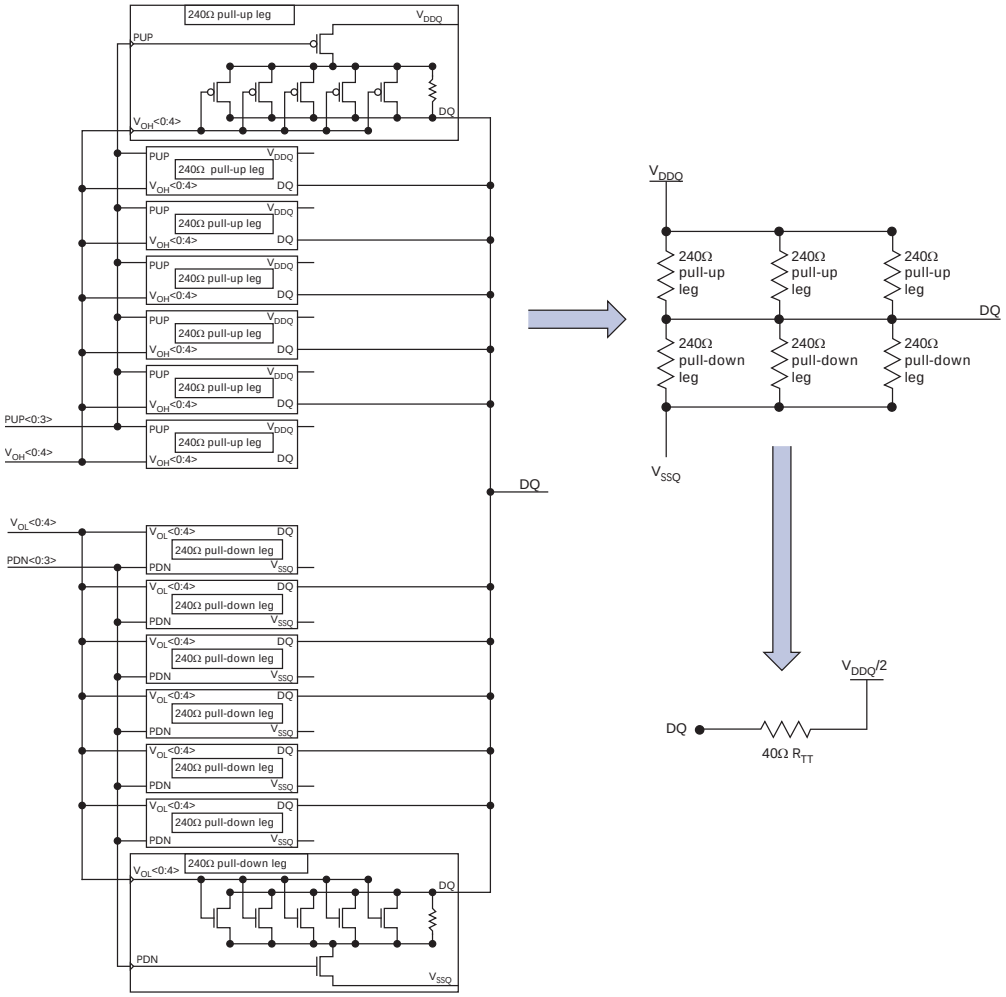
Command and Address Signals

All command and address signals are single-ended and are latched on the rising edge of CK. Because they operate at half the operating frequency of CK, data strobes, DQ, and DM signals, it is possible that adequate signal integrity be met without requiring end termination. Factors, such as length of signals, topology, operating frequency, routing trace type (microstrip or stripline), all contribute to signal integrity and whether end termination is required on these signals. Micron's analysis of a point-to-point topology shows command and address signals routed with stripline require end termination when operating at 933 MHz on traces that are two inches or longer. Routing done with microstrip would likely require termination regardless of trace length. With the numerous variables that impact signal integrity in a system, Micron recommends performing simulations to understand specific termination requirements.

DQ, DM, and Strobe Signals

To achieve robust high frequency operation, the DQ, DM, and DK signals on RLDRAM 3 have been designed with merged driver and on-die termination (ODT) circuitry similar to what is used on DDR3. This type of I/O benefits from improved tolerance on output driver impedance and reduced input capacitance.

Figure 4: Shared Driver and On-Die Termination



Calibration of these signals is done through a routine that compares the resistance of an external precision 240Ω resistor (±1%) connected to ZQ with the pull-up and pull-down legs of each output driver. The ZQ calibration routine is required upon initialization and is recommended based on a system's temperature and voltage drift rates to maintain linear output driver and termination impedance values. See Technical Note TN-41-02, DDR3 ZQ Calibration, for more information about how to calculate the calibration interval.

The output drivers have symmetrical output impedance that can be set to 40Ω or 60Ω via mode register 1. Micron recommends choosing a value that most closely matches the PCB trace impedance of the signals being driven.

ODT values of 40Ω, 60Ω, and 120Ω are also selected via mode register 1. The 40Ω and 60Ω values are intended for terminating point-to-point systems, and the 120Ω value can be useful when terminating a point-to-two-point system. Micron recommends selecting a value based on results from simulation-based signal integrity analysis. When enabled, ODT terminates these signals to $V_{DDQ}/2$. ODT will internally be dynamically disabled on

DQ signals after they begin to drive from a READ command and will turn back on upon the completion of the READ burst. The DM and DK signals are always terminated when ODT is enabled because they are input-only signals.

Termination Considerations for CK and QK

Micron recommends differential termination of 100Ω for both the CK and QK pairs. For the CK pair, place the terminating resistor as close as possible to the RLDRAM 3 device. For the QK pairs, place it as close as possible to the memory controller.

See Figure 5 and Figure 6 on page 9 for termination recommendations for systems sharing a CK pair between two RLDRAM 3 devices. Figure 5 represents a system with trace lengths from the split point to the DRAM of less than 1 inch. Figure 6 represents a system with trace lengths from the split point longer than 1 inch.

Figure 5: Single CK Differential Resistor Placed at Split Point

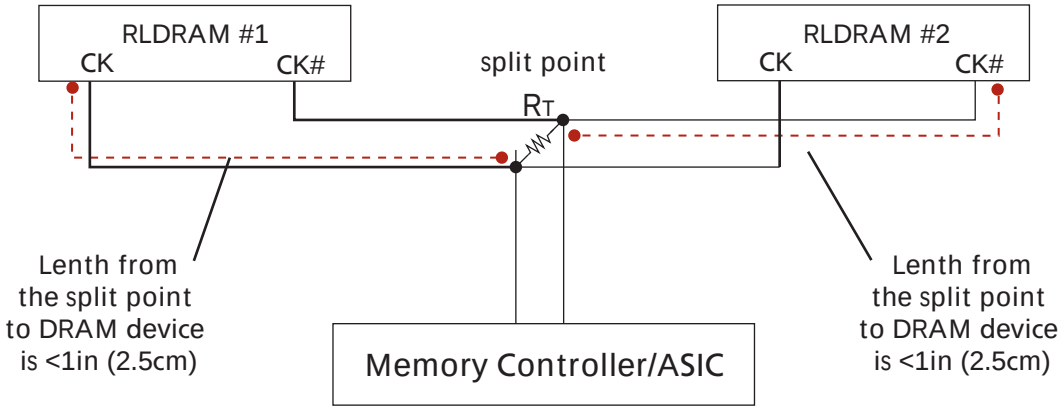
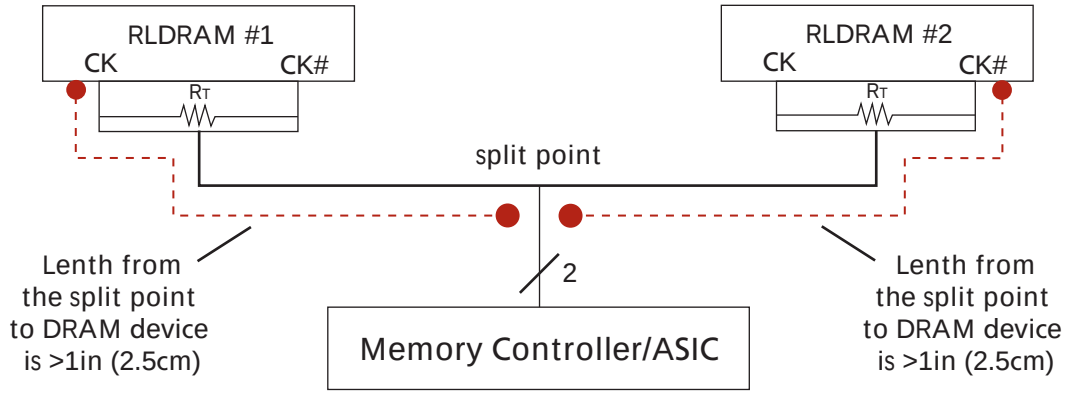


Figure 6: Two CK Differential Resistors Placed at DRAM



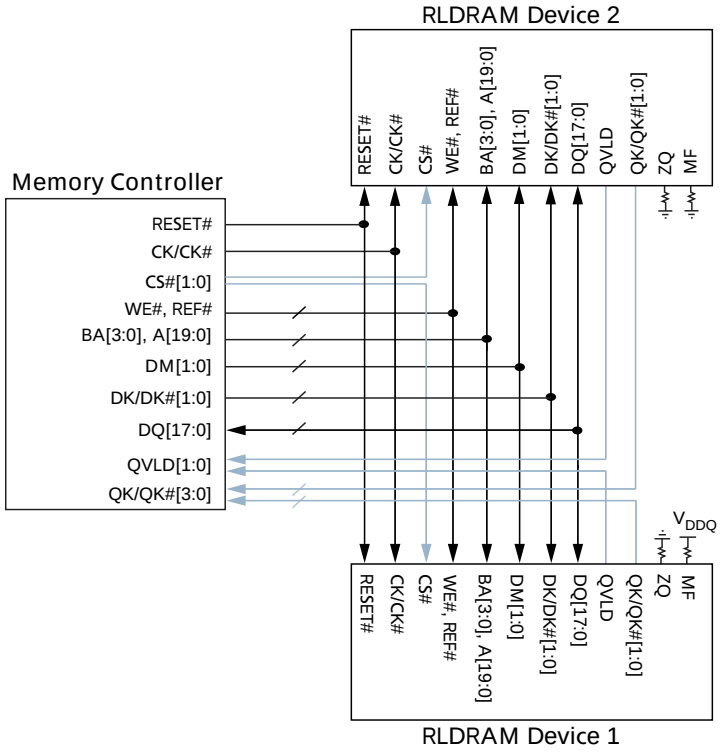
Depth Expansion

There are a number of considerations to make when combining two RLDRAM 3 devices to create an effectively deeper device. Figure 7 on page 10 is two x18 devices illustrating the signals that are shared between the two devices and those that are separated. Two separate CS# signals effectively create a dual rank memory channel. All input signals aside from CS# can be shared in this configuration. With the data bus shared between the two devices, care must be taken to ensure contention is avoided.

Because the QVLD and QK signals never tristate, they cannot be shared between the two devices without experiencing contention. Because QK signals are free-running, the controller has the flexibility to use these signals from one RLDRAM 3 only or to have separate sets for each device. Again, accounting for timing skews in the READ timing budget is required.

The external ZQ calibration resistor either can be shared between the two devices or separated. If shared, only NOPs can be issued by both devices during periods of calibration ($^{t}ZQ_{INIT}$, $^{t}ZQ_{OPER}$, $^{t}ZQ_{CS}$).

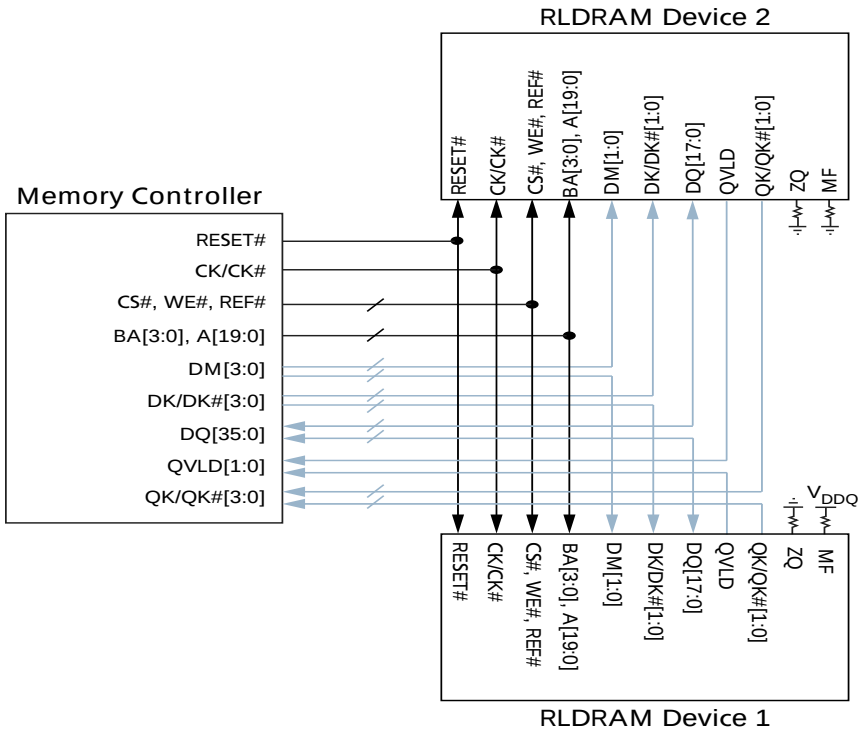
Figure 7: Depth Expansion



Width Expansion

To combine RLDRAM 3 devices to enable a wider data bus, signals can be connected as shown in Figure 8 on page 11. In this configuration, all signals are shared except the DQs, DM, QVLD, and data strobes. The rules regarding sharing of the ZQ pin that are described in “Depth Expansion” on page 9 also apply to width expansion.

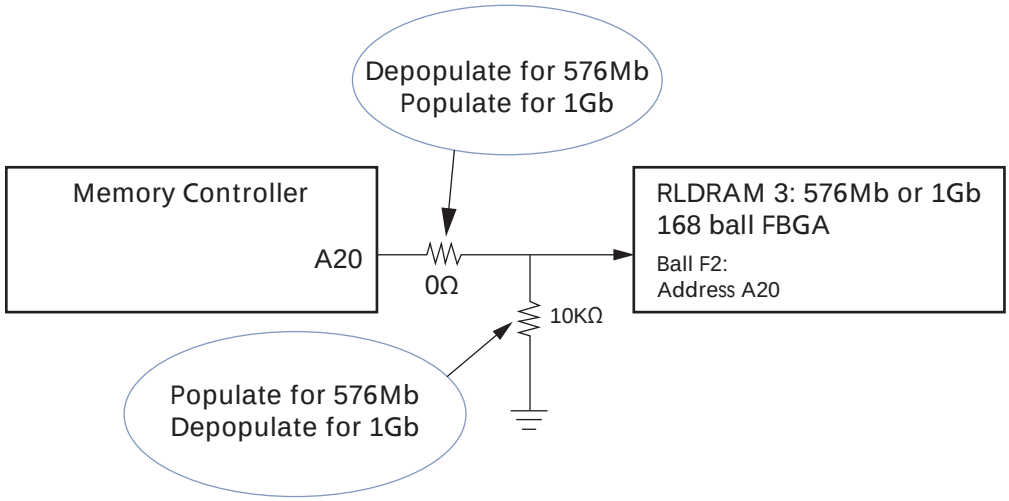
Figure 8: Width Expansion



Future Density Expansion

It is relatively simple to future-proof a board design to accommodate the monolithic 1Gb RLDRAM 3 device on Micron's roadmap. The only additional signal that is needed to support a monolithic 1Gb device beyond the 576Mb density is the address signal, A20. To accommodate the 1Gb device, Micron recommends routing a signal from the controller to the RLDRAM 3 with the topology shown in Figure 9 on page 12. A20 is internally connected on the 576Mb device and has parasitic characteristics of an address pin. It can be connected to V_{SS}.

Figure 9: Single PCB Layout to Accommodate Different RLDRAM 3 Densities



It should be noted that the number of rows will be doubled on the monolithic 1Gb RLDRAM 3 device (32k rows per bank instead of 16k per bank on the 576Mb device). This causes the number of REFRESH commands to double to refresh every cell in the device. The average periodic refresh interval for the 1Gb device will be 0.244µs (as opposed to 0.489µs for the 576Mb device).

Unused Signals

Certain systems may not require the use of all DQ or data strobe pins on the RLDRAM 3 device. If a x18 or x36 device is used but only the lower byte (or lower two bytes of a x36) of data is needed, the following must be done:

- Connect DK1 to V_{SS} via a 1k Ω resistor[1]
- Connect DK1# to V_{DDQ} via a 1k Ω resistor[1]
- Connect DM1 to V_{DDQ} via a 1k Ω resistor[1]
- Connect unused upper DQ byte (or DQ bytes for x36) to V_{SS} via a 1k Ω resistor[1]
- QK1, QK1#, and QVLD1 can be left floating

Notes: 1. If ODT is used, the 1k Ω resistor should be changed to a value 2x that of the selected ODT. This ensures the $V_{IH(AC)}$min and $V_{IL(AC)}$max specifications are adhered to with adequate margin.

RLDRAM 3 Timing Specifications that Impact Timing Budget

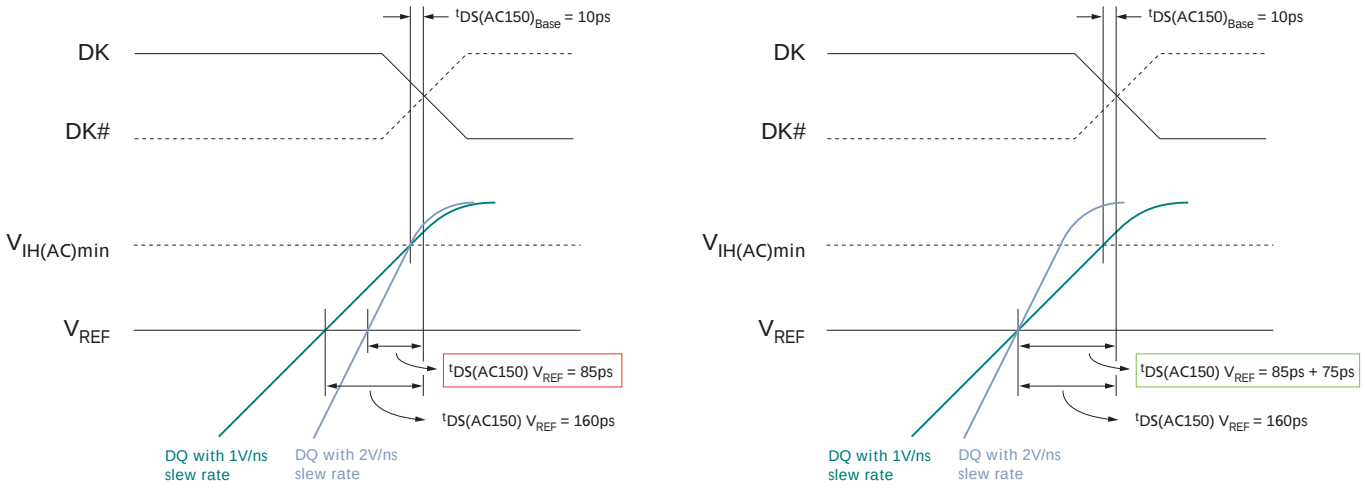
The following section details the relevant RLDRAM 3 specifications that impact a data capture timing budget. Proper understanding of these specifications will ensure that no more or no less of the timing budget is allocated to the RLDRAM 3 than is required.

Write Timing Specifications

The RLDRAM 3 captures data from WRITE commands via the free-running differential input strobes, DK. The controller must provide the DK signals so that they are center-aligned with DQ at the balls of the RLDRAM 3 package. This requires adherence to the setup and hold specifications (^{t}DS[AC150] and ^{t}DH[DC100], respectively). The nominal specifications for data setup and hold timing in the RLDRAM 3 datasheet are based on a nominal slew rate of 1 V/ns. Slew rates faster than this require derating of the base setup

and hold timing specifications. Base setup and hold as well as derating specifications can be found in the RLDRAM 3 datasheet. Derating is required for faster slew rates because the input buffer doesn't begin to turn on until later than it does during the nominal slew rate. This is illustrated in Figure 10 comparing a DQ having a 1 V/ns and a 2 V/ns slew rate. To meet the $^{t}DS(AC150)_{VREF}$ specification, 75ps must be added to the setup time with the 2 V/ns slew rate. Further information on derating can be found in the RLDRAM 3 data sheet.

Figure 10: Derating Setup and Hold Timing



Example without Derating

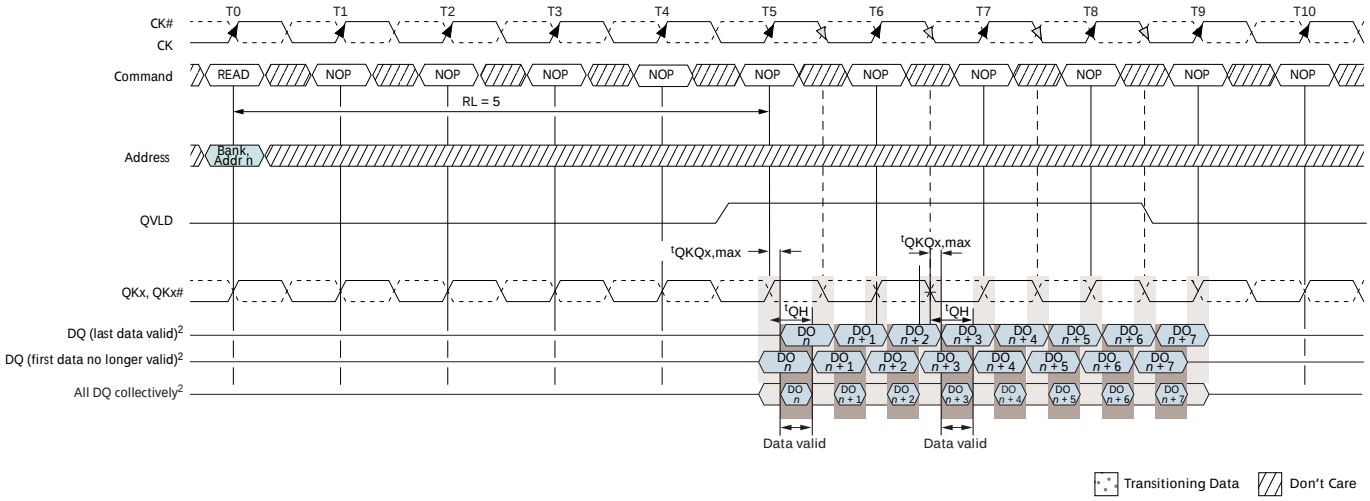
Example with Derating

Read Timing Specifications

Data from a READ command is edge-aligned with the dedicated free-running differential READ strobes, QK. One QK pair is associated with each byte of data (QK[0:3] for the x36 and QK[0:1] for the x18). Because the output data strobes are free-running, a data valid signal, QVLD, is also asserted with the READ data. This simplifies data capture circuitry at the controller. QVLD asserts HIGH one-half-clock cycle prior to valid data on the DQ bus after a READ command has been issued. This gives the controller time to enable its data input buffers prior to capturing data. QVLD subsequently drives low after the READ burst is complete.

The READ data valid window and associated specifications are illustrated in Figure 11 on page 14.

Figure 11: Read Data Valid Window



The specifications shown in Figure 11 represent timing guaranteed at the balls of the RLDRAM 3 package. These timing specifications take into account internal package routing mismatch and skew derived from pattern sensitivities that cause effects, such as SSO.

The ^{t}QKQx timing parameter defines the skew between a QK pair with its respective group of 9 DQ.

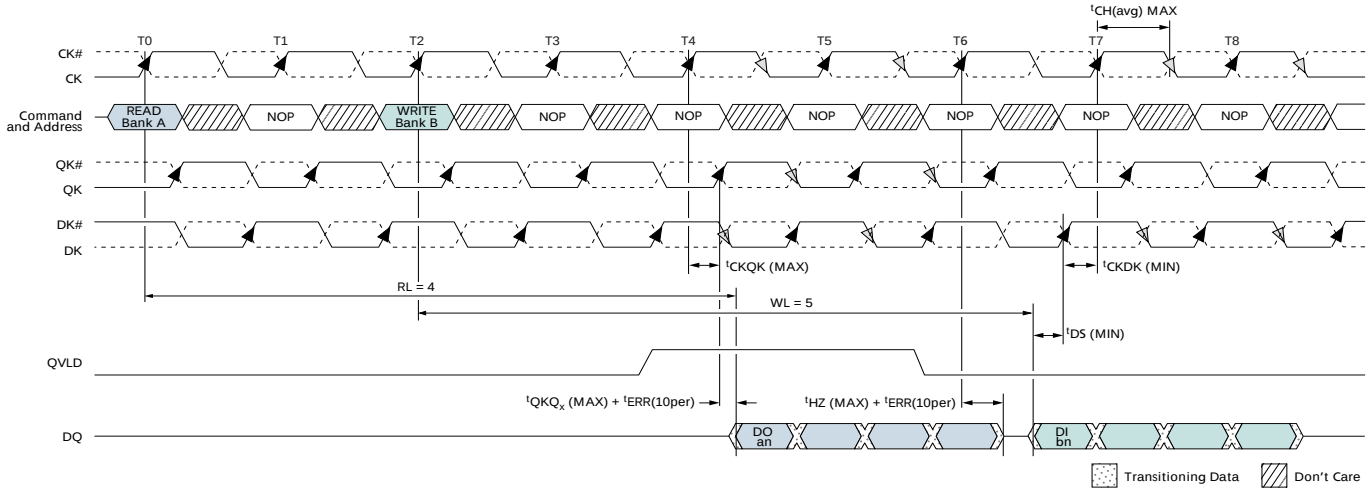
The ^{t}QH parameter assumes worst case duty cycle on CK. Because the RLDRAM 3 DLL does not correct duty cycle distortion, the duty cycle of CK is directly reflected in the duty cycle of QK and DQ. Therefore, any improvements to the CK duty cycle results in direct improvements in ^{t}QH and the resulting data valid window. One specification not shown in Figure 11 that has an impact on the READ data valid window is input clock jitter. The ^{t}QH specification must be derated by the amount of input clock jitter present (larger of $^{t}JIT(per)_{MIN}$ or $^{t}JIT(per)_{MAX}$).

Bus Turnaround Considerations

The RLDRAM 3 allows for back-to-back WRITE to READ and READ to WRITE operations. Additional intermediary NOP commands are only required if the board and/or controller skews are large enough to cause contention on the data bus during a bus turn-around.

Figure 12 on page 15 illustrates the RLDRAM 3 specifications that must be taken into consideration when determining if an additional NOP is required between READ and WRITE commands to avoid data bus contention. In this example, data contention occurs before board skew is even considered if worst case conditions are assumed for all of the RLDRAM 3 input and output timing specifications. To improve upon this, the controller must improve input jitter, duty cycle of CK, and the alignment of CK and DK (^{t}CKDK).

Figure 12: READ to WRITE Bus Turnaround Timing Analysis



Calculating Data Capture Timing Budget

To create a complete data capture timing budget, the RLDRAM 3 timing specifications in Figure 12 must be combined with the timing requirements of the controller. The amount of margin available in the timing budget after the RLDRAM 3 and controller have been accounted for determines the amount of margin left for the board level effects and subsequently determines the amount of effort needed to mitigate these effects. These board level effects include crosstalk, ISI, SSO, termination mismatch, trace length mismatch, input capacitance mismatch, and slew rates.

Simulation

Even after following the recommendations in this design guide, Micron strongly encourages designers perform board-level simulation to verify acceptable signal integrity across the memory interface. Micron offers both IBIS and HSPICE models for the RLDRAM 3 devices to aid in this process. These models can be found in the RLDRAM Part Catalog at www.micron.com. For more information and recommendations on the simulation process, refer to tech note TN-46-11: DDR SDRAM Point-to-Point Simulation Process also found at www.micron.com.

Conclusion

This design guide provides designers with recommendations for creating robust RLDRAM 3-based designs that offer better memory functionality and system stability. Additional RLDRAM 3 design resources can be found at www.micron.com.

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