Technical Note

Calculating Memory System Power for RLDRAM® 2

Introduction

With a unique eight-bank architecture optimized for high frequency and ultra-low random access times, Micron's reduced latency DRAM (RLDRAM® 2) addresses the high bandwidth memory requirements for communication and data storage applications. Because system designers need to accurately project power supply requirements for their systems—and also determine the cooling needs for ATCA and other form factors—they are concerned about calculating RLDRAM 2 power usage.

An accurate way to determine a power budget is essential, but not always provided, in the device data sheets. This technical note explains how RLDRAM 2 devices consume power. It also provides tools to help better estimate the system power specifically consumed by the RLDRAM 2. These tools can be modified to fit a wide variety of different systems. Because all systems need to manage heat, power consumption, and performance while meeting the requirements of a given application, the tools provided in this technical note identify methods for adjusting the RLDRAM 2 system usage to consume less power without greatly impacting overall system performance.

In addition to detailing RLDRAM 2 power consumption, this technical note provides examples and specifications. Because the values provided in the examples here may change over time, the device data sheet must be referenced for the most current values. Note that the underlying concepts of the calculations will remain the same.

For more complete details about the RLDRAM 2, refer to the RLDRAM 2 data sheets at www.micron.com.rldram and to Micron technical note, "RLDRAM 2 Design Guide."

DRAM Operation

To estimate the power consumption of the RLDRAM 2, it is necessary to understand the basic functionality of the device (see Figure 1 on page 2). The master operation of the RLDRAM 2 is controlled by chip select (CS#). When CS# is HIGH, the RLDRAM 2 command decoder is disabled, and incoming commands are ignored. For the RLDRAM 2 to recognize incoming commands, CS# needs to be LOW; this enables the command decoder. After CS# is LOW, commands can be sent to and registered by the RLDRAM 2.

When the RLDRAM 2 device is enabled, it has a simple command set that includes AUTO REFRESH (AREF), READ, WRITE, and MODE REGISTER SET (MRS) commands. Unlike conventional DRAM, ACTIVATE or PRECHARGE commands are not required with RLDRAM 2. Each time a READ or WRITE command is issued, the RLDRAM 2 device automatically activates the required bank and row addresses to transfer the data to the sense amplifiers, and then it restores the data to the cells in the array. This enables reads and writes to take place any time the device is enabled, assuming $^ت RC$ is met for the bank being accessed.

A READ command that is issued to the RLDRAM 2 decodes the bank, row, and column addresses. Data at this address location is temporarily stored in the sense amplifiers until it is driven through the I/O gating to the internal DQ read latch. Once in the latch, data is sent to the output drivers and made available on the DQ pins.

When a WRITE command is issued, the same process occurs in the opposite order. Data from the DQ pins is latched into the data receivers/registers and transferred to the internal data drivers. These drivers then transfer the data to the sense amplifiers through the I/O gating to the decoded bank, row, and column address.

RLDRAM 2 also has on-die termination (ODT) on the data I/O and on the DM signal. When enabled in the mode register, the ODT is controlled dynamically by the RLDRAM 2 and disabled when the RLDRAM 2 is driving the data bus. Because the ODT is terminated to the midrail, additional power is only consumed when the RLDRAM 2 is being written.

Figure 1:   288Mb RLDRAM 2 Functional Block Diagram
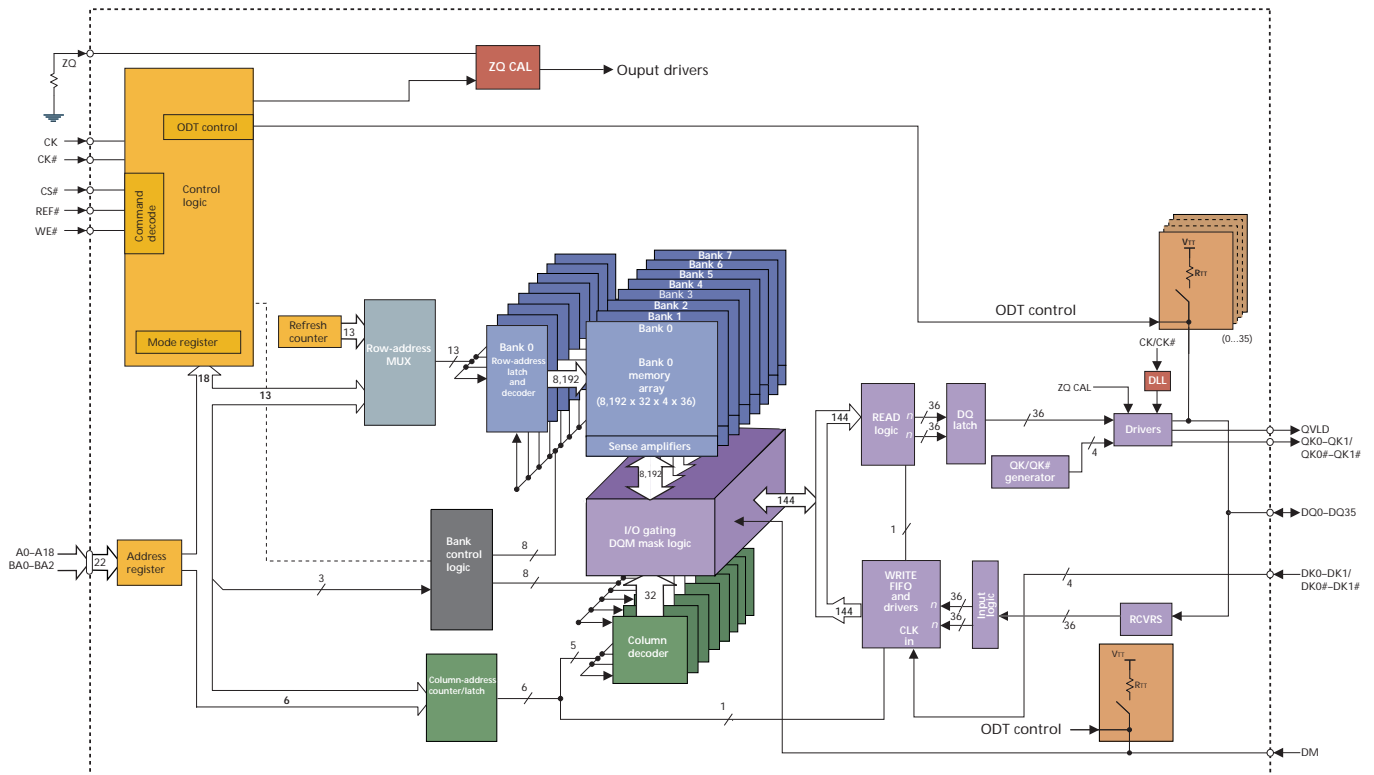
RLDRAM Power Calculators

The I_{DD} values referenced in "Data Sheet Specifications" on page 22 are taken from the 288Mb RLDRAM 2 CIO data sheet. Although the values provided in data sheets may differ among vendors and devices, the concepts for calculating power are the same. It is important to verify all data sheet parameters prior to using the information in this technical note.

Methodology Overview

To calculate system power, complete the required four steps:

1. Calculate the power subcomponents from the data sheet specifications. (This calculation is denoted as Pds[XXX], where XXX is the subcomponent power.)
2. Derate the power based on the command scheduling (Psch[XXX]).
3. Derate the power to the system's actual operating V_{DD} and clock frequency (Psys[XXX]).
4. Sum the subcomponents of the system's operating conditions to calculate the total power consumed by the DRAM.

Background Power

Unlike standard DRAM devices, no CKE signal is present in RLDRAM 2 to disable the propagation of the clock through the RLDRAM 2. The lowest power state (I_{SB1}) is attained when the RLDRAM 2 is idle and no inputs (including the clocks) are toggling. In this state, the RLDRAM 2 device draws about 75mA of current. Figure 2 on page 4 shows the typical current usage of the RLDRAM 2 device when the input signals are idle.

Rather than stopping the input clocks from toggling as is required to obtain the I_{SB1} values, the user can reduce the current demand of the RLDRAM 2 simply by bringing the CS# pin HIGH. This state is called active standby and is represented by I_{SB2} in the data sheet. This mode (see Figure 2 on page 4) is the lowest power state in which the device can function properly. As noted, CS# controls the master operation of the RLDRAM 2. When CS# is HIGH, the command decoder is disabled, and all incoming commands are ignored.

Figure 2:   Standby Current Consumption
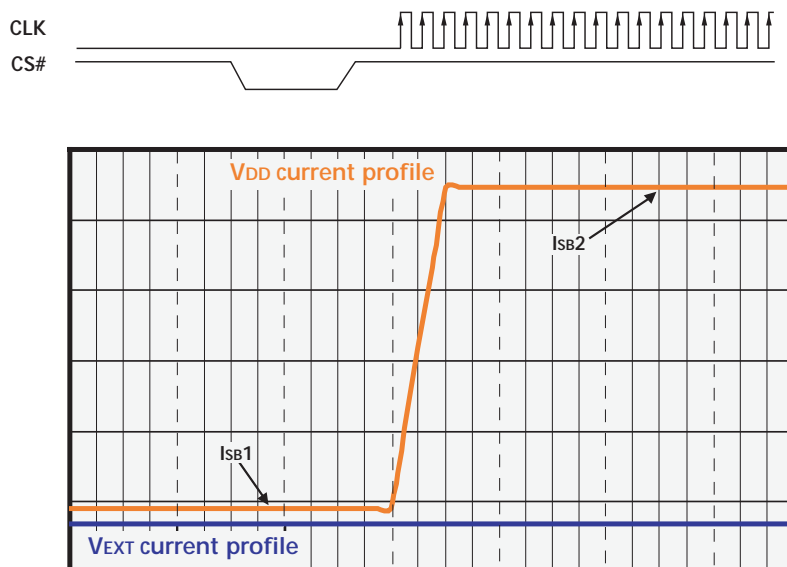
To perform any command on the RLDRAM 2, CS# must be taken LOW. On the first rising edge of CK after CS# goes LOW, a command is registered, assuming setup and hold times are met as specified by the RLDRAM 2 CIO data sheet.

Calculation of the power consumed by the RLDRAM 2 during active standby is easily completed by multiplying the $I_{SB}2$ value and the voltage applied to the device V_{DD} and V_{EXT}.

For the V_{DD} supply:

$$Pds(SB) = I_{SB}2 \text{ x } V_{DD}$$

(Eq. 1)

For the V_{EXT} supply:

$$Pds(SB) = I_{SB}2 \text{ x } V_{EXT}$$

(Eq. 2)

The data sheet specification for the $I_{SB}2$ values are taken at the worst-case V_{DD} (1.9V) and V_{EXT} (2.63V).

The calculations for the V_{DD} supply are as follows:

$$Pds(SB) = 288mA \text{ x } 1.9V$$
$$\mathbf{Pds(SB) = 547.2mW}$$

(Eq. 3)

The calculations for the V$_{EXT}$ supply are as follows:

Pds(SB) = 26mA x 2.63V
Pds(SB) = 68.38mW

(Eq. 4)

Active Power

When CS# is LOW, the RLDRAM 2 device is active and must read or write data. To read or write data, the controller needs to issue a READ or WRITE command along with the appropriate address to an open bank. Because each READ or WRITE command automatically activates the appropriate bank and row, an ACTIVATE command is not necessary. A PRECHARGE command is also automatic after a READ or WRITE command is executed.

Write Power

Whenever CS# is LOW, data can be read from or written to the RLDRAM 2 device. An example of a WRITE cycle is shown in Figure 3 on page 5; Figure 4 on page 6 illustrates the effect of the WRITE command on the current consumption of the RLDRAM 2.

Figure 3:   WRITE Cycle (Single Bank Active)
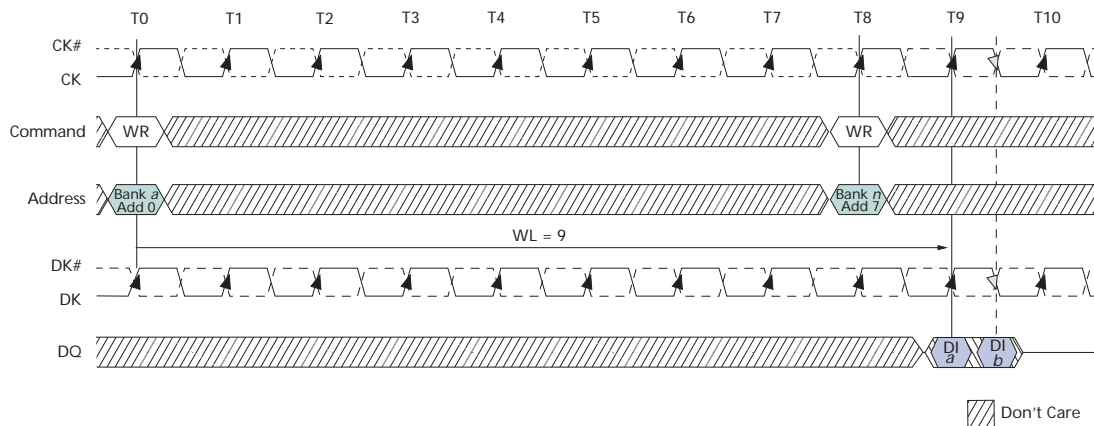
Notes: 1. WR = WRITE command with BL = 2, ^{t}RC = 20ns, and ^{t}CK = 2.5ns.

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Figure 4:   Current Consumption Profile of WRITE (Single Bank Active)
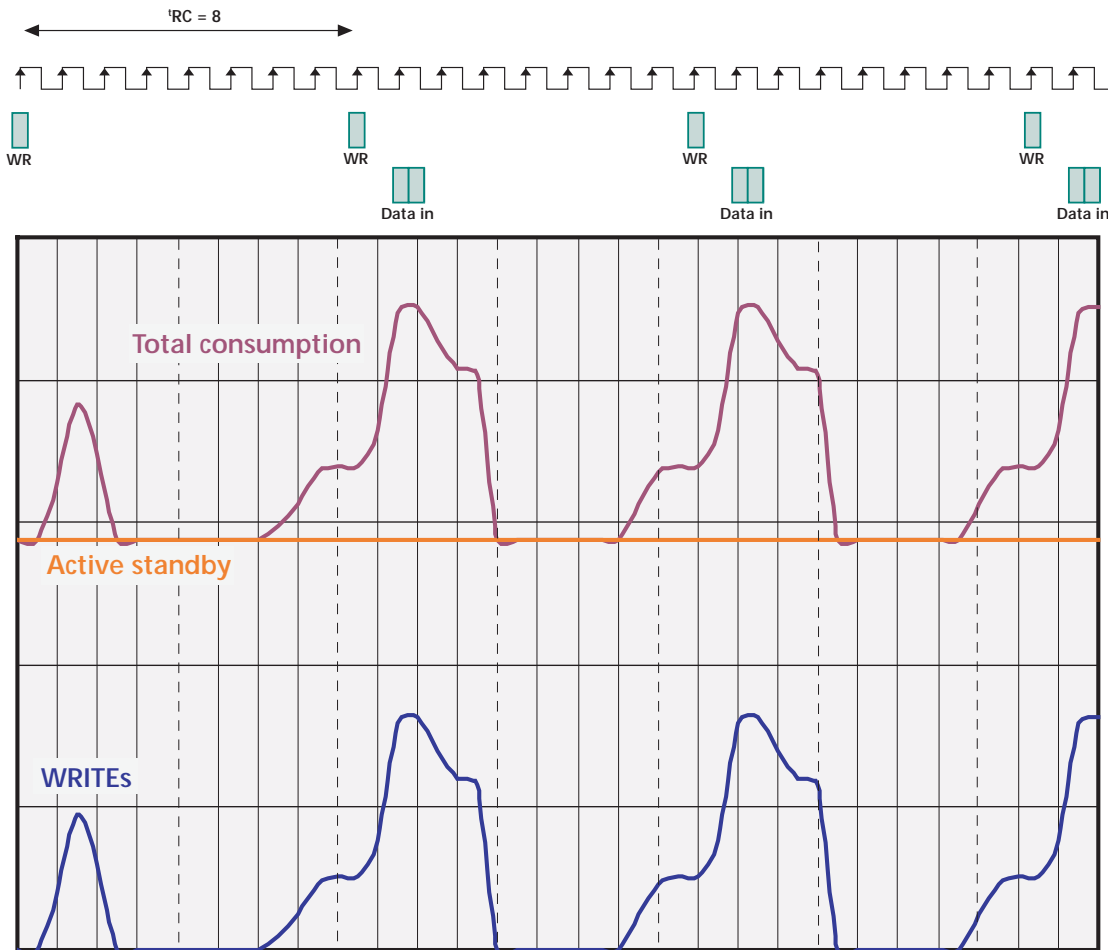
When a single WRITE command is issued, a single bank of the RLDRAM 2 is activated. If a new WRITE command is issued every ^{t}RC, only one bank is active in a BL = 2 mode. The amount of current consumed by having a single bank written is represented by IDD1. In BL = 4 (IDD2) or BL = 8 (IDD3) modes, similar values are available. To identify the power associated with only the WRITE command and not the active standby current, ISB2 must be subtracted. The calculation for the data sheet write component of power, Pds(WR), for BL = 2 is shown in Equation 5 and Equation 6.

For the VDD supply:

Pds(WR) = (IDD1 - ISB2) VDD
Pds(WR) = (374mA - 288mA) x 1.9V
Pds(WR) = 163.4mW

(Eq. 5)

For the V_{EXT} supply:

$Pds(WR) = (I_{DD}1 - I_{SB}2) \times V_{EXT}$
$Pds(WR) = (41mA - 26mA) \times 2.63V$
Pds(WR) = 39.45mW

(Eq. 6)

When constant writes are made in a BL = 2 mode (as shown in Figure 5), the consumption of current associated with the WRITE becomes $I_{DD}2W$. For BL = 4 and BL = 8, these values are $I_{DD}4W$ and $I_{DD}8W$, respectively. The effect on current consumption associated with continuous writes to the RLDRAM 2 can be seen in Figure 6 on page 8.

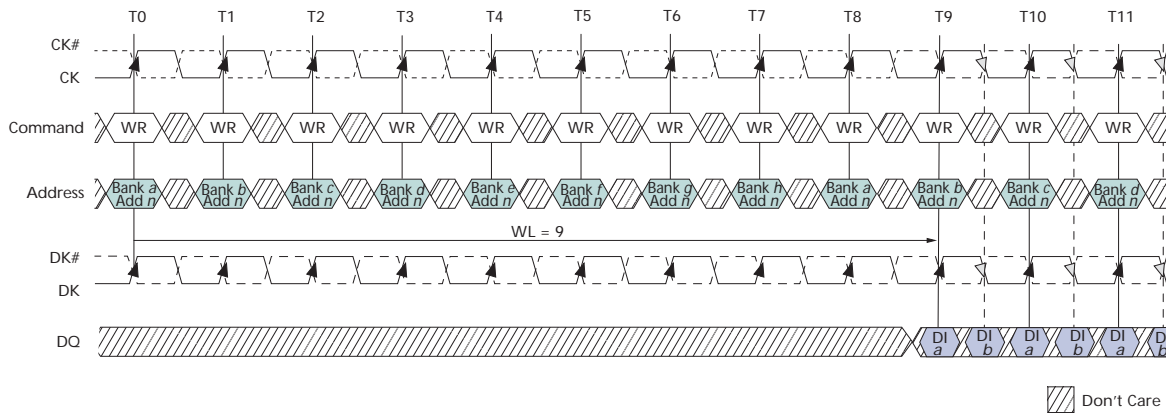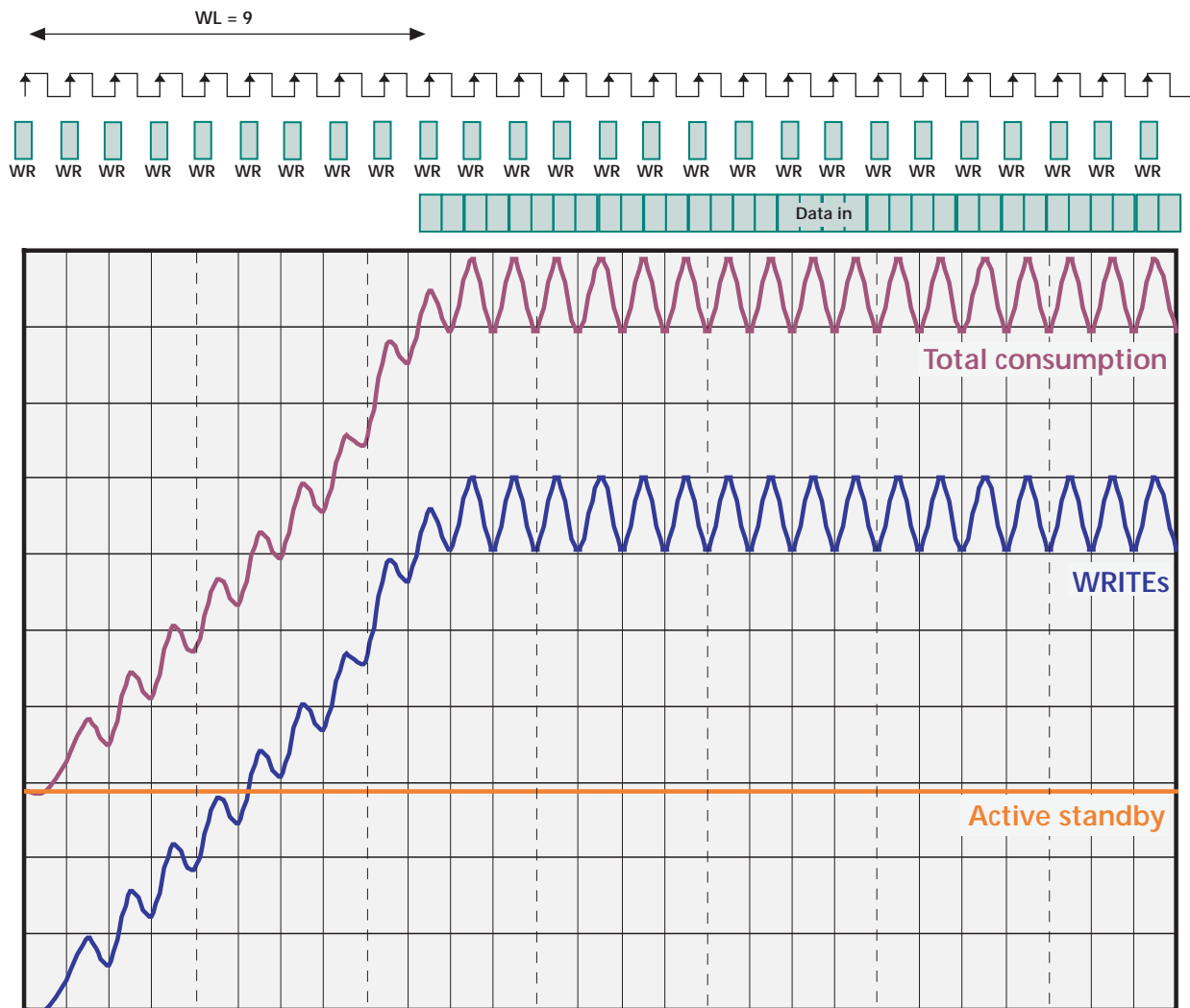**Figure 5:   Continuous WRITE Cycle**

Don't Care

Figure 6:   Continuous Current Write Consumption Profile

The continuous write current consumption profile represents the total power consumed by the RLDRAM 2. To calculate the power consumed by the writes, remove the active standby power from the equation. The continuous write component of the power, Pds(CW), can easily be calculated in BL = 2 mode, as shown in Equation 7 and Equation 8.

For the V_{DD} supply:

Pds(CW) = ($I_{DD}2W1$ - $I_{SB}2$) x V_{DD}
Pds(CW) = (990mA - 288mA) x 1.9V
Pds(CW) = 1333.8mW

(Eq. 7)

For the V$_{EXT}$ supply:

Pds(CW) = (I$_{DD}$2W1 - I$_{SB}$2) x V$_{EXT}$
Pds(CW) = (100mA - 26mA) x 2.63V
Pds(CW) = 194.62mW

(Eq. 8)

To scale the data sheet power to actual power based on command scheduling, first determine the ratio of the available bandwidth being used for write activity. This is denoted as WRsch%, which is the total number of write data cycles that are on the data bus versus the total number of clock cycles.

$$WRsch\% = \frac{(^tCK \times BL \times WR)}{^tRC \times 2}$$

(Eq. 9)

Where
- BL = burst length
- WR = number of WRITE cycles per ^tRC
- ^tRC = random cycle time (in nanoseconds)
- ^tCK = clock cycle time (in nanoseconds)

If we assume ^tCK = 2.5ns, ^tRC = 20, BL = 2, and WR = 3, then:

$$WRsch\% = \frac{2.5ns \times 2 \times 3}{20 \times 2}$$

WRsch% = 37.5%

(Eq. 10)

After the ratio of writes is known, the power associated with the scheduled writes, Psch(WR), can be easily calculated from Pds(CW).

For the V$_{DD}$ supply:

Psch(WR) = Pds(CW) x WRsch%
Psch(WR) = 1333.8mW x 37.5%
Psch(WR) = 500.2mW

(Eq. 11)

For the V$_{EXT}$ supply:

Psch(WR) = Pds(CW) x WRsch%
Psch(WR) = 194.62mW x 37.5%
**Psch(WR) = 72.98mW**

(Eq. 12)

Read Power

Whenever CS# is LOW, data can be read from or written to the RLDRAM 2 device. Figure 7 on page 10 provides an example of a READ cycle. Figure 8 on page 11 illustrates the effect of a READ command on current consumption.

Figure 7:   Single Bank Active READ Cycle
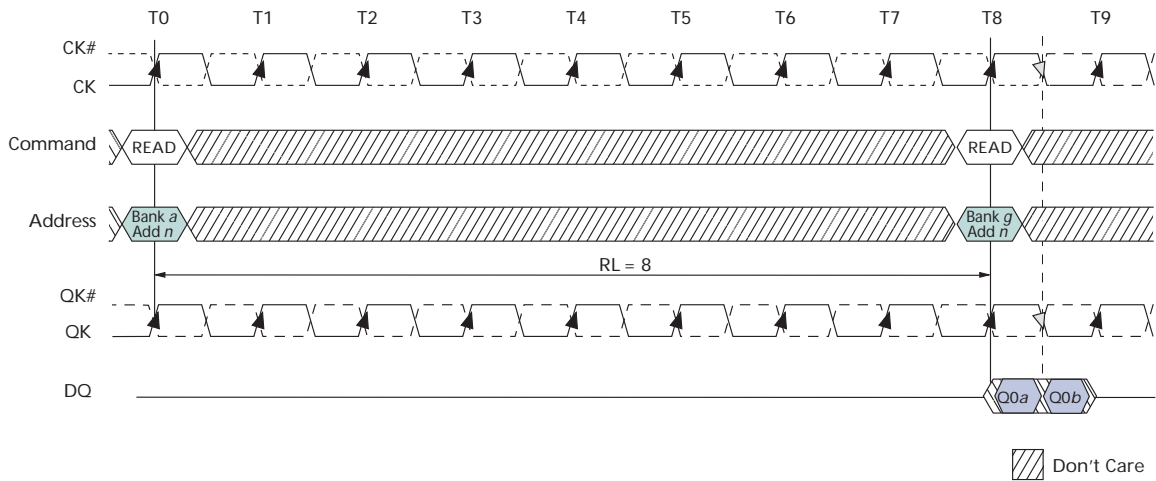
Notes: 1. READ command with BL = 2, ^tRC = 20ns, and ^tCK = 2.5ns.

Figure 8:   Single Bank Active Current Consumption Profile of READ
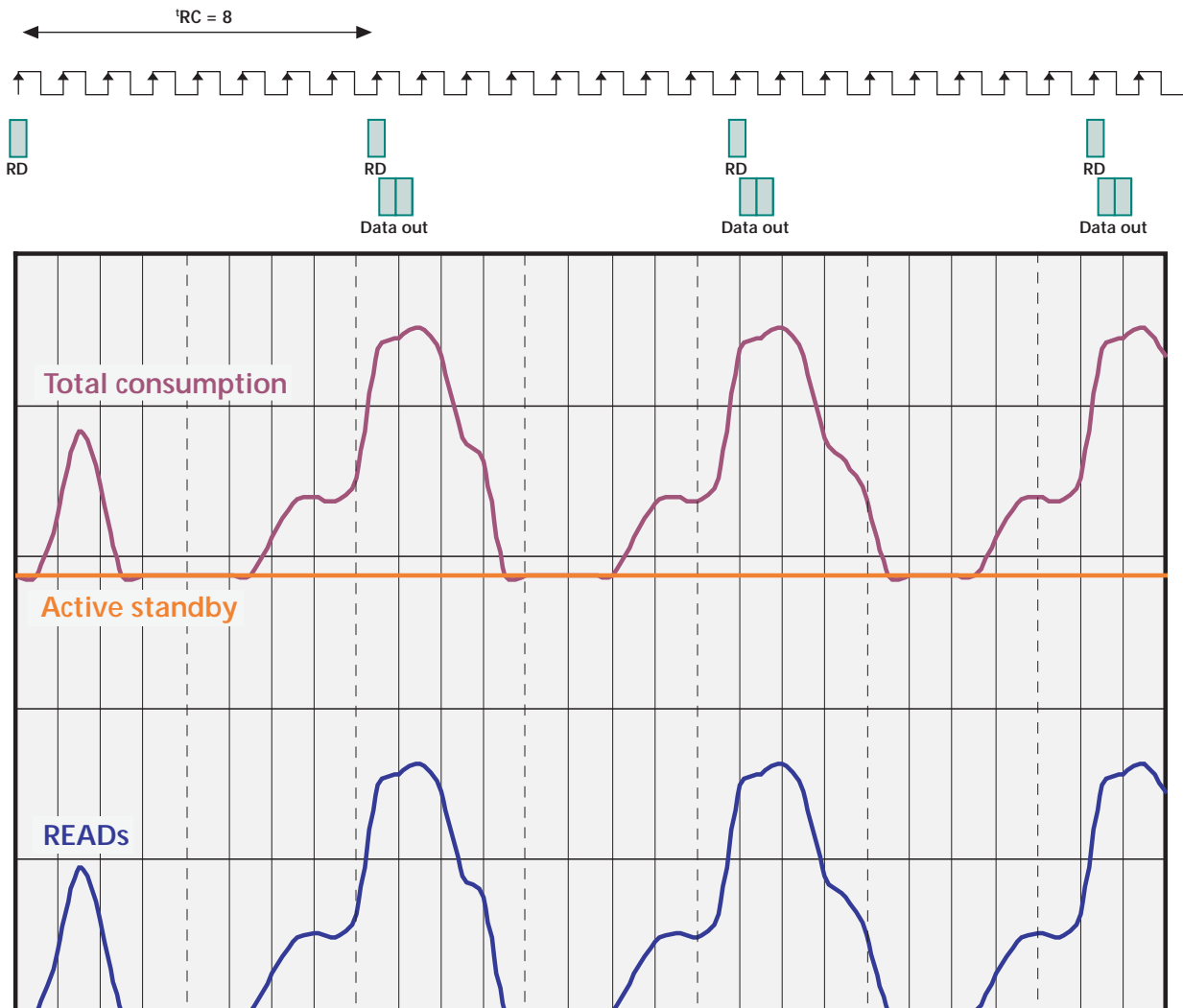
When a single READ command is issued, a single bank of the RLDRAM 2 is activated. If a new READ command is issued every ^{t}RC, only one bank is active. The amount of current consumed by a single bank READ command in a BL = 2 mode is represented by I$_{DD}$1, and values for reading from the RLDRAM 2 are I$_{DD}$2 (BL = 4) and I$_{DD}$3 (BL = 8). Identifying the power associated with only the READ command is also the same as with the WRITE command and can be seen in Equation 13 and Equation 14.

For the V$_{DD}$ supply:

Pds(RD) = (I$_{DD}$1 - I$_{SB}$2) x V$_{DD}$
Pds(RD) = (374mA - 288mA) x 1.9V
Pds(RD) = 163.4mW

(Eq. 13)

For the V_{EXT} supply:

$Pds(RD) = (I_{DD}1 - I_{SB}2) \times V_{EXT}$
$Pds(RD) = (41mA - 26mA) \times 2.63V$
Pds(RD) = 39.45mW

(Eq. 14)

As shown in Figure 9, when constant READ commands are issued in a BL = 2 mode, the consumption of current associated with the read becomes $I_{DD}2R$. For BL = 4 and BL = 8, these values are $I_{DD}4R$ and $I_{DD}8R$, respectively. The effect on current consumption associated with continuous reads to the RLDRAM 2 is illustrated in Figure 10 on page 13.

Figure 9:   Continuous READ Cycle

Don't Care
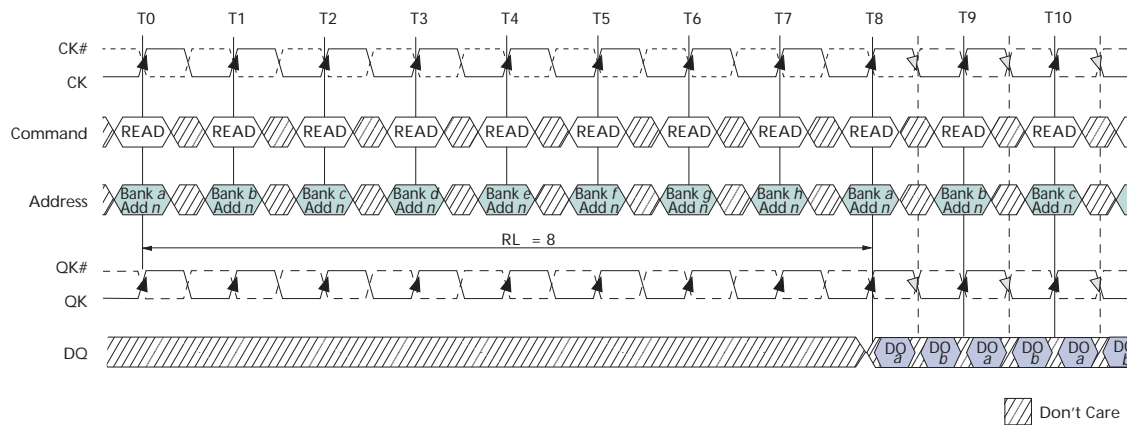
Figure 10: Continuous Current Consumption Profile of READ
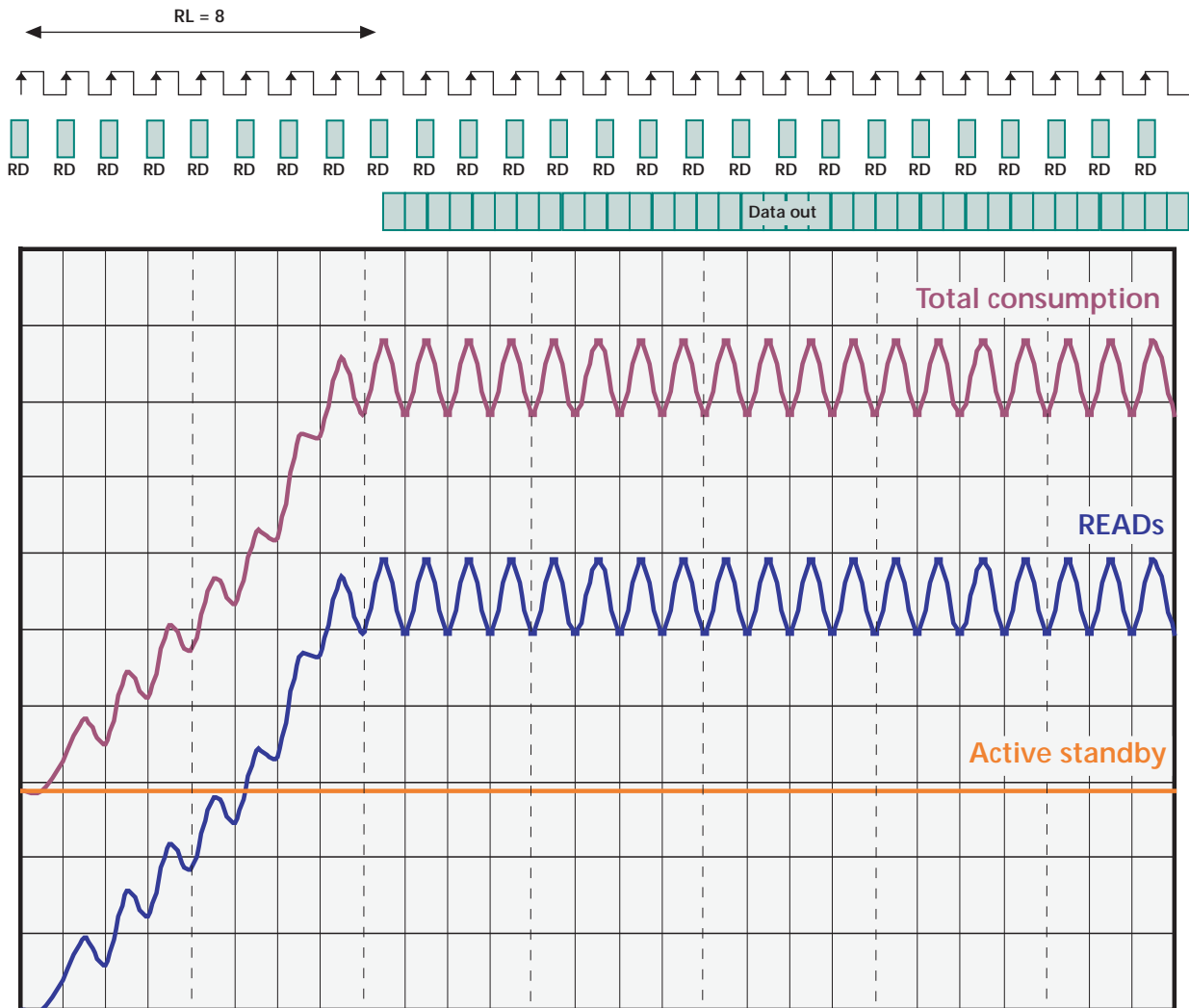
The continuous read current consumption profile represents the total power consumed by the RLDRAM 2. To calculate the power consumed by reads, remove the active standby power from the equation. Calculate the continuous read component of the power, Pds(CR), for BL = 2 as follows:

For the V_{DD} supply:

Pds(CR) = ($I_{DD}2R$ - $I_{SB}2$) x V_{DD}
Pds(CR) = (880mA - 288mA) x 1.9V
Pds(CR) = 1124.8mW

(Eq. 15)

13

For the V_{EXT} supply:

$Pds(CR) = (I_{DD}2R - I_{SB}2)$ x V_{EXT}
$Pds(CR) = (100mA - 26mA)$ x $2.63V$
$Pds(CR) = 194.62mW$

(Eq. 16)

Scaling the data sheet power to the actual power based on command scheduling for reads is similar to that of writes. First, determine the ratio of the available bandwidth being used for read activity. This is noted as RDsch%, which is the total number of read data cycles on the data bus versus the total number of clock cycles. The RDsch% calculation is as follows:

$$RDsch\% = \frac{(^tCK \text{ x } BL \text{ x } RD)}{^tRC \text{ x } 2}$$

(Eq. 17)

Where
- BL = burst length
- RD = number of READ cycles per ^tRC
- ^tRC = random cycle time (in nanoseconds)
- ^tCK = clock cycle time (in nanoseconds)

If we assume $^tCK = 2.5ns$, $^tRC = 20$, $BL = 2$, and $RD = 3$, then:

$$RDsch\% = \frac{2.5ns \text{ x } 2 \text{ x } 3}{20 \text{ x } 2}$$

$RDsch\% = 37.5\%$

(Eq. 18)

After the ratio of reads is known, the power associated with the scheduled reads, Psch(RD), can be easily calculated from Pds(CR).

For the V_{DD} supply:

$Psch(RD) = Pds(CR)$ x $RDsch\%$
$Psch(RD) = 1124.8mW$ x 37.5%
$Psch(RD) = 421.8mW$

For the V_{EXT} supply:

$Psch(RD) = Pds(CR)$ x $RDsch\%$
$Psch(RD) = 194.62mW$ x 37.5%
$Psch(RD) = 72.98mW$

(Eq. 19)

I/O Termination Power

Psch(RD) and Psch(WR) are only part of the total power for read and write sequences. Data sheet specifications do not include output driver power or ODT power. These powers are system-dependent and must be calculated for each system.

RLDRAM 2 systems can vary greatly depending on an application's density and bandwidth requirements. A typical point-to-point system is shown in Figure 11. The data bus connects the controller to a single RLDRAM 2 device. Additionally, the controller and the RLDRAM 2 use ODT for the data lines, so no external passive components are required for this example system.

Figure 11:   Typical System DQ Termination
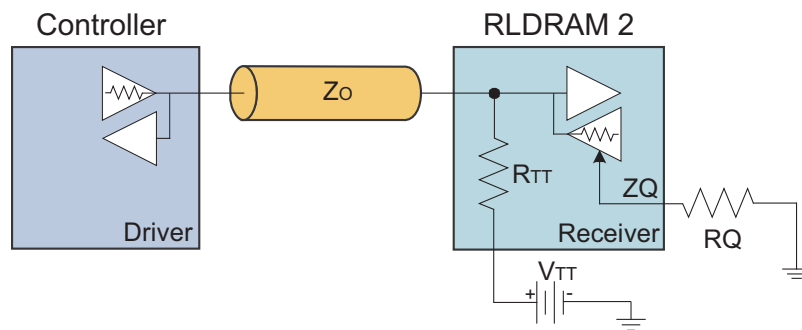
The drivers in the system have an impedance of R_{ON}, which pulls the bus toward V_{DDQ} for a "1" or V_{SSQ} for a "0." The termination on the die is functionally a midrail termination in which a resistor is tied to a V_{TT} supply equal to $V_{DDQ}/2$. R_{TT} is the termination value selected for the device and is nominally 150Ω.

A simple termination scheme for the example system is shown in Table 1. Because this is a point-to-point system, all output drivers are set to 50Ω. Termination at the controller is assumed to be 75Ω, while a worst-case 125Ω is assumed for the RLDRAM 2's ODT value.

Table 1:   Termination Configuration

	Controller		RLDRAM 2	
	R_{ON}	R_{TT}	R_{ON}	R_{TT}
Writes to RLDRAM 2	50Ω	Off	Off	125Ω
Reads from RLDRAM 2	Off	75Ω	R = RQ/5	Off

Two methods can be used to calculate the power consumed by the output driver and ODT. One method is to simulate the system data bus using component Spice models, and then average the power consumed over a sufficiently long pattern of pseudo-random data.

A second, simpler method, however, is to calculate the DC power of the output driver against the termination. This is usually not worst-case, but it provides a first-order approximation of the output power.

The I/O powers that must be calculated include the following:
- **PdqRD:** output driver power when driving the bus
- **PdqWR:** termination power when terminating a write to the RLDRAM 2

The nominal RLDRAM 2 I/O termination DC power for the memory system can be calculated using Thevenin equivalent circuits (see Figures 12 and 13). The resultant I/O termination DC power values for the RLDRAM 2, per I/O pin, are listed in Table 2. The controller termination power is not accounted for in the DRAM I/O termination power values even though they are shown for reference.
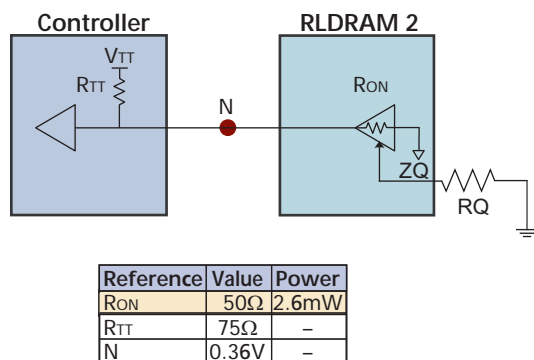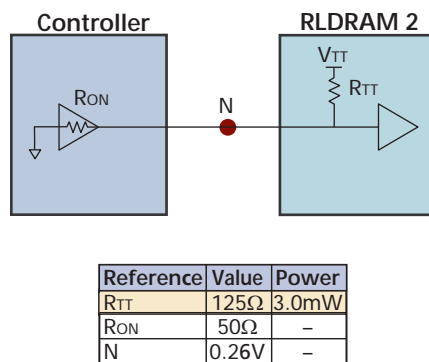
Figure 12: **RLDRAM 2 READ**

Reference	Value	Power
R_{ON}	50Ω	2.6mW
R_{TT}	75Ω	–
N	0.36V	–

Figure 13: **RLDRAM 2 WRITE**

Reference	Value	Power
R_{TT}	125Ω	3.0mW
R_{ON}	50Ω	–
N	0.26V	–

Table 2: **Typical I/O and Termination Power Consumption**

	DC Power (RLDRAM 2)	
	READ	**WRITE**
Accessing the RLDRAM 2	PdqRD = 2.6mW/DQ	PdqWR = 3.3mW/DQ

To calculate the power for output or termination on the DRAM, the power per DQ must be multiplied by the number of outputs (DQ and QVLD) on the device (num_DQR). The QK signals are not counted in the total number of outputs because they are always running and are included in the Isb2 value. For write termination, the DQ and data mask must be included in the sum of the total number of write signals terminated (num_DQW) when the ODT feature is enabled. The values of num_DQR and num_DQW will vary depending on data width of the RLDRAM 2.

Equation 20 calculates the RLDRAM 2 power for the following I/O buffer operations:

- **Pds(DQ):** RLDRAM 2 output driver power when driving the bus
- **Pds(termW):** RLDRAM 2 termination power when terminating a write to the RLDRAM 2

Pds(DQ) = Pdq(RD) x num_DQR
Pds(termW) = Pdq(WR) x num_DQW

(Eq. 20)

To illustrate how the power is calculated, an assumption using a x36 device is shown. For this example, num_DQR includes **36 DQ and the QVLD signal totaling 37**, whereas num_DQW totals 37 to account for the DQ and the data mask signal. The DC power values from Table 2 on page 15 are also used, and the results are presented in Equation 21.

Pds(DQ) = 2.6mW x 41
Pds(DQ) = 106.6mW
Pds(termW) = 3.3mW x 37
Pds(termW) = 122.1mW

(Eq. 21)

To complete the I/O and termination power calculation, the 100 percent usage data sheet specification must be derated based on the data bus utilization. The read and write utilization has already been provided as RDschd% and WRschd%. The power based on command scheduling is then calculated, as shown in Equation 22.

Psch(DQ) = Pds(DQ) x RDsch%
Psch(termW) = Pds(termW) x WRsch%

(Eq. 22)

Sample calculations showing how to determine output and termination percentages are provided in "RLDRAM 2 Power Spreadsheet Usage Example" on page 22.

Refresh Power

Refresh is the final power component to be calculated for the device to retain data integrity. RLDRAM 2 memory cells store data information in small capacitors that lose their charge over time and must be recharged. The process of recharging these cells is called refresh.

In the RLDRAM 2 CIO data sheet, the specification for refresh is I_{REF1}. I_{REF1} assumes the RLDRAM 2 is operating continuously at minimum REFRESH-to-REFRESH command spacing, ^tCK. (This is a BURST REFRESH command in the RLDRAM 2 CIO data sheet.) During this operation, the RLDRAM 2 is also consuming I_{SB2} active standby current. Thus, to calculate only the power due to burst refresh, I_{SB2} must be subtracted, as shown in the following equations.

For the V$_{DD}$ supply:

Pds(REF1) = (I$_{REF1}$ - I$_{SB2}$) x V$_{DD}$
Pds(REF1) = (785mA - 288mA) x 1.9V
Pds(REF1) = 944.3mW

(Eq. 23)

For the V$_{EXT}$ supply:

Pds(REF1) = (I$_{REF1}$ - I$_{SB2}$) x V$_{EXT}$
Pds(REF1) = (133mA - 26mA) x 2.63V
Pds(REF1) = 281.41mW

(Eq. 24)

The RLDRAM 2 also has a distributed refresh parameter (I$_{REF2}$). Here a REFRESH command is issued every ^{t}RC so that only a single bank is active. Again, this parameter includes the I$_{SB2}$ active standby current and must be subtracted, as shown in Equation 25:

For the V$_{DD}$ supply:

Pds(REF2) = (I$_{REF2}$ - I$_{SB2}$) x V$_{DD}$
Pds(REF2) = (326mA - 288mA) x 1.9V
Pds(REF2) = 72.2mW

(Eq. 25)

For the V$_{EXT}$ supply:

Pds(REF2) = (I$_{REF2}$ - I$_{SB2}$) x V$_{EXT}$
Pds(REF2) = (48mA - 26mA) x 2.63V
Pds(REF2) = 57.86mW

(Eq. 26)

However, REFRESH operations are typically distributed evenly over time at a refresh interval of ^{t}REF. Thus, the scheduled refresh power, Psch(REF), is the ratio of ^{t}RC to the average periodic refresh interval maximum (^{t}REF/8K/8 = 0.488μs), multiplied by Pds(REF2), as shown in Equation 27 and Equation 28.

For the V$_{DD}$ supply:

$$Psch(REF) = Pds(REF2) \times \frac{^tRC}{^tREF}$$
$$Psch(REF) = 72.2mW \times \frac{20ns}{0.488\mu s}$$

Psch(RD) = 2.96mW

(Eq. 27)

For the V_{EXT} supply:

$$Psch(REF) = Pds(REF2) \times \frac{t_{RC}}{t_{REF}}$$

$$Psch(REF) = 57.86mW \times \frac{20ns}{0.488\mu s}$$

Psch(REF) = 2.37mW

(Eq. 28)

Power Derating

Thus far, the power calculations have assumed a system is operating at worst-case V_{DD}. They have also assumed that the clock frequency in the system is the same as the frequency defined in the data sheet. The resulting power is denoted as Psch(XXX). Most systems, however, operate at different voltages or clock frequencies than the systems defined in the data sheet. Each of the power components must be derated to the actual system conditions, with the resulting power denoted as Psys(XXX).

Voltage Supply Scaling

Most applications operate near the nominal V_{DD}, not at the absolute maximum V_{DD}. The only power parameters that do not scale with V_{DD} are the data I/O and termination power because the system V_{DD} is already assumed when the initial power is calculated.

On RLDRAM 2, power is typically related to the square of the voltage. This is because most of the power is dissipated by capacitance, with $P = CV^2 f$ where C = internal capacitance, V = supply voltage, and f = frequency of the clock or command (see "Frequency Scaling" on page 19"). Thus, to scale power to a different supply voltage:

$$Psys(XXX) = Psch(XXX) \times \left(\frac{System\ V_{DD}}{MAX\ specification\ V_{DD}}\right)^2$$

(Eq. 29)

Frequency Scaling

Many power components, such as Psch(WR) and Psch(RD), are dependent on the clock frequency at which a device operates. The power consumed in active standby (Pds) is also affected by the clock frequency and can be scaled similarly.

Unlike those mentioned previously, Psch(REF) does not scale with clock frequency. Psch(REF) is dependent on the interval between AREF commands, as discussed in "Refresh Power" on page 17.

The power for components dependent on an operating frequency can be scaled for actual operating frequency as follows:

$$Psys(XXX) = Psch(XXX) \times \frac{freq\_used}{spec\_freq}$$

(Eq. 30)

The sys_freq is the actual clock frequency at which a device operates in the system. The spec_freq is the clock frequency at which the device was tested during the I_{DD} tests. This information is provided in the test condition notes in a data sheet. The test condition notes also describe tests at the maximum clock rate for a specific speed grade, device configuration, and burst length (BL). The combination of all V_{DD} and clock frequency scaling is presented in Equation 31.

$$Psys(SB) = Psd(SB) \text{ x } \left[\frac{sys\_freq}{spec\_freq} \right] \text{ x } \left[\frac{system\,V_{DD}}{MAX\,spec\,V_{DD}} \right]^2$$

$$Psys(WR) = Psch(WR) \text{ x } \left[\frac{sys\_freq}{spec\_freq} \right] \text{ x } \left[\frac{system\,V_{DD}}{MAX\,spec\,V_{DD}} \right]^2$$

$$Psys(RD) = Psch(RD) \text{ x } \left[\frac{sys\_freq}{spec\_freq} \right] \text{ x } \left[\frac{system\,V_{DD}}{MAX\,spec\,V_{DD}} \right]^2$$

$$Psys(REF) = Psch(REF) \text{ x } \left[\frac{system\,V_{DD}}{MAX\,spec\,V_{DD}} \right]^2$$

(Eq. 31)

Calculating Total RLDRAM 2 Power

The tools are now in place to calculate the system power for any usage condition. The last task is to put them together. The various system power subcomponents are summed together, as shown in Equation 32.

$$Psys(TOT) = Psys(SB) + Psys(WR) + Psys(RD) + \\ Psys(REF) + Psys(DQ) + Psys(termW)$$

(Eq. 32)

Having compensated for all primary variables that can affect device power, the total power dissipation of the RLDRAM 2 device operating under specific system usage conditions has now been calculated.

RLDRAM 2 Power Spreadsheet

Calculating all these equations by hand can be tedious. For this reason, Micron has published an online worksheet to simplify the process. Micron's RLDRAM 2 System-Power Calculator, as well as detailed instructions for its use, are available on Micron's Web site at www.micron.com/systemcalc. An example of how to use the system-power calculator is provided in "RLDRAM 2 Power Spreadsheet Usage Example" on page 22.

To use the online spreadsheet, enter the device data sheet conditions on the "RLDRAM 2 Spec" tab. Starting values are provided, but it is important to verify all data sheet parameters prior to using the spreadsheet. Note that multiple speed bins and RLDRAM 2 densities are included, and correct inputs are required for each column used.

After the data sheet values are entered, the actual RLDRAM 2 configuration to be used for the power calculations is selected on the "RLDRAM 2 Config" tab, as shown in Figure 14, Spreadsheet – RLDRAM 2 Configuration Tab. The density, speed grade, configura-

tion, I/O, ODT, nominal $V_{DD}Q$, and burst length are selected with pull-down menus. In addition, the mode register configuration is selected for the different ^tRC and latency modes. These inputs correctly configure the calculator for a specific RLDRAM 2 based on the data input on the "RLDRAM 2 Spec" worksheet.

Figure 14: Spreadsheet – RLDRAM 2 Configuration Tab

RLDRAM 2 density	288Mb ▼
Device width	x36 ▼
Speed grade	-2.5 ▼
Configuration (mode register bits 0–2)	0 (Default) ▼
I/O	Common ▼
On-die termination (mode register bit 7)	1 : On ▼
$V_{DD}Q$ (nominal)	1.8V ▼
Burst length	2 ▼

After the RLDRAM 2 configuration has been selected, the actual system operating conditions, such as V_{DD} and V_{EXT}, system clock frequency, and read and write utilization and capacitive load, are entered into the "System Config" tab, as shown in Figure 15. The burst length is extracted from the "RLDRAM 2 Config" information.

Figure 15: Spreadsheet – System Configuration Tab

System V_{DD}	1.8	V	
System V_{EXT}	2.5	V	
System CK frequency	400	MHz	
Burst length (self extracted)	2		Extracted from the RLDRAM 2 configuration settings
Percent of READs	30%		Note: Minimum refresh rate is assumed,
Percent of WRITEs	10%		Remaining percent is considered to be active standby
Capacitive load on the data bus	20	pF	

After all inputs are entered, the actual RLDRAM 2 device power derated to the system conditions can be found on the "Summary" tab. Note that the interim power calculations for data sheet power and scheduled power are found on the "Power Calcs" worksheet.

Data Sheet Specifications

Table 3: Data Sheet Assumptions for Micron's 288Mb RLDRAM 2 (-25)

| Description	Condition	Symbol	Max -25
Active standby current	CS# = 1; No commands; Bank address incremented, and half of the address/data bits change once every four clock cycles	I_{SB2} (V_{DD}) x36	288
		I_{SB2} (V_{DD}) x18/x9	288
		I_{SB2} (V_{EXT})	26
Operational current	BL = 2; Sequential bank access; Bank transitions once every ^tRC; Half of the address bits change once every ^tRC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD1} (V_{DD}) x36	374
		I_{DD1} (V_{DD}) x18/x9	348
		I_{DD1} (V_{EXT})	41
Distributed refresh current	Single bank refresh; Sequential bank access; Half of the address bits change once every ^tRC; Continuous data	I_{REF2} (V_{DD}) x36	326
		I_{REF2} (V_{DD}) x18/x9	325
		I_{REF2} (V_{EXT})	48
Operating burst write current example	BL = 2; Cyclic bank access; Half of the address bits change every clock cycle; Continuous data; Measurement is taken during continuous write	I_{DD2W} (V_{DD}) x36	990
		I_{DD2W} (V_{DD}) x18/x9	970
		I_{DD2W} (V_{EXT})	100
Operating burst read current example	BL = 2; Cyclic bank access; Half of the address bits change every clock cycle; Measurement is taken during continuous read	I_{DD2R} (V_{DD}) x36	880
		I_{DD2R} (V_{DD}) x18/x9	860
		I_{DD2R} (V_{EXT})	100

Notes: 1. Refer to the data sheet for the most current information and test conditions.
2. I_{DD} is dependent on output loading, cycle rates, burst length, and configuration.

RLDRAM 2 Power Spreadsheet Usage Example

An example for calculating RLDRAM 2 power in the system environment is shown in Figure 16 on page 23. The system assumptions are for a system with point-to-point connections on the data bus and a dual-loaded address and command bus. The data bus consists of two x36 RLDRAM 2 devices that result in a 72-bit data bus for the system. This system is populated with 288Mb density RLDRAM 2 -25 devices. The controller (shown in blue in Figure 16 on page 23) drives a common command/address bus, shared by the RLDRAM 2 (shown in green in Figure 16).

Total data bus utilization for this example is 40 percent with read data using 30 percent of the bandwidth and write data using 10 percent of the bandwidth. All data bus termination follows the guidelines shown in Table 2 on page 16. It is assumed the minimum refresh rate is used for this system.

Figure 16: Example of a Single-Load Data/Dual-Load Address and Command System Environment
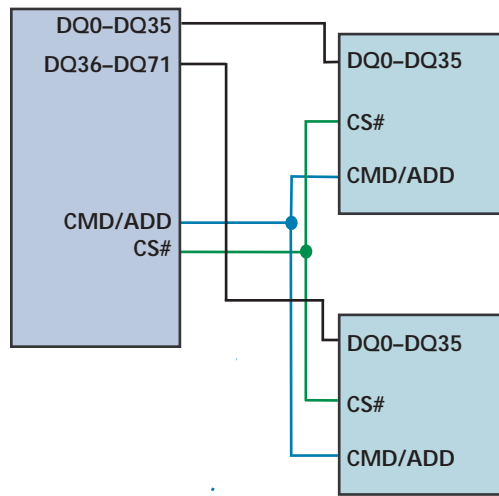
Notes: 1. Total data bus utilization = 40 percent (30 percent read data and 10 percent write data).

To use the RLDRAM 2 Power Calculator spreadsheet, the I$_{DD}$ data sheet values must be loaded into the "RLDRAM 2 Spec" tab. After these values are verified, the DRAM used in the system is selected using the pull-down menus on the "DRAM Config" tab, as shown in Figure 17.

Figure 17: RLDRAM 2 Configuration

RLDRAM 2 density	288Mb
Device width	x36
Speed grade	-2.5
Configuration (mode register bits 0–2)	0 (Default)
I/O	Common
On-die termination (mode register bit 7)	1 : On
V$_{DD}$Q (nominal)	1.8V
Burst length	2

After the RLDRAM 2 is configured, the system implementation of the memory must be set using the "System Config" tab, as shown in Figure 18 on page 24. The I/O and termination powers are system-dependent. This example aligns to those calculated in Table 2 on page 16. Because this example system has two memory devices, each RLDRAM 2 is assumed to consume the total data bandwidth. Thus, each RLDRAM 2 has a read utilization of 30 percent and a write utilization of 10 percent.

With this information, the spreadsheet calculates the average time between read-to-write and write-to-read databus transitions as well as the number of active banks based on the clock frequency. As previously mentioned, the minimum refresh rate is used, and all other cycles are assumed to be active standby.

Figure 18: System Configuration

System V$_{DD}$	**1.8**	V
System V$_{EXT}$	**2.5**	V
System CK frequency	**400**	MHz
Burst length (self extracted)	**2**	
Percent of READs	**30%**	
Percent of WRITEs	**10%**	
Capacitive load on the data bus	**20**	pF

After all assumptions are entered into the spreadsheet, it calculates each subcomponent of power and derates it to the system use condition. The results are shown on the "Summary" tab and in Figure 19. During the system conditions, each RLDRAM 2 uses 311.4mW of power for background operations (STANDBY and REFRESH) on the V$_{DD}$ supply and another 6.5mW on the V$_{EXT}$ supply. For reading data from the RLDRAM 2, 475.2mW of power is consumed on the V$_{DD}$ supply, 75mW on the V$_{EXT}$ supply, and 243.7mW on the V$_{DDQ}$ supply. Writing data to the RLDRAM 2 consumes 178.2mW of power on the V$_{DD}$ supply and 25mW of power on the V$_{EXT}$ supply. In this example, because the ODT is enabled, writes to the RLDRAM 2 also consume an additional 30.6mW on the V$_{TT}$ supply.

Therefore, each RLDRAM 2 consumes a total of approximately 1345.6mW. Because the calculations are completed on a per-RLDRAM 2 basis and the data is assumed to be uniformly distributed among all the RLDRAM 2 in the system, the total memory subsystem power is approximated as two times 1345.6mW, or approximately 2.7W.

Figure 19: Average Power Consumption Summary

	V$_{DD}$	V$_{EXT}$	V$_{DDQ}$	V$_{TT}$	
Psys(STBY)	311.0	39.0	0.0	0.0	mW
Psys(REF)	3.0	0.6	0.0	0.0	mW
Total Standby/Refresh Power	**314.0**	**39.6**	**0.0**	**0.0**	**mW**
Psys(ACT)	207.4	26.0	0.0	0.0	mW
Psys(WR)	126.4	18.5	0.0	30.6	mW
Psys(RD)	319.7	55.5	243.7	0.0	mW
Total RD/WR	**653.4**	**100.0**	**243.7**	**30.6**	**mW**
Total RLDRAM 2 Power	**967.4**	**139.6**	**243.7**	**30.6**	**mW**

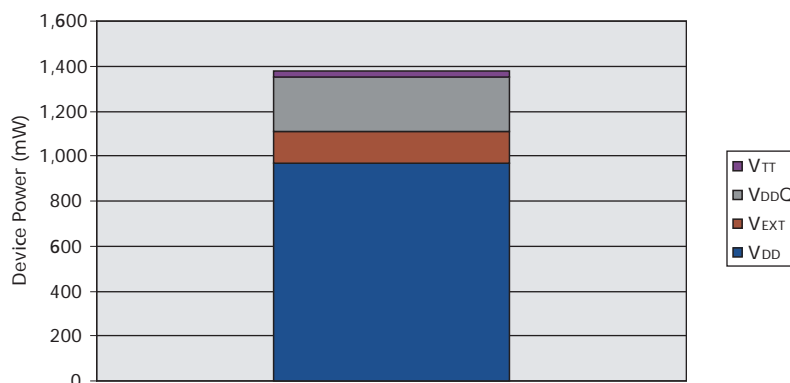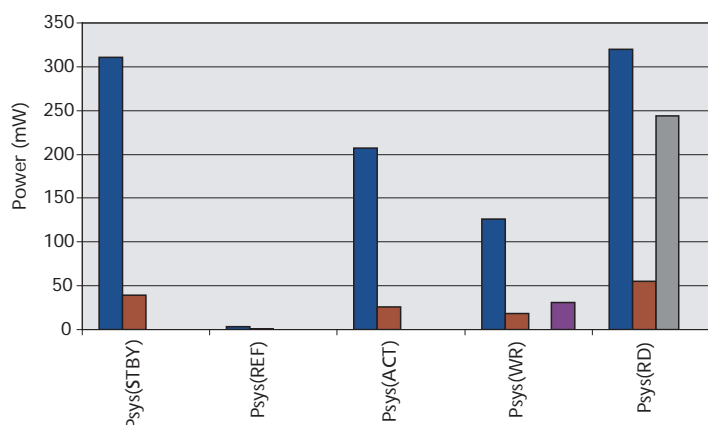**Figure 20: Average Power Consumption per Device**

Figure 21: Power Consumption Breakout

Conclusion

When relying on a data sheet alone, it can be difficult to determine how much power an RLDRAM 2 device consumes in a system environment. However, by understanding the data sheet and how an RLDRAM 2 device consumes power, it is possible to create a power model based on system usage conditions. Such a model can enable system designers to experiment with various memory access schemes to determine the impact on power consumption.

In short, system designers can use this tool to estimate realistic power requirements for RLDRAM 2 devices and to adjust a system's power delivery and thermal budget accordingly, thereby optimizing system performance.

For more information about RLDRAM 2 and other Micron products, visit Micron's Web site at www.micron.com.