Technical Note

Exploring the RLDRAM™ 2 Feature Set

Introduction

With network line rates steadily increasing, memory density and performance are becoming extremely important in enabling network processors to perform packet processing quickly and efficiently. The architecture of reduced latency DRAM 2 (RLDRAM™ 2) addresses these higher-performance requirements by providing the performance-critical features networking and cache that applications need: high density, high bandwidth, and fast, SRAM-like random access. This technical note outlines the many performance-enhancing features offered by the innovative RLDRAM 2 architecture, codeveloped by Micron and Infineon Technologies AG.

Eight-Bank Architecture

As advanced DRAM, RLDRAM 2 memory utilizes an eight-bank architecture that is optimized for high-speed operation and a double data rate I/O for increased bandwidth. The eight-bank architecture enables RLDRAM 2 devices to achieve peak bandwidth by decreasing the probability of random access conflicts. In addition, incorporating eight banks results in a reduced bank size compared to typical DRAM devices, which use four. The smaller bank size enables shorter address and data lines, effectively reducing the parasitics and access time. While bank management remains important with RLDRAM 2 architecture, one bank is always available for use, even in the worst case (burst of two at 400 MHz operation). Increasing the burst length of the device increases the number of banks available.

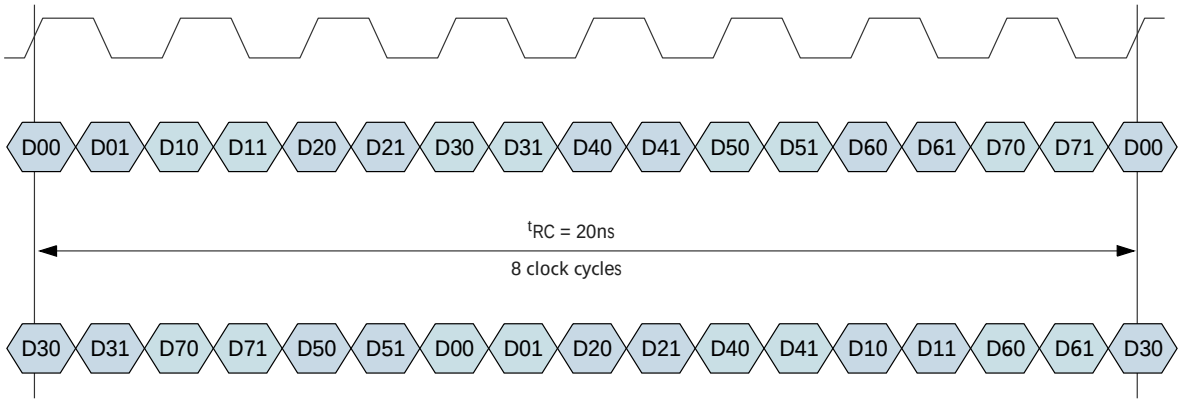
Table 1 illustrates the number of banks that must be employed to obtain full bus utilization, while Figure 1 on page 2 illustrates two examples of the worst case mentioned above; the first shows a sequential access to the banks and the second shows random order accesses.

Table 1: Bank Usage

Common I/O	-2.5	-3.3	-5
BL = 2	8	6	4
BL = 4	4	3	2
BL = 8	2	1/2[1]	1

Notes: 1. Alternates between 1 and 2 banks each successive cycle.

Figure 1: 8-Bank Cyclic Bank Access, 400 MHz 2-Word Burst – CIO Data Bus



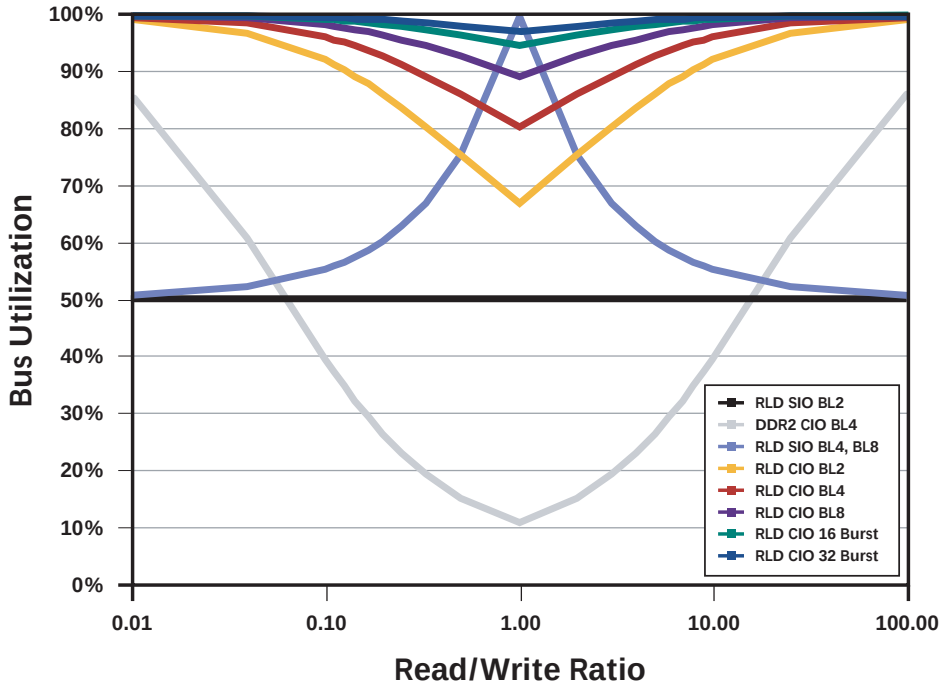
Notes:
1. At least one bank available at all times.
2. Any free bank can be accessed at any time.
3. No sequential order is otherwise needed.
4. Full utilization regardless of frequency.
5. Dxy = data *y* of bank *x*.

I/O Options

RLDRAM 2 architecture offers separate I/O (SIO) and common I/O (CIO) options. The SIO devices have separate READ and WRITE ports to eliminate bus turnaround cycles and contention. Optimized for near-term READ and WRITE balance, RLDRAM 2 SIO devices are able to achieve full bus utilization.

CIO devices have a shared READ/WRITE port that requires one additional cycle to turn the bus around. RLDRAM 2 CIO architecture is optimized for data streaming, where the near-term bus operation is either 100-percent READ or 100-percent WRITE, independent of the long-term balance. Designers should choose an I/O version that provides an optimal compromise between performance and utilization. Figure 2 on page 3 illustrates the performance variations between the versions at different read-to-write ratios.

Figure 2: RLDRAM 2 Bus Utilization



The RLDRAM 2 I/O interface provides other features and options, including support for both 1.5V and 1.8V I/O levels and a programmable output impedance that enables compatibility with both HSTL and SSTL I/O schemes. Micron's RLDRAM 2 devices are also equipped with on-die termination (ODT) to enable more stable operation at high speeds in multipoint systems. These features provide simplicity and flexibility for high-speed designs by bringing both end termination and source termination resistors into the memory device. Application designers can take advantage of these features as needed to reach the RLDRAM 2 operating speed of 400 MHz DDR (800 MHz data transfer).

At high-frequency operation, however, it is important that the signal driver, receiver, printed circuit board network, and terminations be analyzed to obtain good signal integrity and the best possible voltage and timing margins. Without proper terminations, the system may suffer from excessive reflections and ringing, leading to reduced voltage and timing margins. This, in turn, can lead to marginal designs and cause random soft errors that are difficult to debug. Micron's RLDRAM 2 devices provide designers with simple, effective, and flexible termination options for high-speed memory designs.

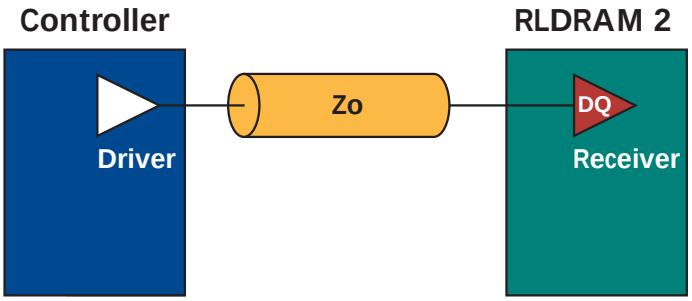
End Termination Resistors

Micron's RLDRAM 2 DQ and DM pins have a built-in or on-die end termination resistor, which offers several key advantages over the on-board termination that has been previously.

The advantages of Micron's RLDRAM 2 termination options are easily illustrated in a case where effective use of end termination can reduce signal integrity problems and improve system timing. The example in Figure 3 is based on a 1.8V model and a Micron® RLDRAM 2 device running at 400 MHz DDR operation.

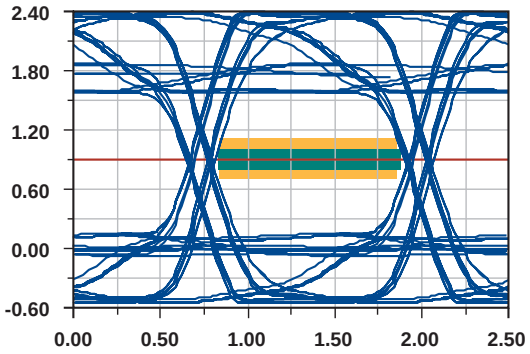
1. With the end termination resistor placed on-die, there are no additional trace stubs to cause reflections.
2. The on-die end termination resistor is automatically controlled: it can be disabled when the RLDRAM 2 device is driving the bus to provide better output control and conserve power, and it can be enabled at all other times to provide end termination of the signal for other drivers on the bus.
3. On-die end termination means there is no need to place termination resistors on the board, saving design time, board space, material costs, and assembly costs, and increasing product reliability.

Figure 3: Memory Subsystem With a Single Micron RLDRAM 2 Device



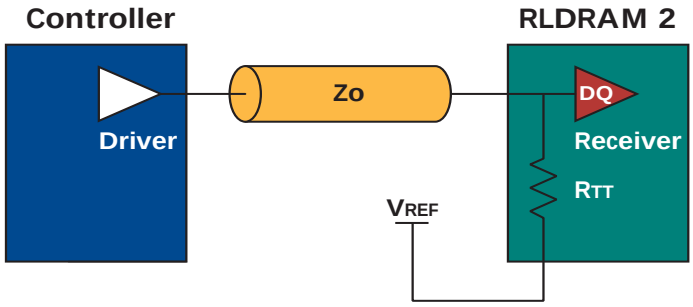
Simulations of this network (see Figure 4 on page 5) show the data eye at the receiver die input, which raises several discussion points. Although the simulation uses a 1.8V model, the voltage at the input can be much higher than 1.8V. Overshoot conditions, both positive and negative, cause the input voltage to range from +2.434V to –0.553V (see the MaxV and MinV measurements in the header of the eye diagram). This overshoot is caused by excess energy in the transition edge that hits the high impedance CMOS input buffer and reflects back to the receiver. Those reflections continue to travel on the transmission line for multiple cycles before finally damping out. Second, note that the jitter measurement in the eye diagram header is measured at 165ps. Contributing to the jitter are the significant overshoot of the waveform and the uncontrolled reflections.

Figure 4: WRITE Cycle Eye Diagram of Unterminated Data Network



Micron's RLDRAM 2 memory offers a low-cost, flexible solution to these problems. By simply setting a bit in the memory configuration register, the system designer can enable the on-die end termination resistor RTT. The effective circuit with the on-die end termination resistor enabled is illustrated in Figure 5.

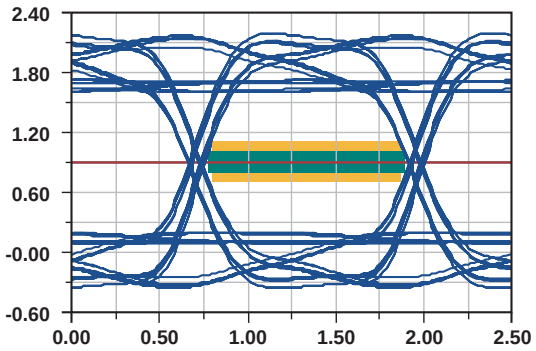
Figure 5: On-Die End Terminated Data Network



Using the same driver, receiver, and transmission line as in the previous example, Figure 6 on page 6 shows the simulation results of this network, including the data eye at the receiver pad.

In Figure 6, the positive and negative overshoot are much better controlled. The on-die end termination resistor absorbs much of the excess energy that was previously reflecting back and forth on the line and causing overshoot problems. This brings the maximum and minimum voltages to +2.186V and –0.359V, respectively. Because the overshoot is better controlled, the jitter measurement is reduced from 165ps to 98ps. Next, compare the width of the data eye or aperture. Without the on-die end termination resistor, the data eye is 1.035ns; with it, the data eye is 1.092ns—a 5 percent increase.

Figure 6: WRITE Cycle Eye Diagram of On-Die, End Terminated Data Network

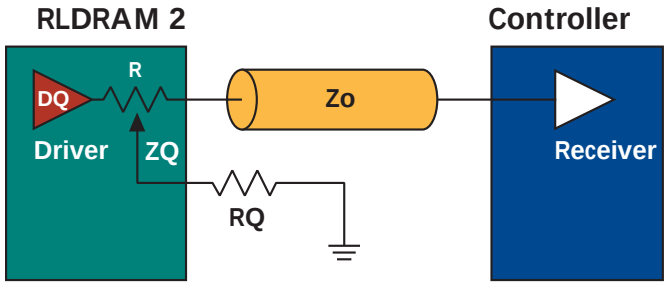


On-Die Source Termination Resistor

The RLDRAM 2 DQ pins also have on-die source termination. The DQ output driver impedance can be set in the range of 25 to 60 ohms. The driver impedance is selected by means of a single external resistor to ground that establishes the driver impedance for all the device DQ drivers. As was the case with the on-die end termination resistor, using the RLDRAM 2 on-die source termination resistor eliminates the need to place termination resistors on the board—saving design time, board space, material costs, and assembly costs, while increasing product reliability. It also eliminates the cost and complexity of end termination for the controller at that end of the bus. With flexible source termination, designers can build a single printed circuit board with various configurations that differ only by load options, and adjust the Micron RLDRAM 2 memory driver impedance with a single resistor change.

To illustrate the effectiveness of the RLDRAM 2 on-die source termination resistor, the same unterminated model is used as before, but the operation changes from a WRITE cycle to a READ cycle. The RLDRAM 2 device becomes the data driver, as shown in Figure 7.

Figure 7: On-Die Source Terminated Data Network



The impedance of the transmission line (Zo) will vary depending on the printed circuit board characteristics, but for this case study, a transmission line impedance of 60 ohms is assumed. If the driver is not properly matched, a waveform like the one shown in Figure 8 is possible.

As before, there are significant overshoot and ringing problems with the Figure 8 waveform. Depending on the particular controller specifications, these voltage levels may exceed device input specifications. However, with the RLDRAM on-die source termination resistor feature, the driver output impedance can be set to better match the transmission line, resulting in the eye diagram shown in Figure 9 on page 8.

Again, in examining key measurements of the data eye, the jitter is below 100ps and the data eye is at 1.100ns, both of which are very good eye measurements. The signal is well controlled for both rising and falling edges, and the overshoot is significantly reduced to within the input design requirements of most controllers.

Figure 8: READ Cycle Eye Diagram of Unterminated Data Network

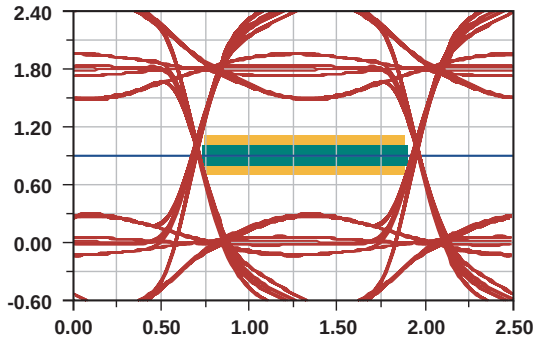
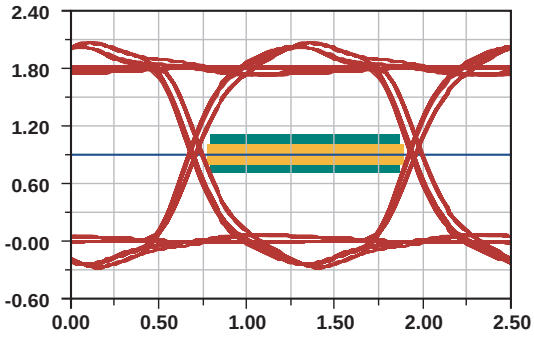


Figure 9: READ Cycle Eye Diagram of Source Terminated Data Network



Conclusion

RLDRAM 2 memory combines performance-critical features to provide both flexibility and simplicity for a wide range of applications. An I/O interface that supports both 1.5V and 1.8V levels, a programmable output impedance, and on-die termination help systems achieve maximum performance. Add to that an innovative eight-bank architecture and separate and common I/O options to help enable high efficiency on the data bus, and the result is an impressive, innovative feature set that makes RLDRAM 2 memory a versatile, high-performance device.

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