

# TECHNICAL NOTE

### DESIGNING IN SDRAM FOR FUTURE UPGRADES

### Introduction

The standard life cycle of a DRAM component is in the order of five years before the market pushes for larger density components. However, with the emergence of new designs, this cycle is becoming less of a concern. Today's SDRAM components are being designed to accommodate a seamless migration to higher densities without product redesign. This is an important aspect to consider as you approach any new design with SDRAM. The two main areas that you need to pay close attention to in your original design to accommodate higher density chips are refresh rate and addressing.

### **Refresh Rate**

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is non-persistent, so it must be issued each time a refresh is required. When designing for higher density upgrades, the refresh requirements must be kept in mind. The internal refresh controller generates the addressing. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 64Mb and 128Mb SDRAM components require 4,096 AUTO REFRESH cycles every 64ms, while the 256Mb and 512Mb SDRAM components require 8,192 AUTO REFESH cycles every 64ms due to the extra row address line for the x4, x8, and x16 configurations. The refresh count on the x32 configurations does not increase to 8,192 until the 512Mb device.

The extra row in the x4, x8, and x16 configurations of the 256Mb and 512Mb SDRAM components causes the distributive refresh rate to be cut in half, from 15.625 $\mu$ s to 7.812 $\mu$ s SDRAM components. Alternatively, at the minimum cycle rate (<sup>t</sup>RFC), the 64Mb and 128Mb components require 4K refresh and the 256Mb and 512Mb require 8K refresh.

The row addressing for the x32 devices differs slightly from the x4, x8 and x16 configurations. The periodic refresh decreases to 7.812µs moving from the 256Mb device to the 512Mb device.

Figure 2: 54-Ball VFBGA

<u>x4</u>	<u>x8</u>	<u>x16</u>				<u>x16</u>	<u>x8</u>	<u>x4</u>
-	-	Vdd	1•	54	П	Vss	-	-
NC	DQ0	DQ0	2	53		DQ15	DQ7	NC
-	-	VDDQ	3	52		VssQ	-	-
NC	NC	DQ1	4	51		DQ14	NC	NC
DQ0	DQ1	DQ2	5	50		DQ13	DQ6	DQ3
-	-	VssQ	6	49		VDDQ	-	-
NC	NC	DQ3	7	48		DQ12	NC	NC
NC	DQ2	DQ4	8	47		DQ11	DQ5	NC
-	-	VddQ	9	46		VssQ	-	-
NC	NC	DQ5	10	45		DQ10	NC	NC
DQ1	DQ3	DQ6	11	44		DQ9	DQ4	DQ2
-	-	VssQ	12	43		VddQ	-	-
NC	NC	DQ7	13	42		DQ8	NC	NC
-	-	Vdd	14	41		Vss	-	-
NC	NC	DQML	15	40		NC	-	-
-	-	WE#	16	39		DQMH	DQM	DQM
-	-	CAS#	17	50		CLK	-	-
-	-	RAS#	18	5,		CKE	-	-
-	-	CS#	19	A12 For 256/512Mb36		NC	-	-
-	-	BA0	20	55		A11	-	-
-	-	BA1	21	5.		A9	-	-
-	-	A10	22	33		A8	-	-
-	-	A0	23	52		A7	-	-
-	-	A1	24	51		A6	-	-
-	-	A2	25	50		A5	-	-
-	-	A3	26	29		A4	-	-
-	-	Vdd	27	28		Vss	-	-

### Figure 1: 54-Pin TSOP

# 1 2 3 4 5 6 7 8 9 A (vss) (Q015) (vss0) (Vs00) (V000) (Q00) (V00) B (D014) (Q013) (V000) (Vs00) (Q02) (D01) C (D012) (D011) (vss0) (Vs00) (Vs00) (Q02) (D01) C (D012) (D011) (vs00) (Vs00) (Vs00) (Q02) (D01) C (D012) (D011) (vs00) (Vs00) (Vs00) (D02) (D01) D (D010) (D09) (Vs00) (Vs00) (D04) (D03) D (D010) (D09) (Vs00) (Vs00) (D04) (D03) E (D03) (NC) (Vs5) (Vs00) (D00) (D07) F (U00M) (CLK) (KE) (Cas) (Ras) (Ras) (Ras) G (A12) (A11) (A9) (A1) (A10) (A1) (A10) J (vs) (A5) (A4)



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### Figure 3: 86-Pin TSOP

<u>x</u> 3	2				x32
VDD DQ00 VDDQ DQ1 DQ2 VSSQ DQ3 DQ4 VDQ5 DQ6 VSSQ DQ6 VSSQ DQ6 VSSQ DQ6 VSSQ DQ6 VSSQ DQ6 VSSQ DQ6 VSSQ BA1 A10 A0 A1 A10 A0 A1 A10 A0 A1 BA0 BA1 DQM2 VDD DQ10 CQ10 CQ10 CQ10 CQ10 DQ10 CQ10 CQ10 CQ10 CQ10 DQ3 DQ4 VDDQ DQ4 DQ5 DQ6 VSSQ DQ10 CQ10 DQ10 DQ5 DQ6 VSSQ DQ10 DQ10 DQ10 DQ5 DQ6 VSSQ DQ10 DQ10 DQ10 DQ10 DQ5 DQ6 VSSQ DQ10 DQ10 DQ10 DQ10 DQ10 DQ10 DQ5 DQ6 VSSQ DQ10 DQ10 DQ10 DQ10 DQ10 DQ10 DQ10 DQ1		1 • 2 3 4 5 6 7 8 9 9 10 11 12 13 14 15 16 17 18 19 20 21 A11 For 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38	86 85 84 83 82 81 80 79 78 77 76 75 74 73 72 71 76 75 75 76 68 67 66 65 64 63 62 64 63 62 61 60 59 58 55 55 55 54 52 51 50 90 50 51 50 50 50 51 50 50 50 50 50 50 50 50 50 50 50 50 50		x32 Vss DQ15 VssQ DQ14 DQ13 VbDQ DQ12 DQ11 VssQ DQ9 VbDQ DQ30 DQ29 VbDQ VbDQ VbDQ DQ30 DQ28 DQ28 DQ28 DQ28 DQ28 VbDQ
	-1			J	

	Figure 4: 90-Ball VFBGA									
	1	2	3	4	5	6	7	8	9	
А	DQ26	DQ24	O Vss				VDD	DQ23	DQ21	
В	DQ28	VDDQ	O VssQ					O VssQ	DQ19	
С	VssQ	DQ27	DQ25				DQ22	DQ20	VDDQ	
D	VssQ	DQ29	DQ30				DQ17	DQ18	VDDQ	
Е	VDDQ	DQ31						DQ16	VssQ	
F	Vss	DQM3	A3				A2		VDD	
G	O A4	A5	<b>A6</b>				A10	A0	A1	
н	A7	A8	O NC/A12	H3 is A1	2 for the			BA1	A11	
J	O CLK	CKE	O A9	512Mb NC in al	x 32 and I others		BAO	O CS#	O RAS#	
К	DQM1						O CAS#	O WE#		
L	VDDQ	DQ8	O Vss					DQ7	VssQ	
М	O VssQ	DQ10	DQ9				DQ6	DQ5	VDDQ	
Ν	O VssQ	DQ12	DQ14				DQ1	DQ3	VDDQ	
Ρ	DQ11	VDDQ	VssQ					⊖ VssQ	DQ4	
R	DQ13	DQ15	O Vss					DQ0	DQ2	
I	L									



### **SDRAM Addressing**

The second design area to consider is addressing. Unfortunately, addressing issues are often overlooked. The most significant design issue to keep in mind is that row and column address lines that are "Don't Care" for the lower density components must be accounted for to migrate to higher density components. An example of this can be found in Table 1, which illustrates the migration path of SDRAM components from 64Mb to 512Mb. You need to pay particular attention on the 256Mb and 512Mb components because they use an extra row address line, A12, which is pin 36 (see Figure 1 and Figure 2). In the lower density parts, pin 36 and pin 40 are No Connect (NC). The number of column address lines also increase as you increase the density of the SDRAM components as seen in Table 1. If the extra address pins are not accounted for, you will see addressing problems as you move to the higher density components. (The problems will manifest in the form of storing data in unknown locations due to floating address lines for the higher density components.) This problem can easily be overcome by tying the higher order address bits, for the lower density applications, to ground during the appropriate command time. For unused columns, pins must be driven to a known, consistent state, either high or low, when writing to the SDRAM component. This procedure will not utilize the entire capacity of the higher density chip, but it will assure that data is allocated to the proper address. The controller can also be designed to use the higher order address lines for the larger chips if you need the extra memory later.

SDRAM DENSITY	ADDRESSING	X4	X8	X16	X32
64Mb <sup>1</sup>	Row	A0-A11	A0-A11	A0-A11	A0-A10
(4 banks)	Column	A0-A9	A0-A8	A0-A7	A0-A7
128Mb <sup>1</sup>	Row	A0-A11	A0-A11	A0-A11	A0-A11 <sup>2</sup>
(4 banks)	Column	A0-A9, A11	A0-A9	A0-A8	A0-A7
256Mb <sup>1</sup>	Row	A0-A12 <sup>3,4</sup>	A0-A12 <sup>3,4</sup>	A0-A12 <sup>3,4</sup>	A0-A11
(4 banks)	Column	A0-A9, A11	A0-A9	A0-A8	A0-A8
512Mb <sup>1</sup>	Row	A0-A12 <sup>3,4</sup>	A0-A12 <sup>3,4</sup>	A0-A12 <sup>3,4</sup>	A0-A12 <sup>5</sup>
(4 banks)	Column	A0-A9, A11, A12 <sup>3,4</sup>	A0-A9, A11	A0-A9	A0-A8

Table 1: SDRAM Addressing

NOTE:

2. Pin 21 goes from NC to A11

3. Refresh goes from 15.625µs per row to 7.8µs per row

4. Pin 36 goes from NC to A12

5. Micron has assigned A12 to pin 69 on the 86-Pin TSOP package



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<sup>1. 54-</sup>pin TSOP (x4, x8, x16) and 86-pin TSOP (x32)