TECHNICAL NOTE

DESIGNING IN SDRAM FOR FUTURE UPGRADES

Introduction

The standard life cycle of a DRAM component is in the order of five years before the market pushes for larger density components. However, with the emergence of new designs, this cycle is becoming less of a concern. Today's SDRAM components are being designed to accommodate a seamless migration to higher densities without product redesign. This is an important aspect to consider as you approach any new design with SDRAM. The two main areas that you need to pay close attention to in your original design to accommodate higher density chips are refresh rate and addressing.

Refresh Rate

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is non-persistent, so it must be issued each time a refresh is required. When designing for higher density upgrades, the refresh requirements must be kept in mind.

The internal refresh controller generates the addressing. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 64Mb and 128Mb SDRAM components require 4,096 AUTO REFRESH cycles every 64ms, while the 256Mb and 512Mb SDRAM components require 8,192 AUTO REFESH cycles every 64ms due to the extra row address line for the x4, x8, and x16 configurations. The refresh count on the x32 configurations does not increase to 8,192 until the 512Mb device.

The extra row in the x4, x8, and x16 configurations of the 256Mb and 512Mb SDRAM components causes the distributive refresh rate to be cut in half, from 15.625µs to 7.812µs SDRAM components. Alternatively, at the minimum cycle rate (^{t}RFC), the 64Mb and 128Mb components require 4K refresh and the 256Mb and 512Mb require 8K refresh.

The row addressing for the x32 devices differs slightly from the x4, x8 and x16 configurations. The periodic refresh decreases to 7.812µs moving from the 256Mb device to the 512Mb device.

Figure 1: 54-Pin TSOP

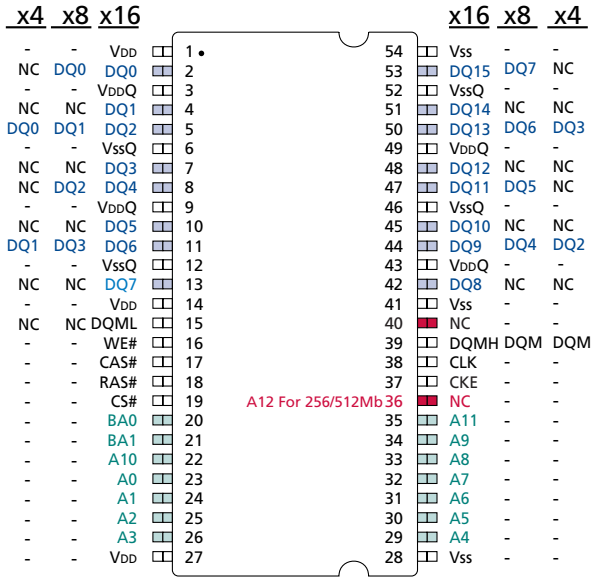


Figure 2: 54-Ball VFBGA

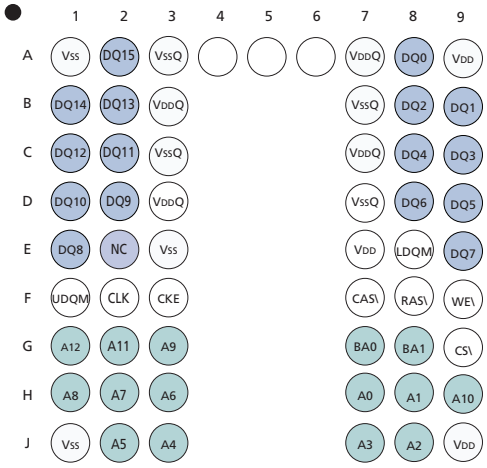


Figure 3: 86-Pin TSOP

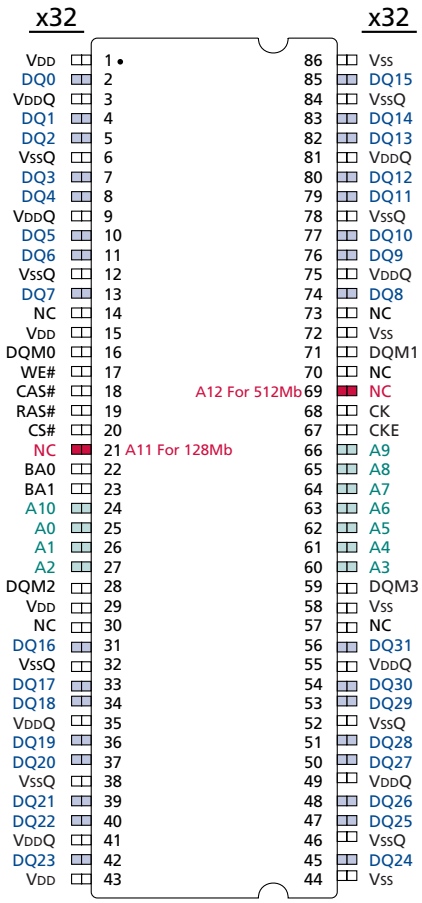
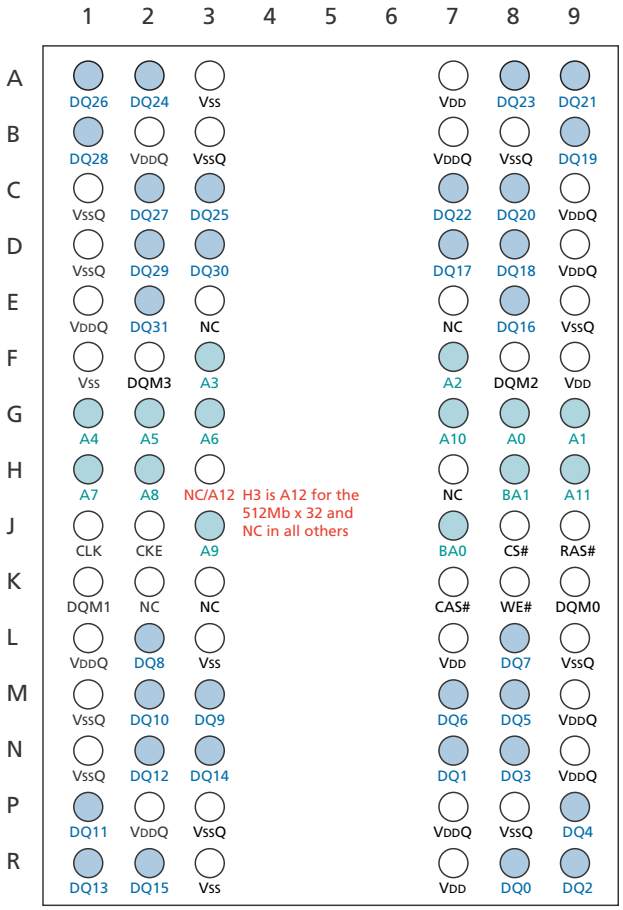


Figure 4: 90-Ball VFBGA



SDRAM Addressing

The second design area to consider is addressing. Unfortunately, addressing issues are often overlooked. The most significant design issue to keep in mind is that row and column address lines that are "Don't Care" for the lower density components must be accounted for to migrate to higher density components. An example of this can be found in Table 1, which illustrates the migration path of SDRAM components from 64Mb to 512Mb. You need to pay particular attention on the 256Mb and 512Mb components because they use an extra row address line, A12, which is pin 36 (see Figure 1 and Figure 2). In the lower density parts, pin 36 and pin 40 are No Connect (NC). The number of column address lines also increase as you increase the density of the SDRAM components as seen in Table 1. If the extra address pins are not accounted for, you will see addressing problems as you move to the higher density components. (The problems will manifest in the form of storing data in unknown locations due to floating address lines for the higher density components.) This problem can easily be overcome by tying the higher order address bits, for the lower density applications, to ground during the appropriate command time. For unused columns, pins must be driven to a known, consistent state, either high or low, when writing to the SDRAM component. This procedure will not utilize the entire capacity of the higher density chip, but it will assure that data is allocated to the proper address. The controller can also be designed to use the higher order address lines for the larger chips if you need the extra memory later.

Table 1: SDRAM Addressing

SDRAM DENSITY	ADDRESSING	X4	X8	X16	X32
64Mb[1] (4 banks)	Row	A0-A11	A0-A11	A0-A11	A0-A10
	Column	A0-A9	A0-A8	A0-A7	A0-A7
128Mb[1] (4 banks)	Row	A0-A11	A0-A11	A0-A11	A0-A11[2]
	Column	A0-A9, A11	A0-A9	A0-A8	A0-A7
256Mb[1] (4 banks)	Row	A0-A12[3,4]	A0-A12[3,4]	A0-A12[3,4]	A0-A11
	Column	A0-A9, A11	A0-A9	A0-A8	A0-A8
512Mb[1] (4 banks)	Row	A0-A12[3,4]	A0-A12[3,4]	A0-A12[3,4]	A0-A12[5]
	Column	A0-A9, A11, A12[3,4]	A0-A9, A11	A0-A9	A0-A8

NOTE:

1. 54-pin TSOP (x4, x8, x16) and 86-pin TSOP (x32)
2. Pin 21 goes from NC to A11
3. Refresh goes from 15.625µs per row to 7.8µs per row
4. Pin 36 goes from NC to A12
5. Micron has assigned A12 to pin 69 on the 86-Pin TSOP package

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