

Technical Note

DDR2 SODIMM Optimized Address/Command Nets

Introduction

DDR2 small-outline dual in-line memory modules (SODIMMs) have several basic module configurations and a number of complex topologies. Operating speeds range from PC2-3200 through PC2-6400 with module configurations including single-rank, dual-rank, planar, stacked, x8-, and/or x16-based designs. Due to the significant assortment of DDR2 SODIMM options, it was imperative to optimize the module address and command bus structure for both performance and compatibility, particularly with regard to mixed loading of configurations.

The purpose of this document is to provide the system-level designer with an overview of the DDR2 SODIMM family and offer insight into termination techniques utilized on the commands and addresses for these modules. Note that the clock nets and data bus structure are also critical but are more of a point-to-point topology and, thus, much simpler to optimize. As such, this technical note will focus on the command and address structure, ultimately equipping the system-level designer with the knowledge needed to properly support the full breadth of DDR2 SODIMM memory options.

JEDEC-Defined Raw Cards

The Joint Electron Device Engineering Council (JEDEC) has defined a full range of module configurations that generate a standardized base for all DDR2 SODIMMs. There are primarily four types of cards: the single-rank module built with x8 DRAM; the single-rank module built with x16 DRAM; the dual-rank module built with x8 DRAM; and the dual-rank module built with x16 DRAM. See Table 1 on page 2 for a detailed listing.

These cards have been designed to work in a single-channel, dual-slot memory system with either one or many of the two cards populated. Memory simulations assume the controller to be approximately 4,900 mils from the first SODIMM, the second SODIMM to be within 600 mils from the first SODIMM, and a 50-ohm termination to V_{TT} within 370 mils. $V_{TT} = V_{DDQ}/2$. See Figure 1 on page 2.

Figure 1: Typical Single-Channel, Dual-Slot DDR2 Motherboard Topology

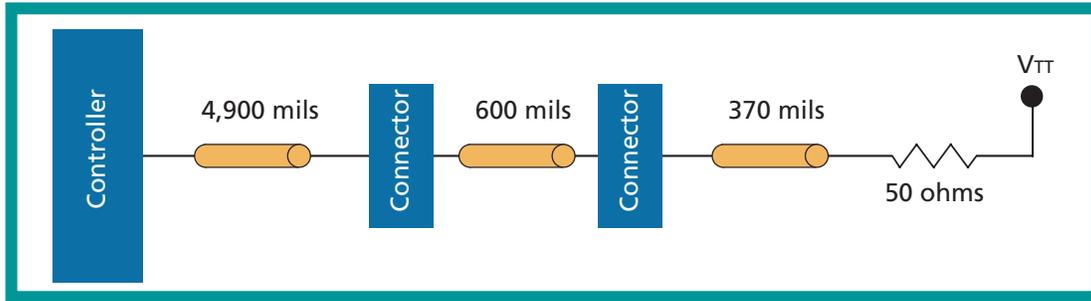


Table 1: JEDEC-Defined Base Reference Designs

Card Identifier	Module Ranks	Number of DRAM	DRAM Configuration	Package
Raw Card A	Dual	8	x16	Planar
Raw Card B	Single	8	x8	Planar
Raw Card C	Single	4	x16	Planar
Raw Card D	Dual	16	x8	Stacked
Raw Card E/F	Dual	16	x8	Planar

Evaluation of the Bus Structure

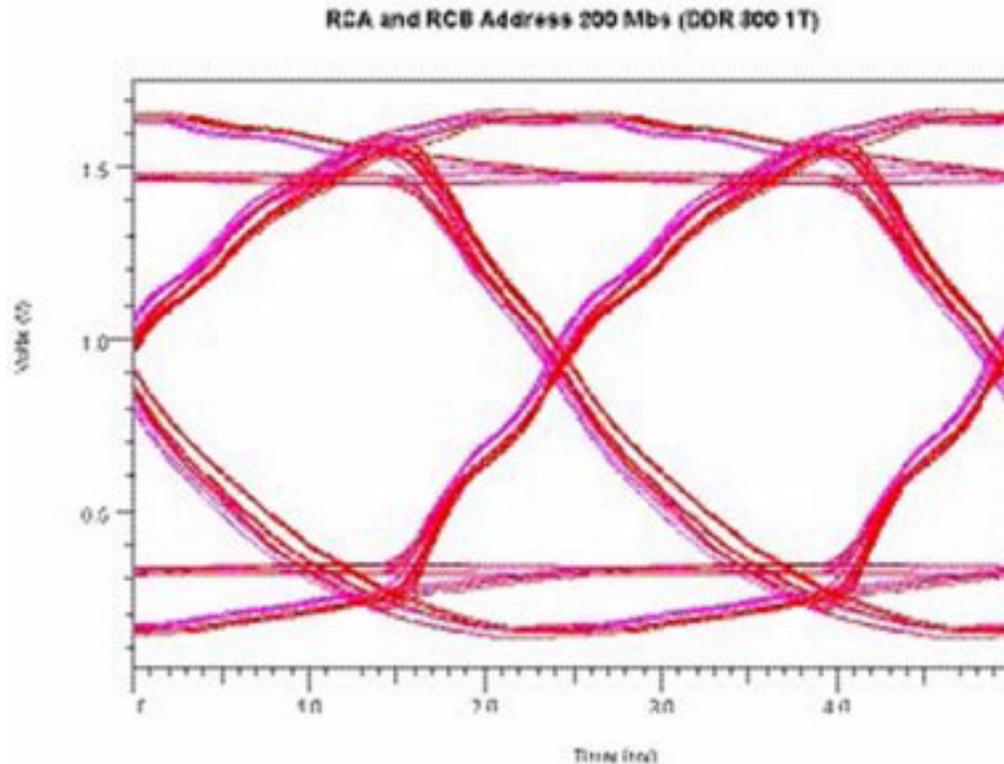
Each of the raw card designs has a series resistor positioned directly at the card edge connector on the module. Through simulation, this “stub” resistor has shown to help isolate reflections in a standard unbuffered notebook system where more than one memory module is used. In fact, to perform correctly, this stub resistor is an absolute requirement for the complex DDR2 multi-drop buses.

With the aid of simulation, we can see that the stub resistor actually performs two functions. Primarily, it isolates modules from each other. Secondly, it acts as a wave-shaping resistor between the driver and the receiver. Simulation from any single module shows that as the resistor value is increased the edges become slower, resulting in a smaller aperture. The increase in resistor value also generally reduces jitter.

Equally important is symmetry of the routed channel to ensure robust signal integrity. This is especially necessary where two memory modules need to be interchangeable in a dual-slot environment. Ideally, each memory module will have exactly the same number of devices (or loads) to balance between the modules and minimize reflections (or resonance) on the bus. When the resonance gets very bad, the result is usually non-monotonic signaling and a reduction of slew rates.

There are at least six raw card types defined by JEDEC, and the cards are somewhat different in topologies and loads. This original mixture of cards combined with their individual effects on each other could have contributed to inconsistent timing windows and possible system failures.

Figure 2: RCA/RCB Eye Diagram



Optimization of RCA, RCB, and RCC

The topologies for raw card A (RCA) and raw card B (RCB) address and command nets were designed with symmetrical routing. Both of these designs have address and command nets routed to eight individual memory devices, and both utilize a 3-ohm stub resistor. From a signal integrity perspective, they look very similarly matched. See Figure 2. As expected, when either of these two cards was originally simulated with the raw card C (RCC), resonance problems were seen.

The RCC also utilized a 3-ohm resistor but only had four loads, so the loads are not balanced between the two cards. To overcome the loading mismatch between the cards, additional trace length was added to the address nets of RCC. This accomplished two tasks: first, the extra trace length looks capacitive in nature, so it makes the card look more like RCA and RCB from a loading perspective; second, the timing of the RCC receivers is shifted in time to again make RCC look more like RCA and RCB. This is good from most system performance perspectives, as the four-memory-load module timing now looks very similar to the eight-memory-load module timing. The end result is that the RCC module closely matches the RCA and RCB modules electrically, which makes all three now interchangeable. See Figure 3 on page 4.

Figure 3: RCA and Optimized RCC Eye Diagram

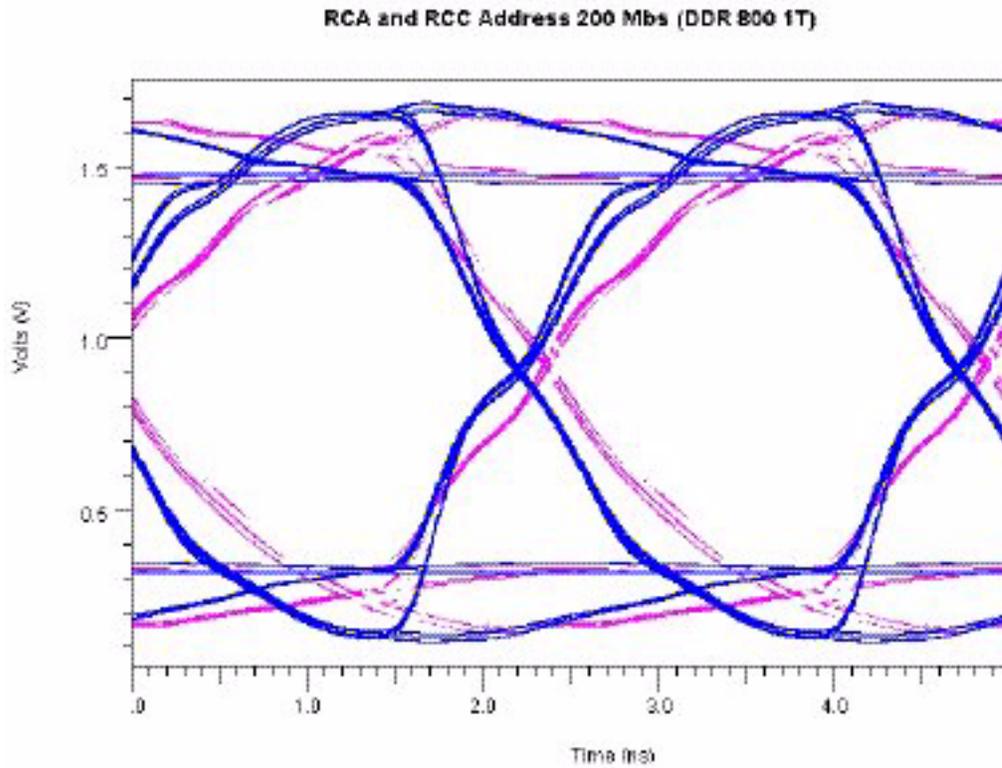
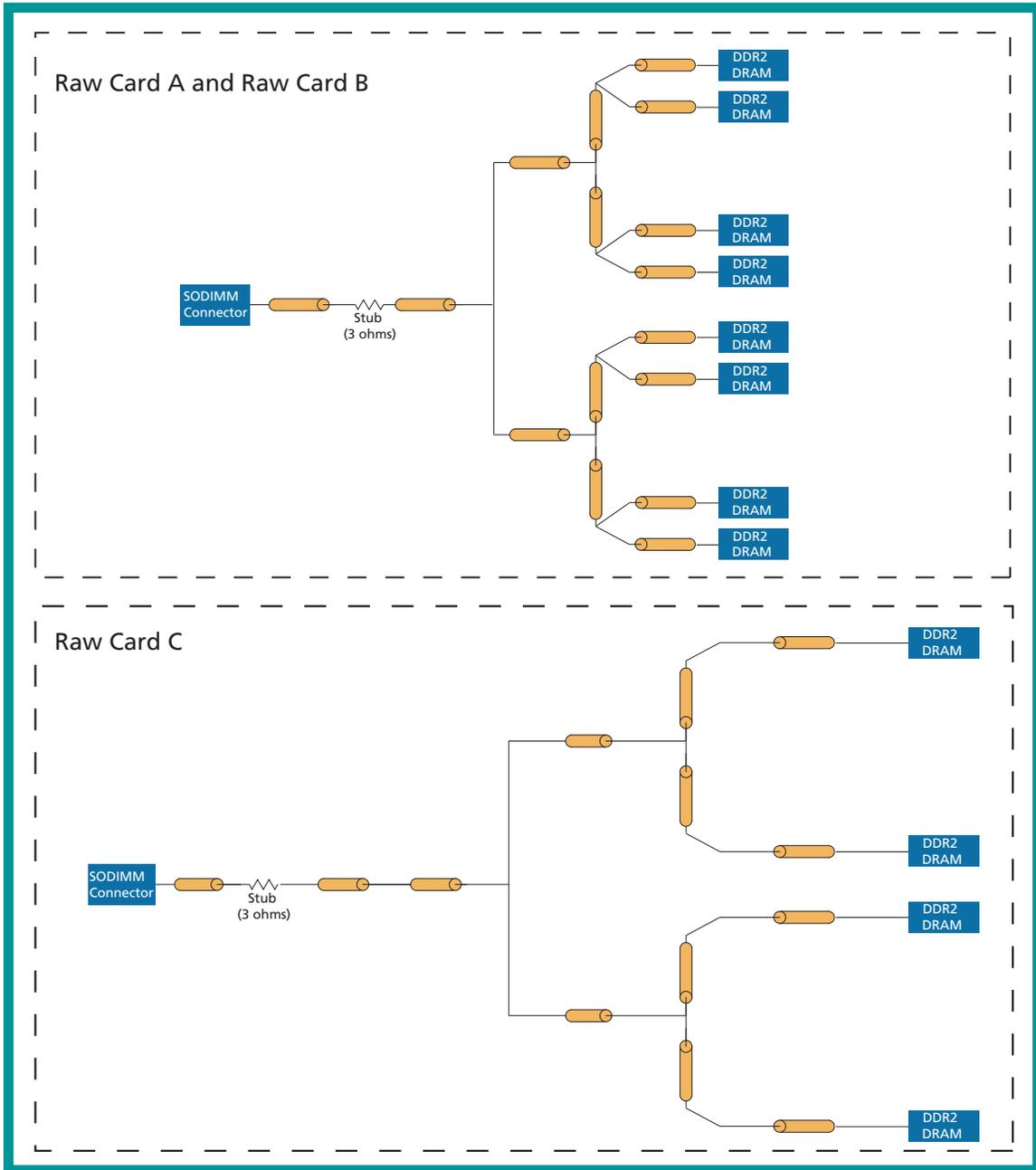


Figure 4: Address and Command Topology for RCA, RCB, and RCC



- Notes:
1. All trace impedances are 60 ohms.
 2. Raw card A uses x16 DRAM.
 3. Raw card B uses x8 DRAM.
 4. Raw card C uses x16 DRAM.

Optimization of RCD

Typically, the first generations of ultra-high-density modules require the use of DRAM stacking or other methods to increase the module density beyond the density of the DRAM currently available. For this purpose, raw card D (RCD) has been created. Raw card D greatly increases the complexity level because it contains sixteen DRAM in a two-rank configuration. See Figure 7 on page 9. With the high number of loads, the stub resistor value should be very small empirically. Simulation demonstrated that a small stub resistor provided a greater aperture size when a single RCD module was utilized. However, when running at higher frequencies mixed with any of the other raw cards in the first slot, RCD loading resonances reduce margin. See Figure 5 on page 7.

Evaluation of the combined structure (RCD mixed with any other raw cards) strictly from the point of energy distribution indicated the RCD card needed a larger stub resistor value to block the energy going to the RCD, which allows more energy for the more lightly loaded modules. See Figure 6 on page 8. It was found that in a mixed environment, a 10-ohm resistor value on RCD improved the aperture size on RCC by about 1,000ps–2,500ps (depending on driver strength). When two RCD cards were placed together, the larger resistor reduced the aperture slightly (approximately 100ps for every 2.5 ohms of increase). The driver strength plays an important role when the channel is so heavily loaded. To ensure good edge rates and apertures with optimal margins, it is desirable to use a stronger driver if two RCD cards are utilized simultaneously.

Figure 5: Less than Optimal Eye (RCC with 10 ohms, RCD with 3 ohms)

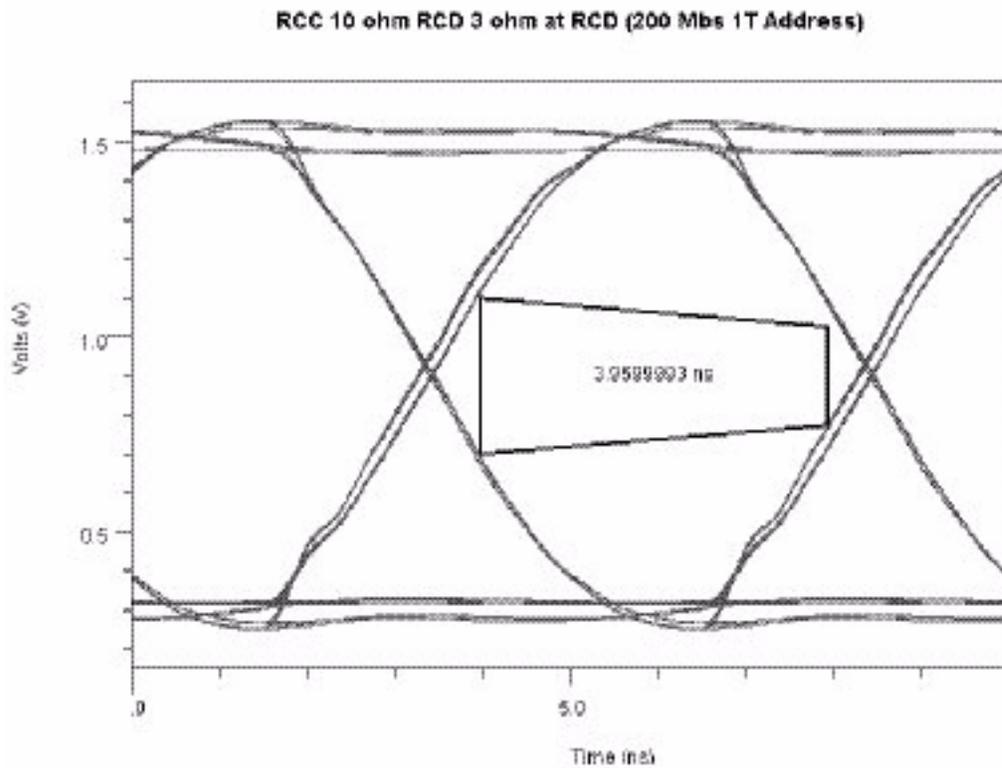
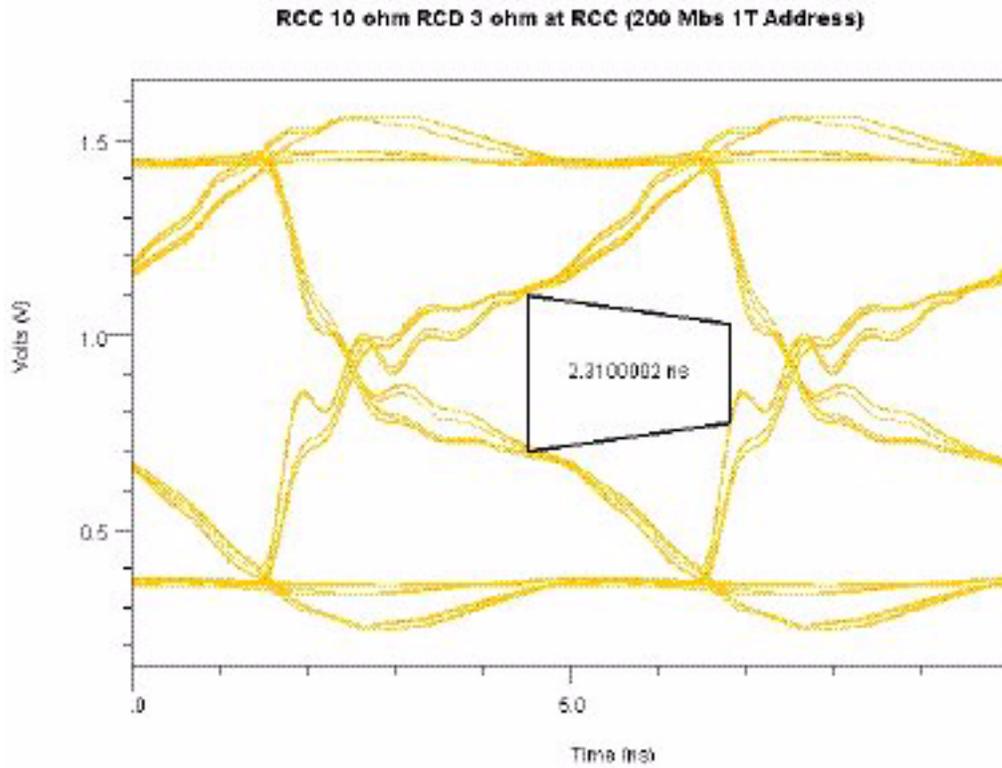


Figure 6: Good Eye (RCC with 3 ohms, RCD with 10 ohms)

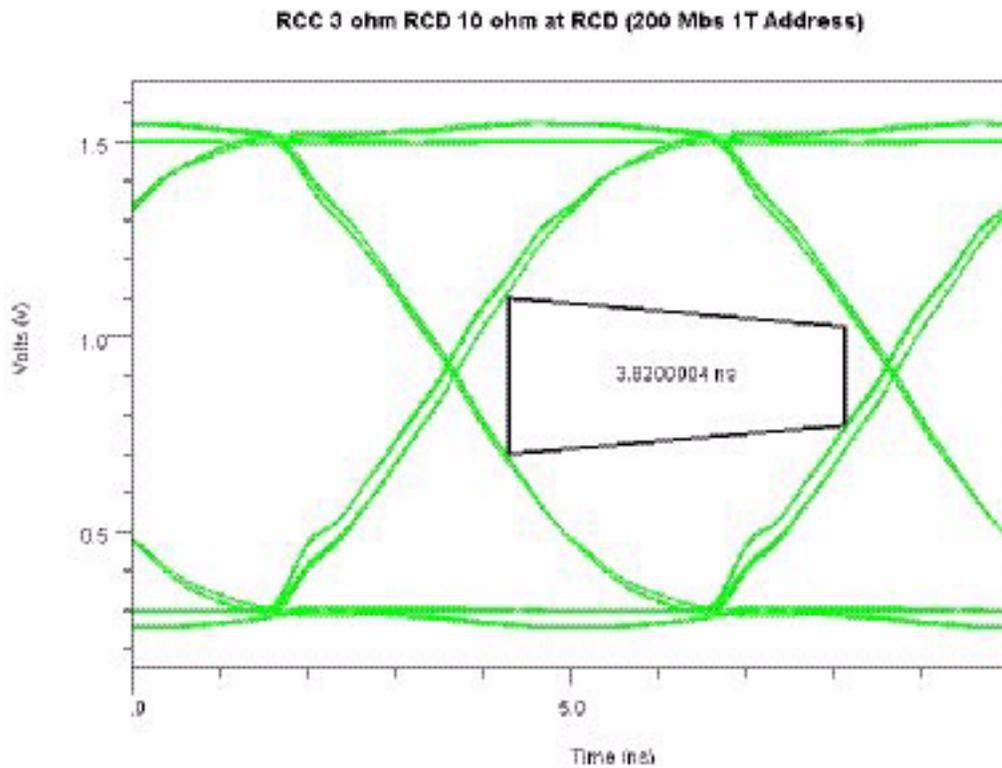
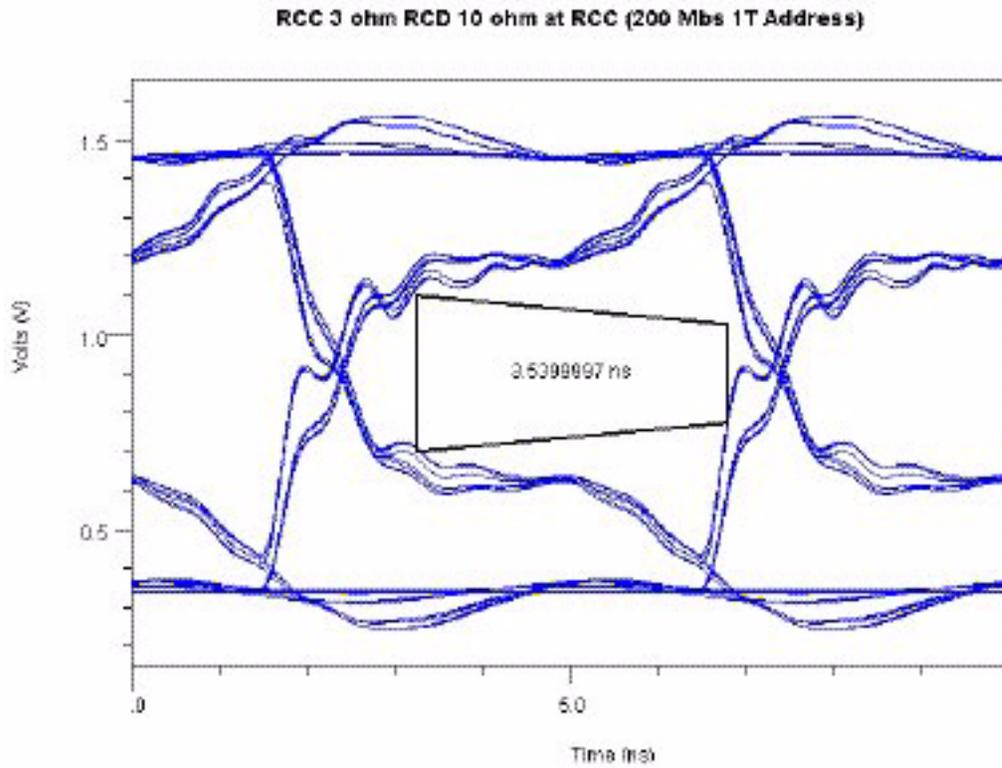
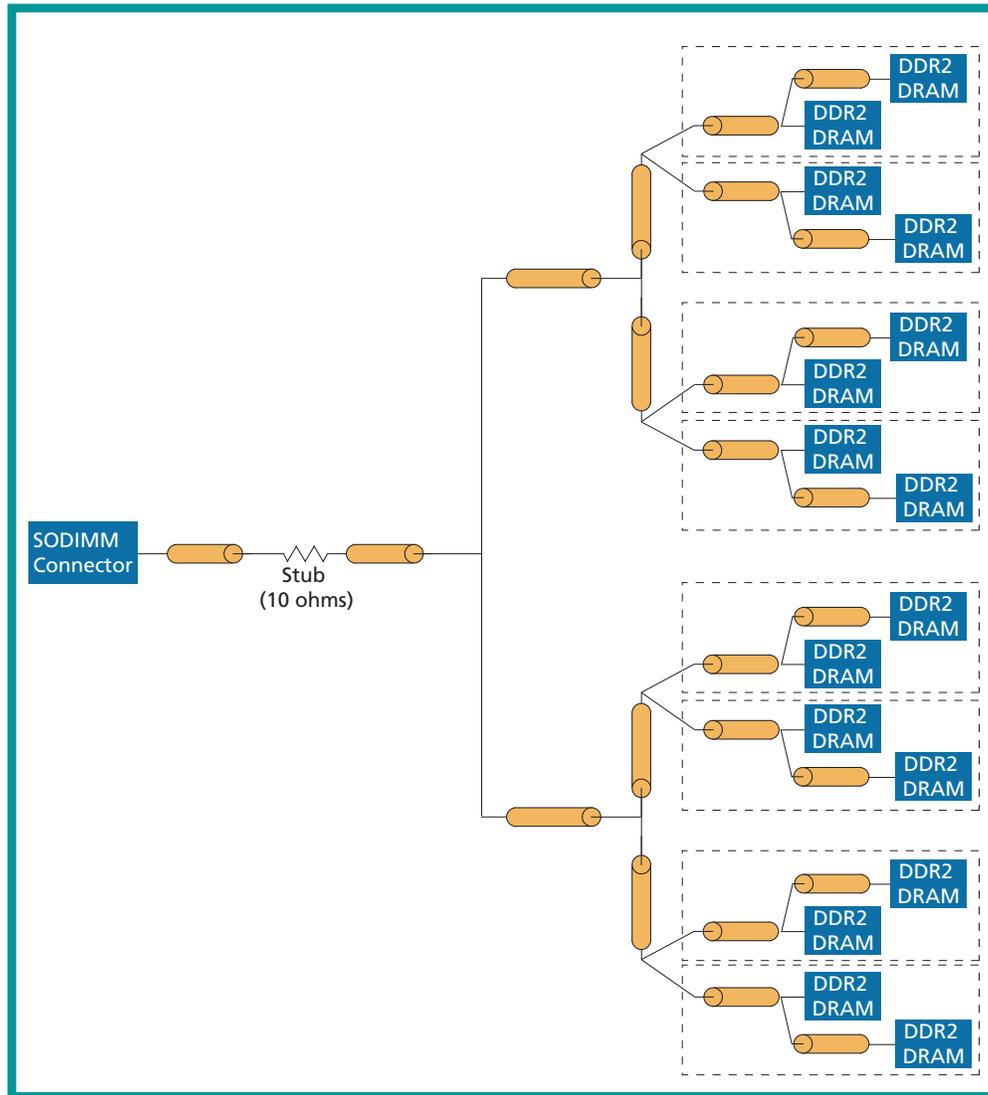


Figure 7: Address and Command Topology for RCD



- Notes: 1. All trace impedances are 60 ohms.
- 2. Raw card D uses x8 DRAM (stacked).

Adding in RCE and RCF

Raw card E (RCE) and raw card F (RCF) are not symmetrical, but are very similar to RCD performance-wise. RCE and RCF are planar solutions, whereas RCD is a stacked solution. These planar solutions also utilize a 10-ohm stub resistor.

Conclusion

DDR2 SODIMMs are much better matched than modules of previous technology. The advantages of using the smaller stub resistor with the lighter loaded card and the larger stub resistor with the heavier loaded card are significant. This technique greatly reduces the resonance problems created by loading conditions from mismatched modules with little or no loss in timing margins. Resonances at all frequencies have not been completely eliminated, but the frequency distribution analysis provides adequate informa-

tion to show the solution is very good up to around 500 MHz–600 MHz, which is well above any 1T DDR2 addressing frequencies. Also significant are the improvements made by utilizing very balanced tree structures on the modules themselves.

Ultimately, the module topology and stub resistor combinations should provide an effective solution for DDR2 SODIMM system performance for single- and dual-slot module systems.



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