Technical Note

DDR2 Package Sizes and Layout Requirements

Introduction

DDR2 breaks new ground in many areas, including its creativity in packaging solutions. This new technology will be offered in several configurations with many new densities. DDR2's life expectancy is predicted to span several generations of DRAM process technology, and a majority of memory users would like to see a trend that moves toward smaller package sizes. Therefore, the Joint Electron Device Engineering Council (JEDEC) has defined a packaging guideline that enables optimal packaging solutions over the complete life span of DDR2 products.

Board Layout: What Board Designers Must Know

Previous DRAM technology supported x16, x8, and x4 in one common footprint for TSOP or FBGA. Under the old paradigm, each of the densities and configurations on DDR1 was compatible with the "single standard" 66-pin TSOP package—this held true on the standard 60-ball FBGA package as well. The electrical array accommodated all densities and configurations. The 4x and x8 configurations were a subset of the x16 configuration, which made this work particularly well. (See Figure 1 on page 2.) This allowed the board designer to utilize one common footprint for all densities and configurations.

DDR2's x16 device has a different ballout from the x4/x8 array. The early DDR2 x16 package may include up to 92 balls, but the x4/x8 package might only have 60 balls with a different ball array. Therefore, in order to be compatible with all vendors, densities, and future package options, it is absolutely critical for the designer to understand both the complexity of the new DDR2 devices and the multiple layout combinations.

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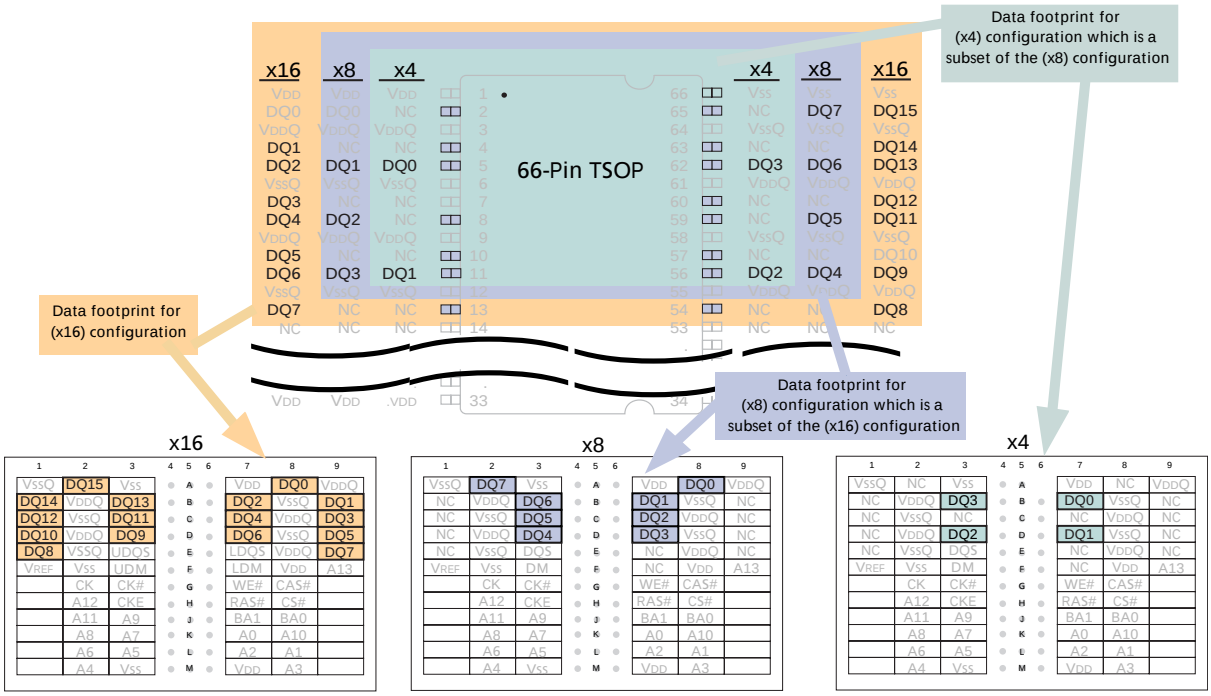
Figure 1: Generic DDR1 Package Solution



60-Ball FBGA (Top View)

Note: For DDR1, all densities and all configurations utilize the same footprint: 66-pin TSOP or 60-ball FBGA.

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DDR2 Packages: Defined by JEDEC

Unlike previous memory technologies, all DDR2 devices will be offered only in FBGA packages, and there are different ball assignments for the different packages. JEDEC has defined larger package sizes with support balls for the earlier DDR2 product densities and smaller package outlines without support balls for a future migration path. This technical note identifies the different package families and electrical connections critical to the layout aspects of DDR2. Additionally, it discusses the common landing pattern (CLP)—a pad array that can accommodate the footprints for all JEDEC-approved DDR2 devices.

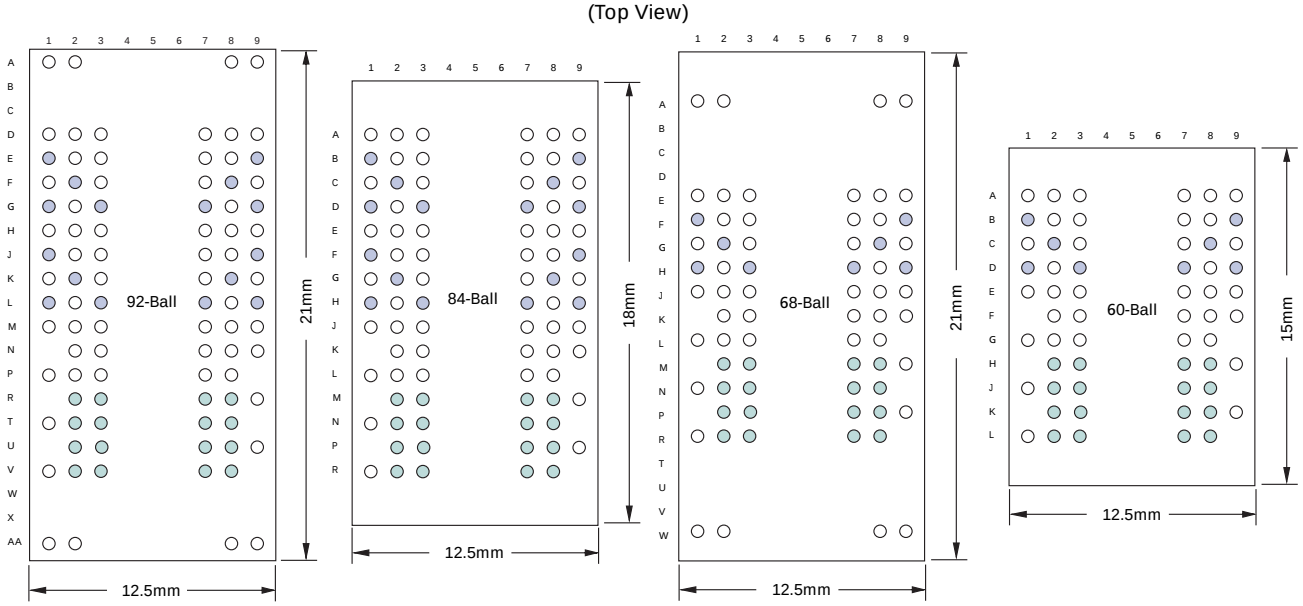
Ball Grid Arrays and Package Sizes

Within the working committees of JEDEC there have been four primary package variations defined for DDR2 SDRAM. The comprehensive sets of drawings are available at www.jedec.org. Access the drawings through JEDEC > JC-11 committee > MO-207 profile.

These four variations include two families of packages—one set with support balls (outrigger balls) that allows for a maximum package size of 21mm x 12.5mm and one set without support balls that advocates smaller footprints. See Figure 2 for simplified ball arrays and package variations.

Before beginning any DDR2 board layout work, the designer must identify the target devices and determine how this may affect placement and routing. If more than one configuration, vendor, or density might be utilized, the package size could vary greatly and additional landing pads may be required. Figure 3 on page 4 illustrates the common landing pattern in use with a variety of package options.

Figure 2: Variations of the MO-207 DDR2 Packages



Package (MO-207) Variation	DL-z	DK-z	DM-z	DJ-z
Number of Total Balls	92	84	68	60
Number of Support Balls	8	0	8	0
Maximun Size in mm (L x W)	21 x 12.5	18 x 12.5	21 x 12.5	15 x 12.5

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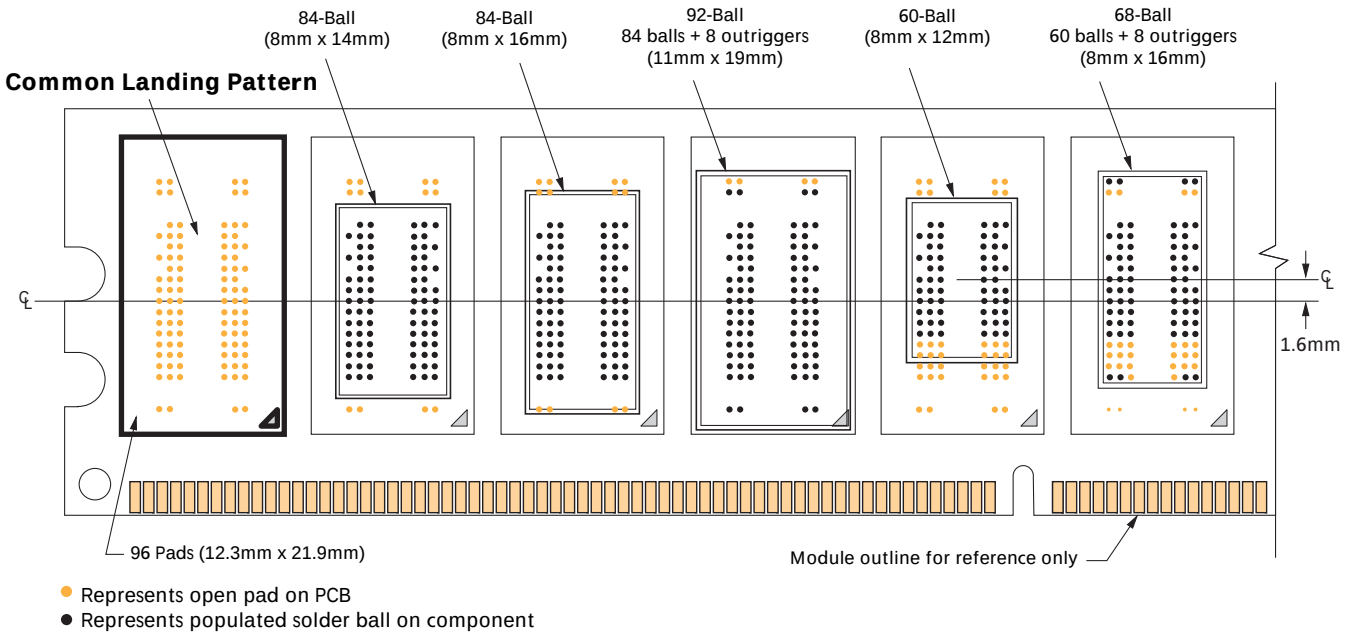
Figure 3: Example Placements of Typical Packages Sizes on the CLP



Note: The 60-ball and 68-ball packages are offset by +1.6mm in the x-direction.

Understanding the Ball Array

The optimal device package would be very small with the least amount of electrical connectors/solder balls possible. However, due to larger DDR2 die sizes of the first density, this may not be achievable. The first generations of higher density parts typically have a larger die size and may require the package with outrigger balls.

In the x16 configuration with a package size larger than 18mm x 12.5mm, two outrigger balls have been added to each corner of the array. This provides the required mechanical strength to securely mount the device to the PCB. Generally, if the overhang of the package is over 3mm, support balls are recommended. (Refer to Table 1 on page 5 for DDR2 maximum package dimensions.)

The electrical array of the 84-ball package is identical to that of the larger 92-ball device but without the outriggers, ensuring a smooth transition to smaller packages because routing changes are unnecessary. Figure 4 on page 5 shows the compatibility of these two (x16) packages.

Likewise, for the x4/x8 package there are two options, one with support balls and one without support balls. The larger 68-ball package for the x4/x8 configuration, which includes outrigger balls and has the same electrical array as the smaller 60-ball package. See Figure 5 on page 6 for more details.

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Table 1: DDR2 Package Dimension (mm)

Package	Length	Width	Comment
	Max	Max	
92-Ball (DL-z)	21	12.5	Includes support balls
84-Ball (DK-z)	18	12.5	
68-Ball (DM-z)	21	12.5	Includes support balls
60-Ball (DJ-z)	15	12.5	

Note: Though the MO-207 document allows a maximum package width of 12.5mm, most JEDEC-based module designs only support a maximum package width of 12.3mm.

Figure 4: Pad Layout and Comparison of 92-Ball (DL-z) vs. 84-Ball (DK-z) Components Only

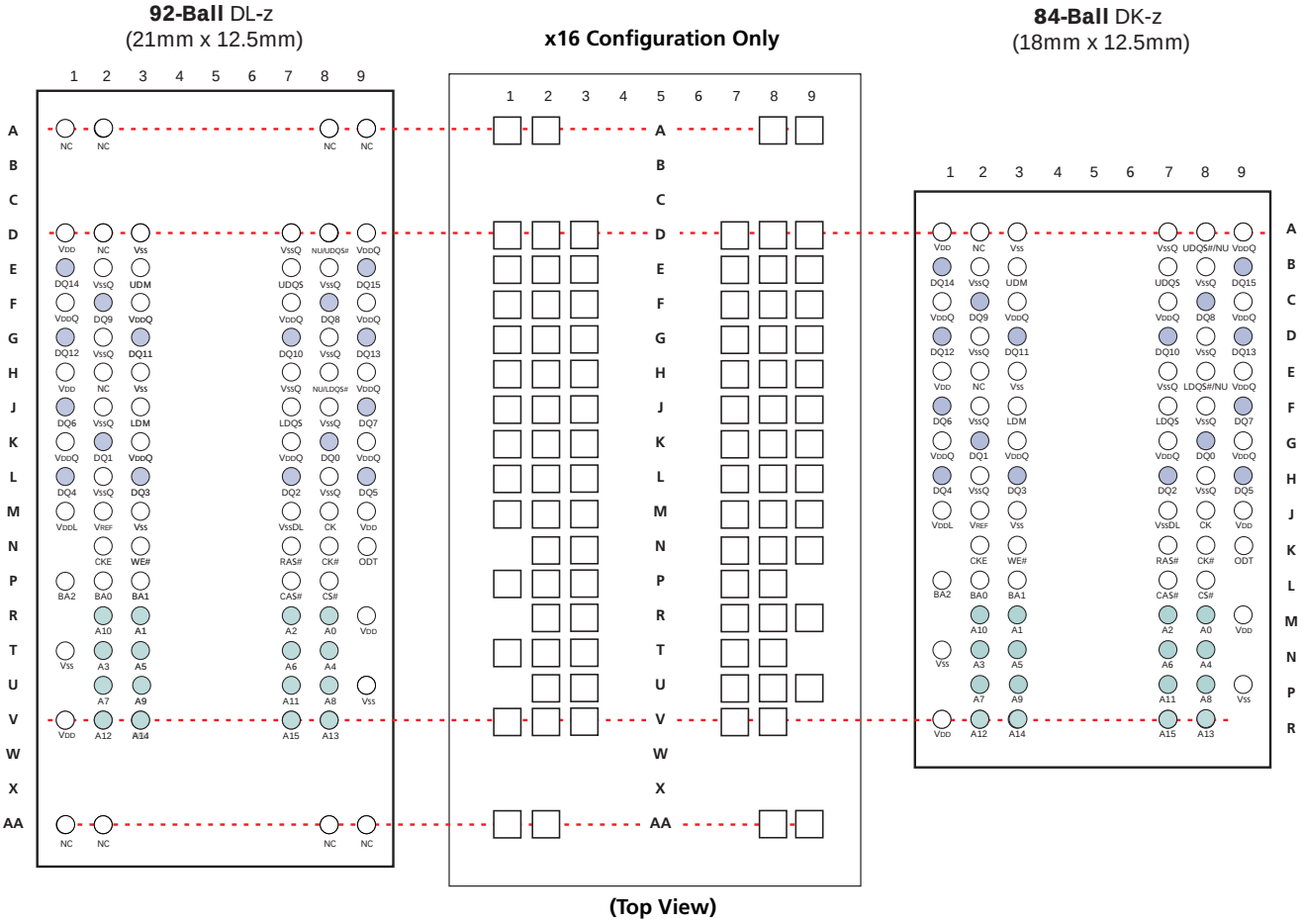

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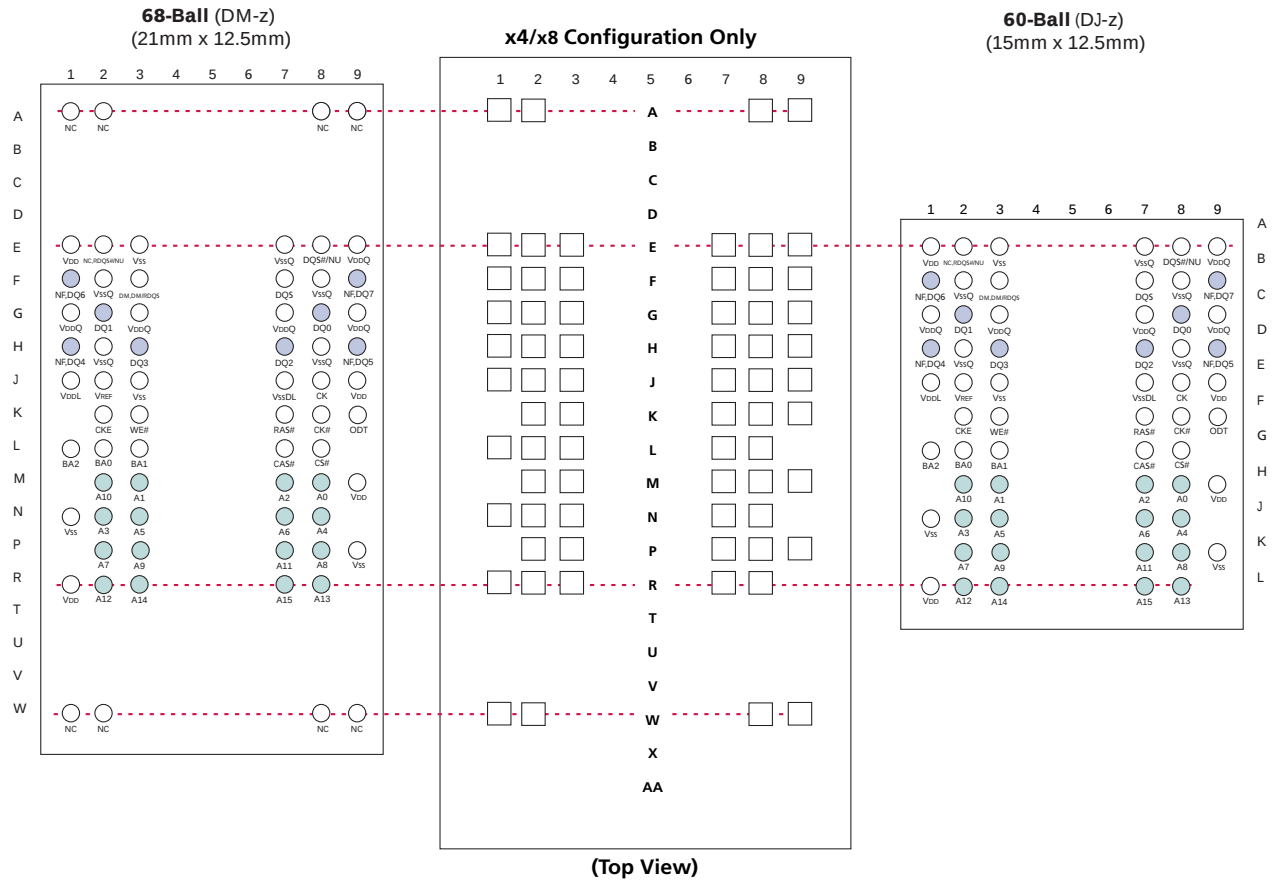
Figure 5: Pad Layout and Comparison of 68-Ball (DM-z) vs. 60-Ball (DJ-z) Components Only



Common Landing Pattern

Layout Compatibility

At first glance, it appears that all packages and all ball arrays are very similar, and routing should be easy as long as it is designed for the worst-case x16 configuration. However, if the board design has been routed for a 92-ball array, the 84-ball array will fit by default; likewise, if the design is routed for a 68-ball array, the 60-ball array will fit. A layout that needs to accommodate all packages and all configurations requires a special landing pattern with additional pads.

Dimensional Requirements

JEDEC has defined a common landing pattern (CLP) for use with the standard modules. Currently, there are two variations which support the different component length requirements—the SODIMM/UDIMM and the RDIMM solution. The SODIMM/UDIMM version allows for a slightly longer package size than the RDIMM option.

These two variations of the CLP provide layouts that accommodate most vendors, densities, and configurations for DDR2 components.

The SODIMM/UDIMM CLP accepts x4, x8, and/or x16 components up to 21mm in length.

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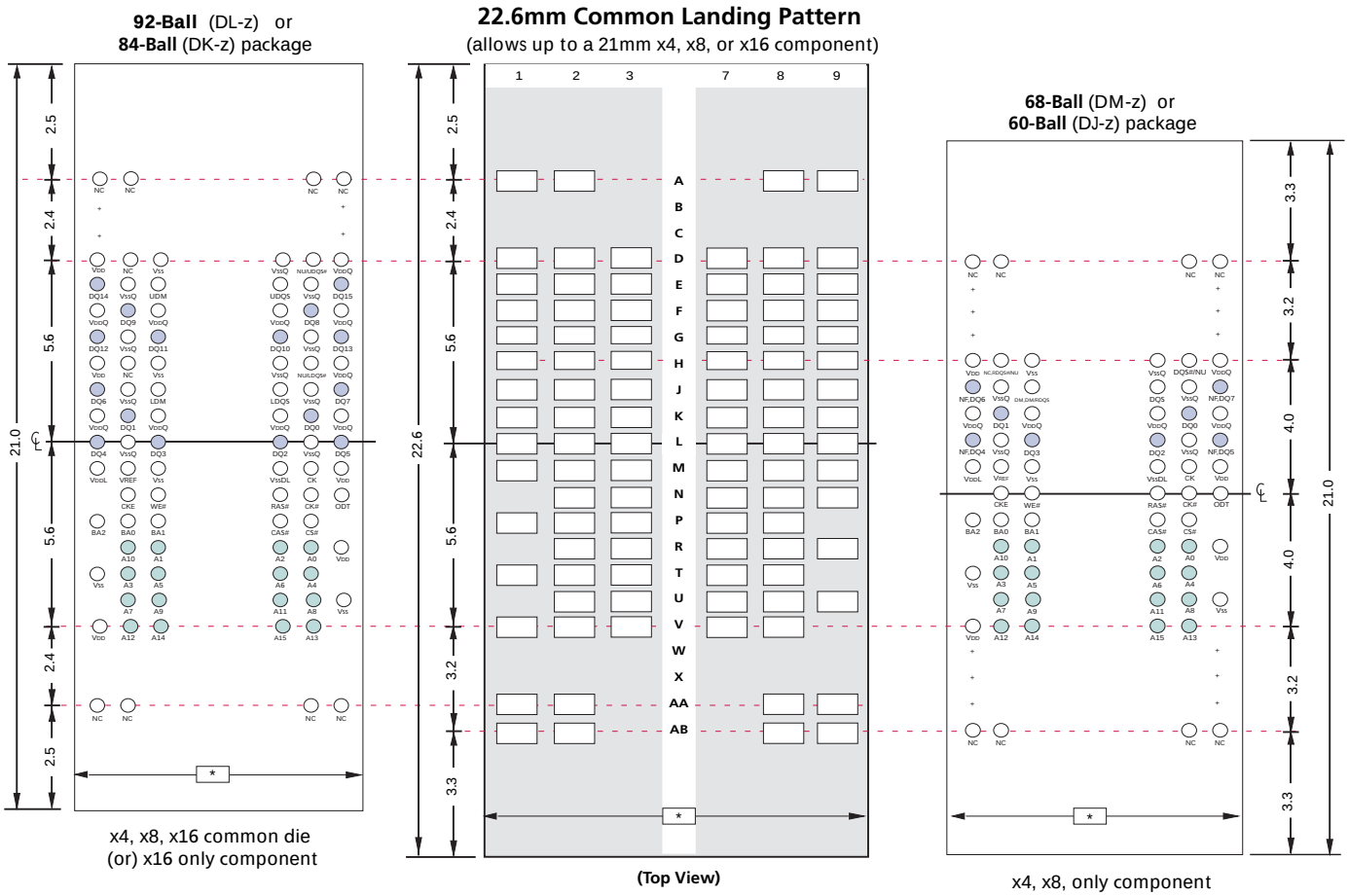
The RDIMM CLP allows a 21mm x4/x8 component, but only 19.6mm for x16 components. Due to module space constraints, both have a maximum package width of 12.3mm.

Figure 6 and Figure 7 reflect the dimensional aspects of the CLP as utilized on the JEDEC SODIMM/UDIMM and RDIMM standard gerber files.

Figure 6: UDIMM/SODIMM's CLP – Overall Dimensions



Notes: 1. Width dimensions are not to scale but have a 12.3mm maximum.
2. The x16 package is aligned to the top and the x4/x8 is aligned to the bottom of the CLP.

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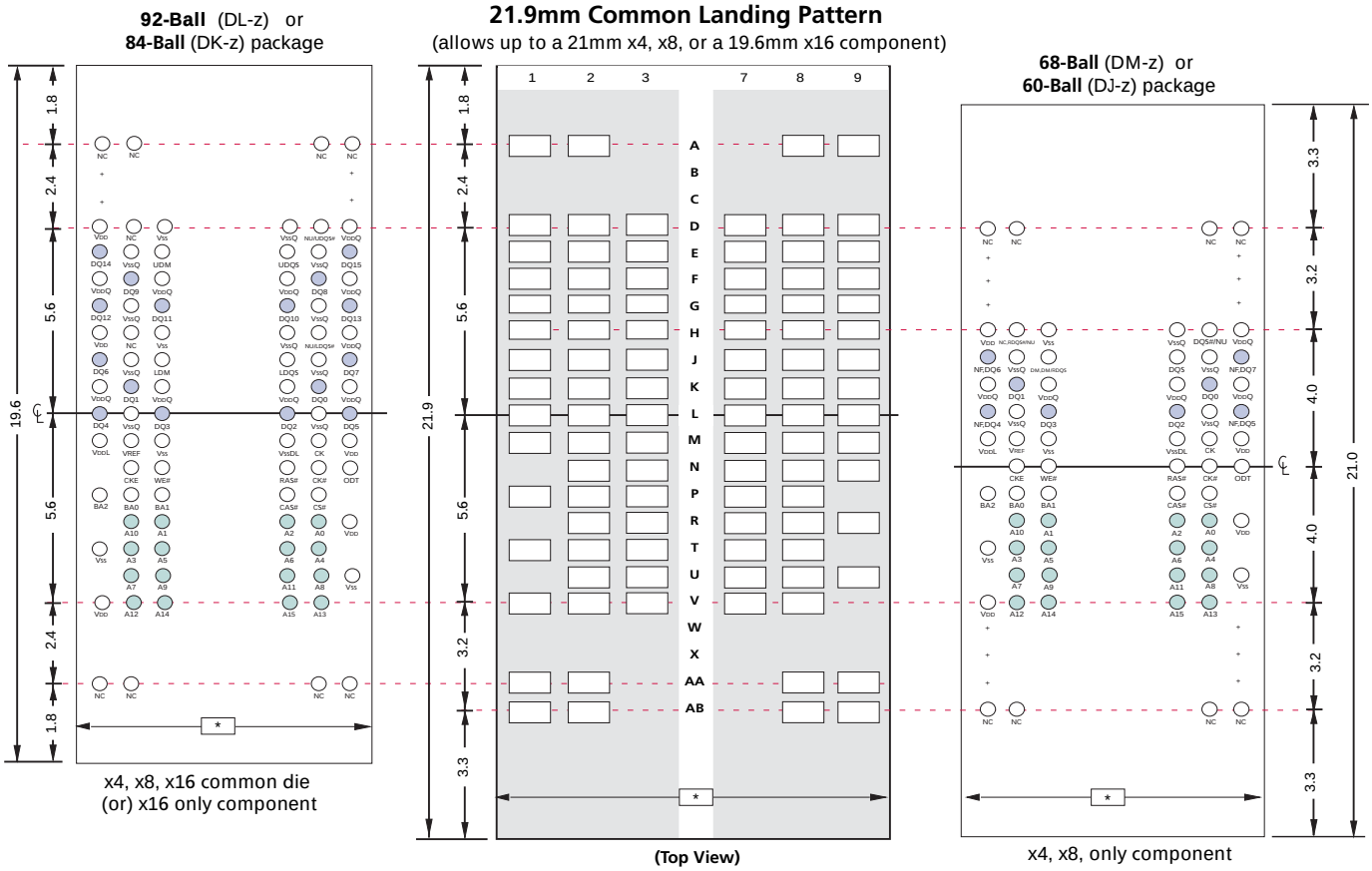
Figure 7: RDIMM's CLP – Overall Dimensions



Notes: 1. Width dimensions are not to scale but have a 12.3mm maximum.
2. The x16 package is aligned to the top and the x4/x8 is aligned to the bottom of the CLP.

Electrical Requirements

It is very important to realize that due to different electrical arrays, each package option has more or less rows. Because of this, the row identification of the CLP may not match that of each individual device variation. For example, pad M7 in the CLP is VssDL, but ball M7 on the 84-ball package is address A2. To simplify simulation when using the Micron IBIS models, the board designer has the option of utilizing the nomenclature for the device (M7 = address A2) or the nomenclature of the CLP (M7 = VssDL).

As a solution, the CLP incorporates all pads from all ball arrays (x4, x8, and x16), including those with or without the outriggers. This means that a 96-pad array, for example, can accommodate any of the four package types. See Figure 8 on page 9.

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Figure 8: Exploded View of Electrical Pattern of CLP

The electrical array of the CLP exists within row D through row V, and the outrigger pads are located at rows A, AA, and AB. For the x16 option, rows D, E, F, and G provide the upper data byte; for the x4/x8 options, the pads on rows E, F, and G are no connects (NC), and row D provides additional power/ground pins.

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Table 2: Multifunctional Pads on the CLP

CLP Pad Location	Pad Usage		
	x4	x8	x16
E1, E9, F2, F8, G1, G3, G7, G9	NC	NC	DQ8–DQ15
J1, J9, L1, L9	NF	DQ4–DQ7	DQ4–DQ7
H2	NU	RDQS	NC
J3	DM	RDQS#	LDM
E3	–	–	UDM
E7	–	–	UDQS
D8	NC[1]	NC[1]	UDQS#
E2, E8, F1, F3, F7, F9, G2, G8	–	–	Supply

Notes: 1. NC on 68-ball package, not applicable on 60-ball package.

When a 68-ball package is placed on the CLP, it is important to note that there are two outrigger balls (A1 and A9) that may be connected to supply pads on the CLP (D1 and D9).

See Table 3 and Figure 9 below for a detailed example.

Table 3: Special-Use Pads on the CLP (by package type)

CLP Pad Location	Pad Usage			
	92-Ball (DL-z)	84-Ball (DK-z)	68-Ball (DM-z)	60-Ball (DJ-z)
D1	VDD	VDD	NC	Not Applicable
D9	VDDQ	VDDQ	NC	Not Applicable

Figure 9: Outrigger Balls May Connect to Power Balls on CLP

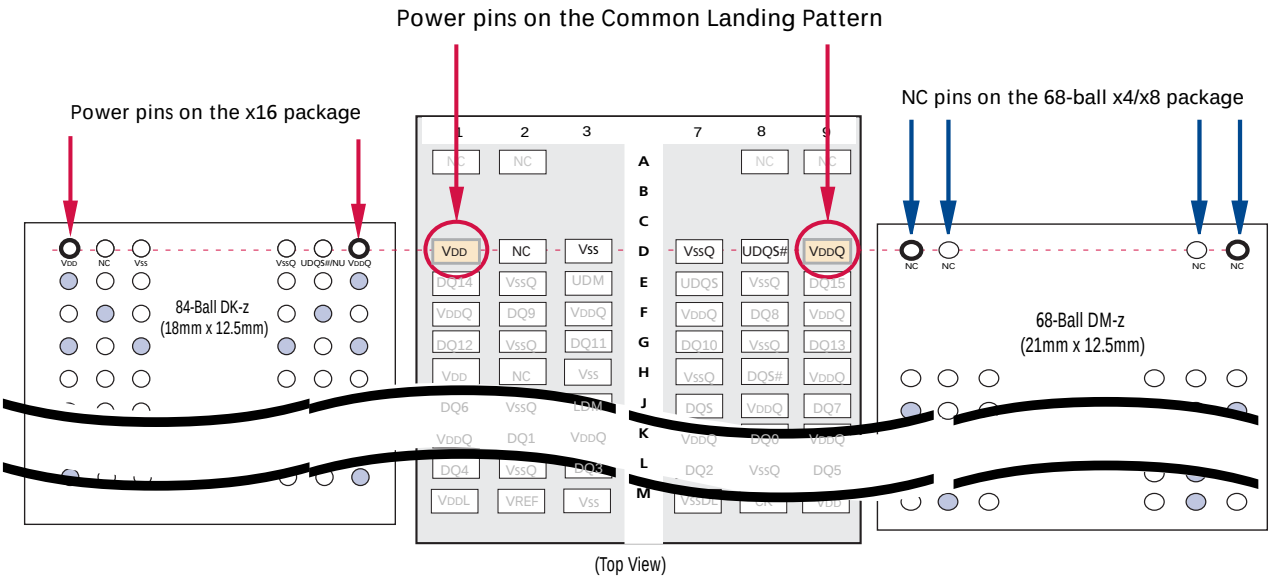

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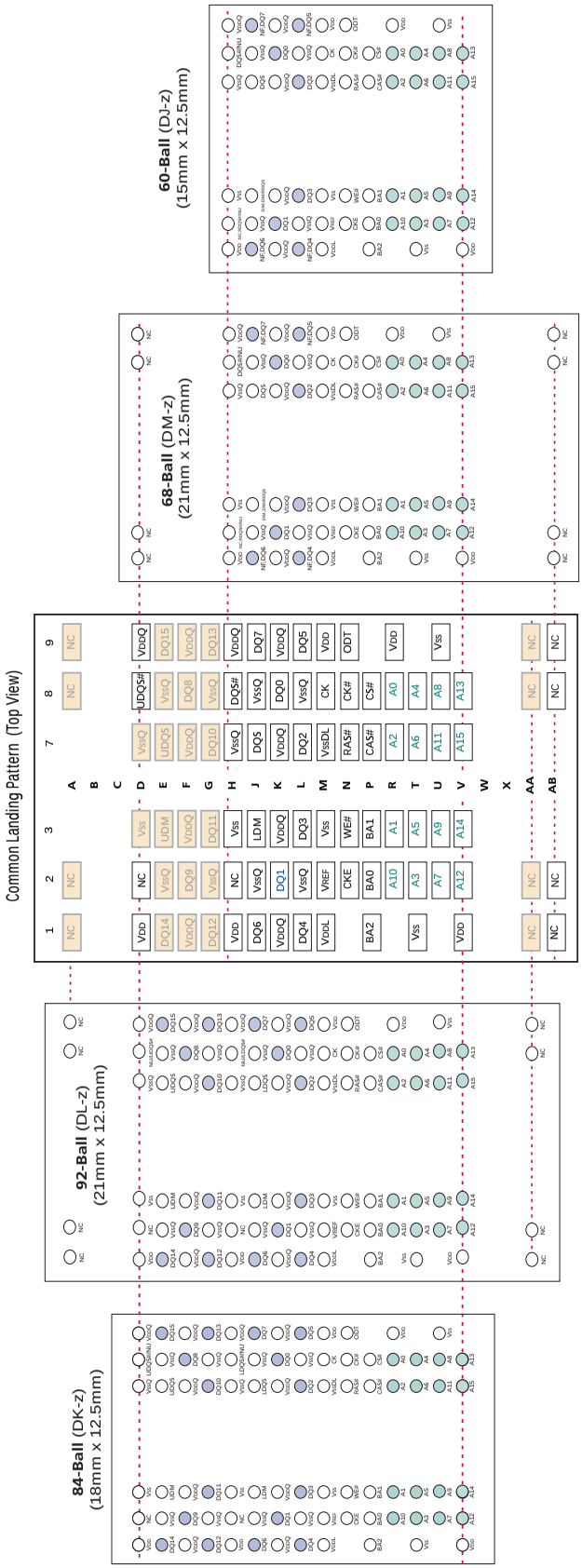
Figure 10: CLP Showing Placement of All Package Options



Note: Refer to individual data sheet for specific pin out.

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Table 4: Cross-Reference of CLP Signal Name/Location to Package Ball Location

CLP Signal Name	CLP Pad Location	Individual Package Locations			
		92-Ball DL-z	84-Ball DK-z	68-Ball DM-z	60-Ball DJ-z
A0	R8	R8	M8	M8	H8
A1	R3	R3	M3	M3	H3
A2	R7	R7	M7	M7	H7
A3	T2	T2	N2	N2	J2
A4	T8	T8	N8	N8	J8
A5	T3	T3	N3	N3	J3
A6	T7	T7	N7	N7	J7
A7	U2	U2	P2	P2	K2
A8	U8	U8	P8	P8	K8
A9	U3	U3	P3	P3	K3
A10	R2	R2	M2	M2	H2
A11	U7	U7	P7	P7	K7
A12	V2	V2	R2	R2	L2
A13	V8	V8	R8	R8	L8
A14	V3	V3	R3	R3	L3
A15	V7	V7	R7	R7	L7
BA0	P2	P2	L2	L2	G2
BA1	P3	P3	L3	L3	G3
BA2	P1	P1	L1	L1	G1
CAS#	P7	P7	L7	L7	G7
CK	M8	M8	J8	J8	E8
CK#	N8	N8	K8	K8	F8
CKE	N2	N2	K2	K2	F2
CS#	P8	P8	L8	L8	G8
LDM	J3	J3	F3	F3 (DM/RDQS)	B3 (DM/RDQS)
DQ0	K8	K8	G8	G8	C8
DQ1	K2	K2	G2	G2	C2
DQ2	L7	L7	H7	H7	D7
DQ3	L3	L3	H3	H3	D3
DQ4	L1	L1	H1	H1 (DQ4/NF)	D1 (DQ4/NF)
DQ5	L9	L9	H9	H9 (DQ5/NF)	D9 (DQ5/NF)
DQ6	J1	J1	F1	F1 (DQ6/NF)	B1 (DQ6/NF)
DQ7	J9	J9	F9	F9 (DQ7/NF)	B9 (DQ7/NF)
DQ8	F8	F8	C8	–	–
DQ9	F2	F2	C2	–	–
DQ10	G7	G7	D7	–	–
DQ11	G3	G3	D3	–	–
DQ12	G1	G1	D1	–	–
DQ13	G9	G9	D9	–	–
DQ14	E1	E1	B1	–	–
DQ15	E9	E9	B9	–	–
DQS	J7	J7 (LDQS)	F7(LDQS)	F7	B7
DQS#	H8	H8 (NU/LDQS#)	E8 (NU/LDQS#)	E8 (DQS#/NU)	A8 (DQS#/NU)

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Table 4: Cross-Reference of CLP Signal Name/Location to Package Ball Location (Continued)

CLP Signal Name	CLP Pad Location	Individual Package Locations			
		92-Ball DL-z	84-Ball DK-z	68-Ball DM-z	60-Ball DJ-z
NC	A1	A1	–	–	–
NC	A2	A2	–	–	–
NC	A8	A8	–	–	–
NC	A9	A9	–	–	–
NC	D2	D2	A2	A2	–
NC	H2	H2	E2	E2 (NU/RDQS)	A2 (NU/RDQS)
NC	AA1	AA1	–	–	–
NC	AA2	AA2	–	–	–
NC	AA8	AA8	–	–	–
NC	AA9	AA9	–	–	–
NC	AB1	–	–	W1	–
NC	AB2	–	–	W2	–
NC	AB8	–	–	W8	–
NC	AB9	–	–	W9	–
ODT	N9	N9	K9	K9	F9
RAS#	N7	N7	K7	K7	F7
UDM	E3	E3	B3	–	–
UDQS	E7	E7	B7	–	–
UDQS#	D8	D8 (NU/URDQS#)	A8 (NU/URDQS#)	A8 (NC)	–
V_{DD}	D1	D1	A1	A1 (NC)	–
V_{DD}	H1	H1	E1	E1	A1
V_{DD}	M9	M9	J9	J9	E9
V_{DD}	R9	R9	M9	M9	H9
V_{DD}	V1	V1	R1	R1	L1
V_{DDQ}	D9	D9	A9	–	–
V_{DDQ}	H9	H9	E9	E9	A9
V_{DDQ}	K1	K1	G1	G1	C1
V_{DDQ}	K3	K3	G3	G3	C3
V_{DDQ}	K7	K7	G7	G7	C7
V_{DDQ}	K9	K9	G9	G9	C9
V_{DDQ} (NC)	F1	F1	C1	–	–
V_{DDQ} (NC)	F3	F3	C3	–	–
V_{DDQ} (NC)	F7	F7	C7	–	–
V_{DDQ} (NC)	F9	F9	C9	–	–
V_{SSQ} (NC)	E2	E2	B2	–	–
V_{SSQ} (NC)	E8	E8	B8	–	–
V_{SSQ} (NC)	G2	G2	D2	–	–
V_{SSQ} (NC)	G8	G8	D8	–	–
V_{REF}	M2	M2	J2	J2	E2
V_{SS}	D3	D3	A3	–	–
V_{SS}	H3	H3	E3	E3	A3
V_{SS}	M3	M3	J3	J3	E3
V_{SS}	T1	T1	N1	N1	J1

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Table 4: Cross-Reference of CLP Signal Name/Location to Package Ball Location (Continued)

CLP Signal Name	CLP Pad Location	Individual Package Locations			
		92-Ball DL-z	84-Ball DK-z	68-Ball DM-z	60-Ball DJ-z
VSS	U9	U9	P9	P9	K9
VDDL	M1	M1	J1	J1	E1
VSSDL	M7	M7	J7	J7	E7
VSSQ	J2	J2	F2	F2	B2
VSSQ	J8	J8	F8	F8	B8
VSSQ	H7	H7	E7	E7	A7
VSSQ	L2	L2	H2	H2	D2
VSSQ	L8	L8	H8	H8	D8
VSSQ	D7	D7	A7	–	–
WE#	N3	N3	K3	K3	F3

Conclusion

Layout for DDR2 designs is easily managed once the DDR2 package options are understood. (Options include package-size variation, uniquely-defined ballout/electrical arrays, and required multiple-use pads for supporting configurations.)

Because of the diverse options available with DDR2, a defined common landing pattern provides the designer with maximum layout flexibility. By using the CLP, a printed circuit board can accommodate all DDR2 device configurations and will be compatible with most package options, regardless of vendor or future die revisions.

For additional information or the latest DDR2 data sheets, please refer to Micron's Web site at www.micron.com/products.

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