Technical Note

Power Solutions for DDR2 Notebook PCs

In cooperation with TEXAS INSTRUMENTS

Overview

This technical note provides general guidelines for designing power circuitry for DDR2 memory. It includes the DDR2 voltage requirements and encompasses a sample reference design focused on the Texas Instruments Incorporated (TI) TPS51116, a complete DDR2 memory power solution that includes a synchronous buck controller, 3A linear dropout regulator (LDO), and buffered references.

DDR2 Advantages for Notebooks

DDR2 memory is an excellent solution for notebook computers. Aside from faster speeds, its greatest advantage over older memory technologies is its reduced power consumption, which results in cooler operating temperatures and extended battery life (see Figure 1 on page 2).

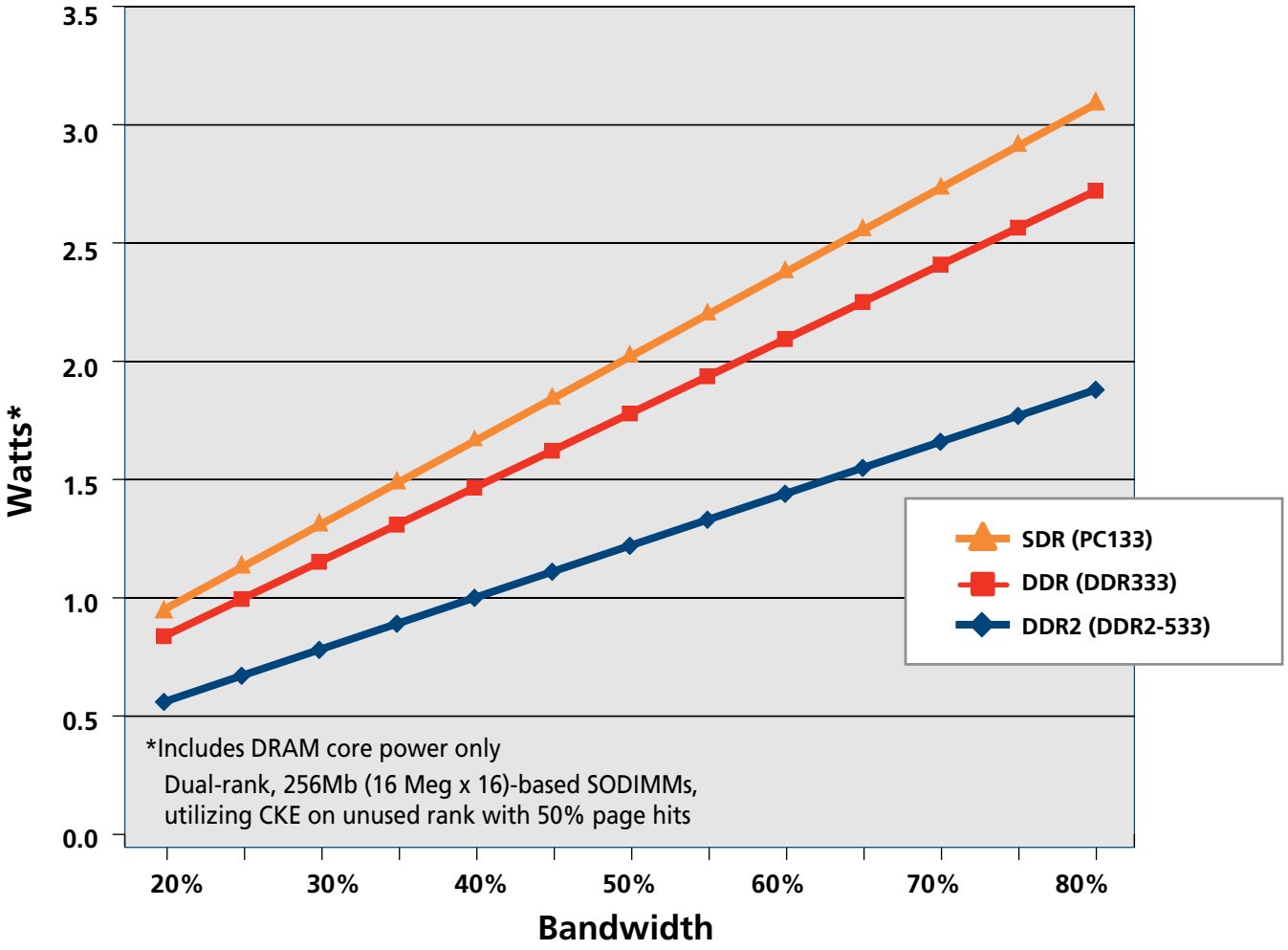
The reduced power consumption is realized through a number of design features, including lower operating voltages, reduced page sizes, and 4*n*-prefetch support. DDR2 memory uses a low operating voltage of only $V_{DD} = V_{DDQ} = 1.8V$ and supports an SSTL_18 I/O interface. The reduced page sizes minimize the activation current, and the 4*n*-prefetch architecture allows the device core to run at a slower frequency while driving an ultra-fast data rate (currently up to 1066 MT/s/b).

Another advantage of DDR2 memory in notebooks is higher density in the same space; aside from the voltage-key placement and pinout change, the DDR2 SODIMM uses the same 200-pin socket as DDR.

At the device level, DDR2 components are manufactured at individual memory densities up to 2Gb (at the component level, this reflects a 128Mb x 16 or 256Mb x 8 device), which means DDR2 supports a 4GB channel with just 2 slots.

Also new with DDR2 memory is on-die termination (ODT), which has a significant impact on signal quality and power dissipation. ODT gives the controller more effective management of termination to the high-speed signals where and when it is needed.

Figure 1: Power Performance Curves on SDR, DDR, and DDR2



DDR2 Notebook Assumptions

JEDEC has defined 4 standardized small outline, dual in-line memory modules (SODIMMs) that include single- and dual-rank DIMMs utilizing either x16 or x8 devices. All 4 configurations are 64-bit-wide unbuffered SODIMMs with predefined electrical and mechanical specifications.

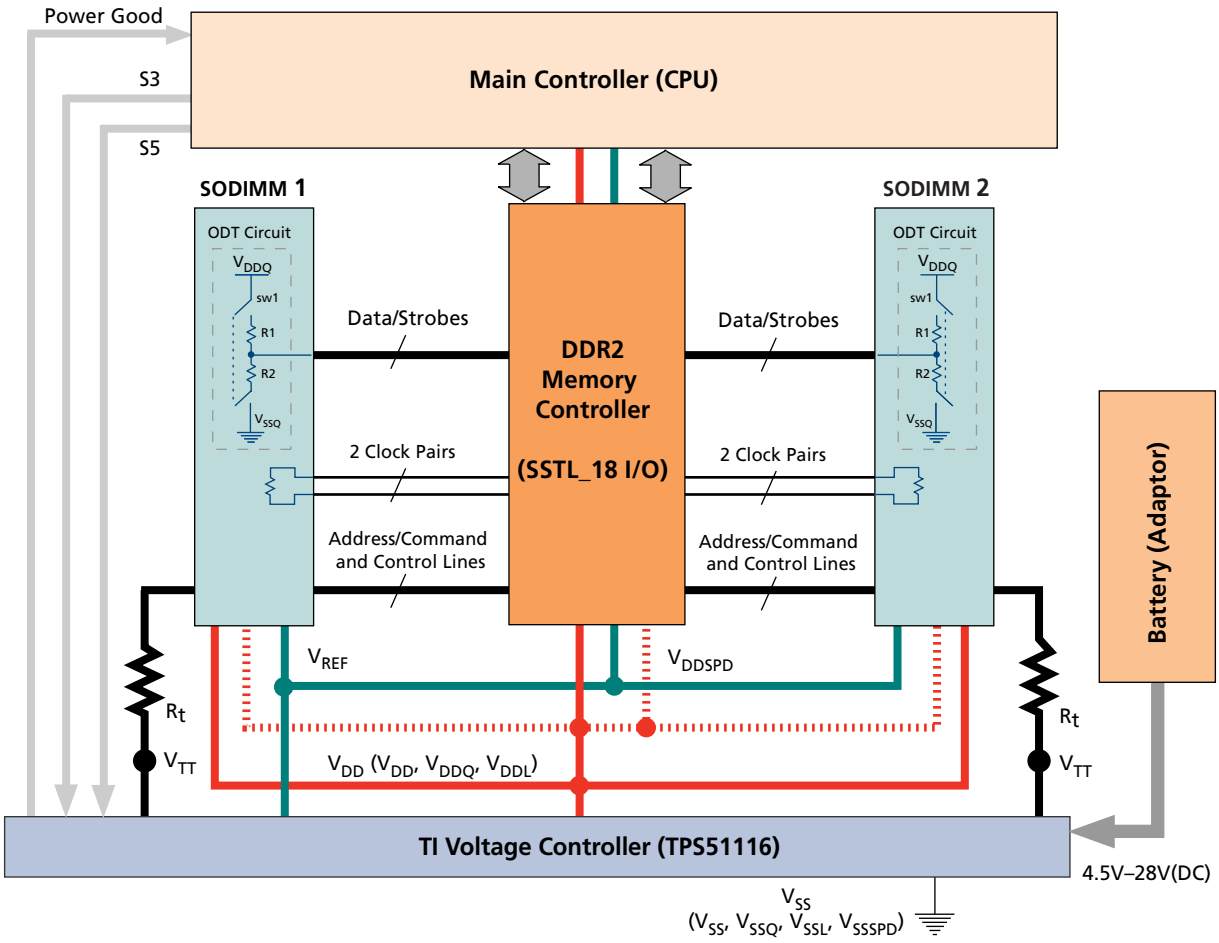
This technical note assumes that the notebook system designer will utilize a dual memory channel with 2 slots, 1 per channel (see Figure 2 on page 3). For a dual-channel, 2-slot system, both the address and command lines terminate at V_{TT} through a resistor. All the high-speed data strobes and data signals utilize localized ODT. On the module, the differential clock pairs (CK/CK#) are differentially terminated.

This combination makes for a low-cost, low-power application that maximizes battery life while maintaining a small size and high performance.

DDR2 Voltage Requirements

One challenge in designing a DDR2 system is meeting the strict power requirements and predefined power-up and initialization sequences as defined by JEDEC (JESD79-2 DDR2 SDRAM Specification). Therefore, it is critical that the initial power ramps be controlled to meet specifications. In addition, both the termination voltage (V_{TT}) and reference voltage (V_{REF}) must maintain their respected relationships to V_{DD} at all times. The following sections provide detailed voltage requirements for DDR2 notebook systems.

Figure 2: Functional Block Diagram of a Dual-Channel, 2-Slot DDR2 Notebook



Supply

V_{DD} (V_{DD}, V_{DDL}, V_{DDQ})

The DDR2 device requires a single power source for primary supply voltages in order to ensure that all voltage levels track each other, especially during the power ramp. At the module level, V_{DD} (device core), V_{DDL} (device DLL), and V_{DDQ} (device I/O) share a single power plane with the interconnecting pins labeled as V_{DD}. Likewise, V_{SS}, V_{SSL}, and V_{SSQ} share a common ground plane labeled as V_{SS}.

The memory supply voltage is specified as $V_{DD} = V_{DDQ} = 1.8V$ with a DC tolerance of ±100mV. DC is defined as any signal ≤20 MHz. At the initial power-up, all supply power should be stable and meet specification within ≤10ms.

The amount of current each module consumes depends on the density and speed of the module, number of ranks, and, most importantly, the usage conditions. For example, to build a high-density, dual-rank module using (x8) DRAMs, 16 individual devices are required. A system utilizing 2 of these modules and running a heavy-use condition may consume up to 7W–8W. However, the same system, using 1 lower-density, dual-rank module using (x16) DRAMs, will have only 8 discrete components each, and, under moderate use conditions, might consume a total of only 1.5W–2W.

Micron's Web site has a dedicated technical note, "TN-47-04: Calculating Memory System Power for DDR2," and a custom DDR2 power calculator that provide additional information about how to estimate actual module power usage at www.micron.com/systemcalc.

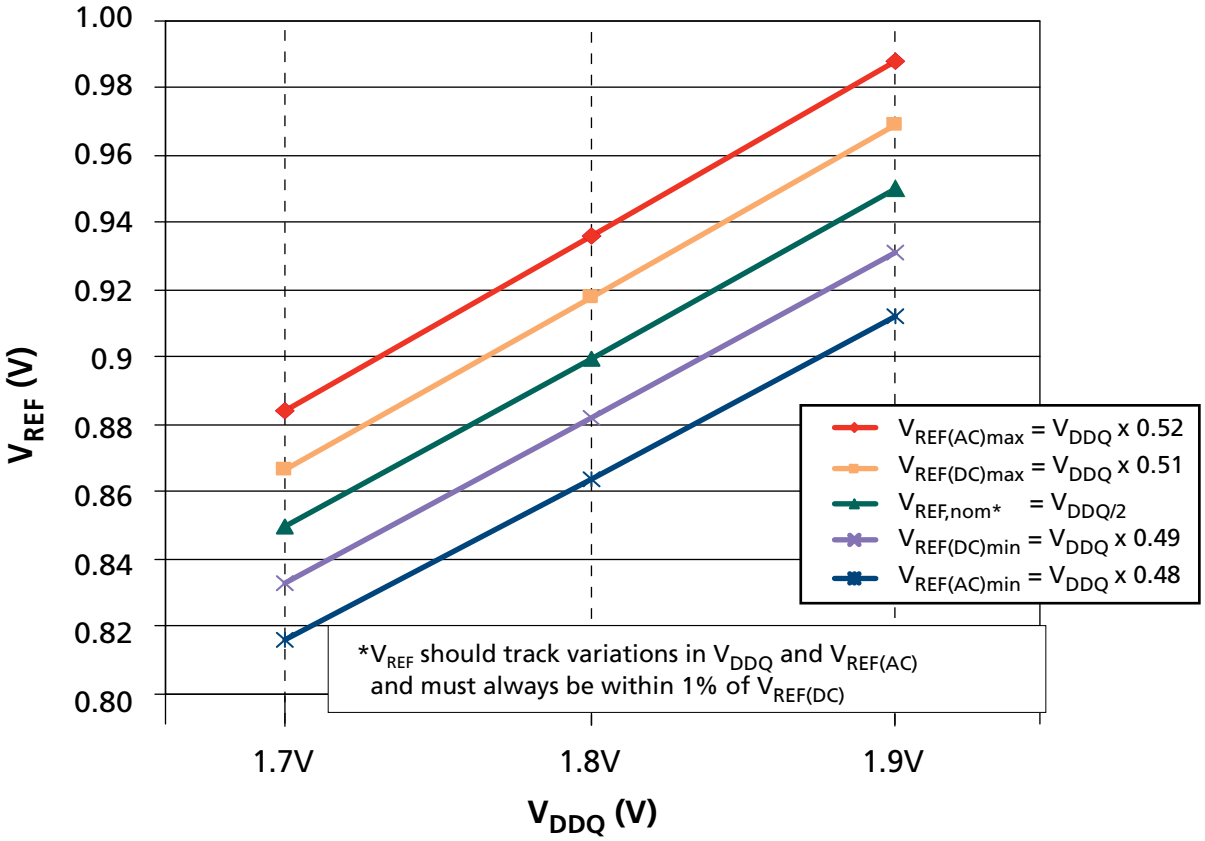
V_{REF}

Another key supply voltage is the input reference voltage (V_{REF}). All DDR2 input receivers are calibrated to operate within the specified V_{REF} input levels. For proper device operation, it is critical that the V_{REF} input is free from excess noise or voltage variations. Any degrading of the V_{REF} input voltage directly affects the setup and hold times of the DDR2 device.

V_{REF} is expected to equal $V_{DDQ/2}$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±1% of the DC value. Peak-to-peak AC noise on V_{REF} must not exceed ±2% of $V_{REF(DC)}$. AC noise is defined as any noise over 20 MHz in frequency. There is virtually no current draw on the DDR2 V_{REF} pin; only leakage current is present (less than 5µA per DRAM component).

Figure 3 on page 5 shows the industry-standard voltage specifications and tracking requirements for V_{REF}.

Figure 3: Required V_{REF} Voltage Relationships



V_{TT}

DDR2 memory is optimized for stub-series terminated logic at 1.8V (SSTL_18) operation. The address, command, and control lines require system-level termination to a midpoint voltage. This midpoint voltage is called V_{TT} (or the I/O termination voltage). Having the termination sit at midpoint ensures symmetry for switching times. It is important that V_{TT} tracks any variation in the DC levels of V_{REF}. By specification, at all times V_{TT} must equal V_{REF} ±40mV. The termination voltage (V_{TT}) is supplied directly to the motherboard but not to the module. See Figure 4 on page 6 for logic levels of a properly terminated SSTL_18 signal.

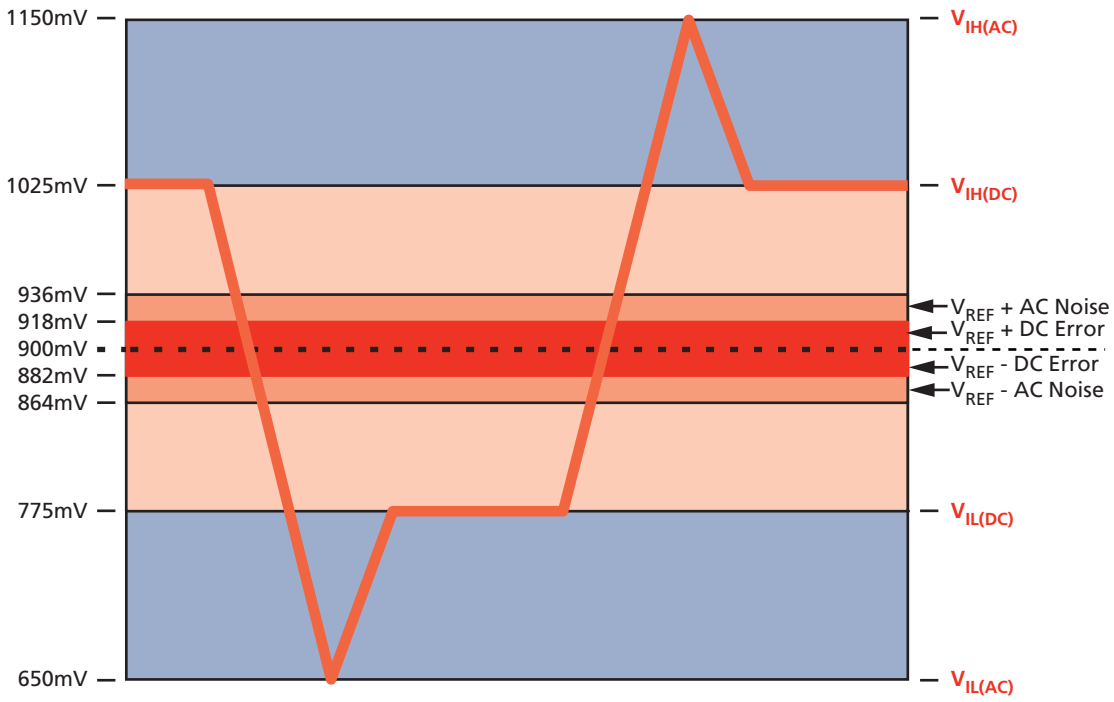
ODT (On-Die Termination)

As previously mentioned, DDR2's high-speed, bidirectional signals (data and strobes) are uniquely terminated with on-die termination (ODT). This new feature allows for optimal signal quality (see Figure 5 on page 6) by dynamically controlling the exact termination value where and when it is needed. For example, the ideal placement for termination is at the end of the active signal trace. So, when WRITING to SODIMM1, the memory controller dynamically disables the ODT function on SODIMM2 and the memory controller (both buses) and activates the ODT circuitry on SODIMM1 (at the end of the active transmission line). Likewise, during a READ from either SODIMM, the

memory controller dynamically disables the ODT circuitry at both SODIMM locations and enables ODT circuitry on the active bus at the memory controller. ODT facilitates a much-simpler board design that uses fewer components and thereby costs less.

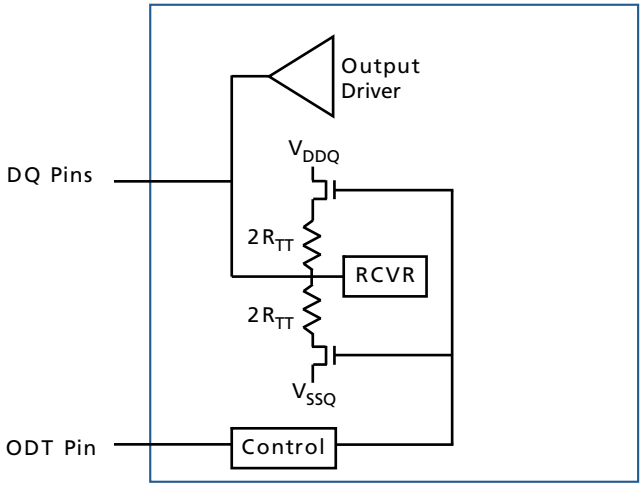
ODT also allows better thermal and power-management control. For example, during DRAM inactive times, most memory controllers completely disable the termination in order to conserve power. ODT can accomplish this dynamically.

Figure 4: SSTL_18 Single-Ended Input-Logic Levels



Note: Numbers in diagram reflect nominal values (V_{DD} = V_{DDQ} = 1.8V)

Figure 5: Functional Block Diagram of ODT



V_{DDSPD}

Although not utilized for the DRAM, there is one additional power requirement for the SODIMM—the power for the serial present detect (SPD) EEPROM, which holds the module operating parameters. This voltage (V_{DDSPD}) has a wide range tolerance, from +1.7V to +3.6V. In its worst case, the current draw of this pin should be no more than 3mA–4mA.

Power Management for Notebooks with Micron DDR2 and TI TPS51116

Designers who use Micron's DDR2 memory modules can now incorporate TI's TPS51116, an integrated power-management solution that combines a DC/DC current-mode switching controller with a 3A sink/source linear dropout regulator (LDO). This highly integrated device significantly reduces the number of external components typically required to support all the power management for DDR2 memory systems, making the TPS51116 easy to use while offering a smaller total-solution size and lower total-solution cost, without sacrificing performance.

TPS51116: A Solution for Complete DDR2 Power Management

Figure 6 on page 8 shows a typical application schematic for the TPS51116 and how it integrates into the complete DDR2 power-management solution with:

- Synchronous current mode DC/DC controller to power V_{DD}
- Buffered reference to provide V_{REF} (V_{REF} tracks one-half V_{DD})
- 3A sink/source LDO to power V_{TT} (V_{TT} tracks V_{REF})
- S3/S5 sleep-state controls

This high-level integration simplifies the design of the power-management segment of DDR2 memory. This places the burden on the TPS51116 to meet the industry-standard specifications and the proper management of S3 and S5 states.

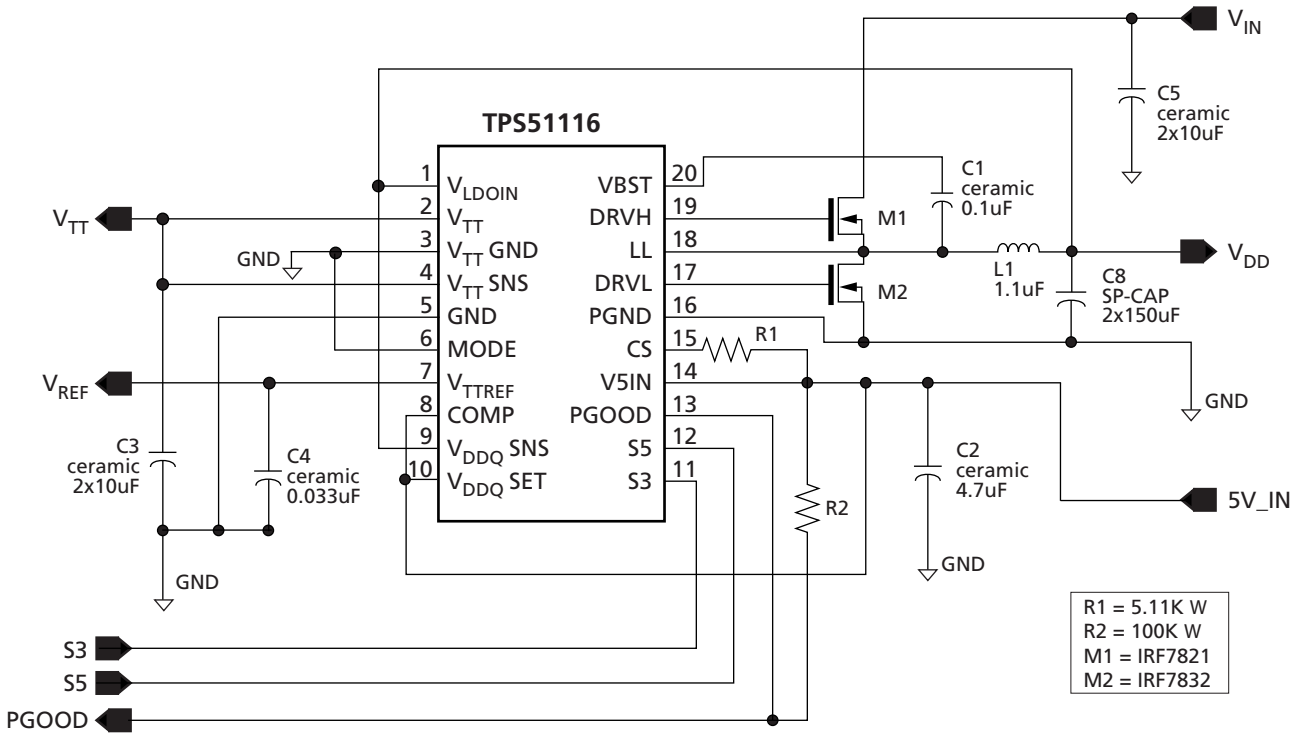
The synchronous current mode DC/DC controller is used to power V_{DD}/V_{DDQ}. Implementing the power supply requires 2 external NFETs, in addition to an inductor and input/output capacitors. This output is used to power DDR2 memory's V_{DD}/V_{DDQ} and is able to achieve high efficiency during wide load variation—expected to range from 10mA to 10A.

The output of TPS51116's switcher is internally divided down by one half and is used to generate V_{REF}. The V_{REF} output tracks changes in V_{DD}/V_{DDQ} with a high level of accuracy, achieved by the precisely matched internal-resistor divider. V_{REF} is buffered, helping increase its immunity to noise and changes in load. This is critical in maintaining the stringent V_{REF} to V_{DDQ} tracking requirements of the DDR2 device.

The final-output-voltage rails required for DDR2 is for V_{TT}. The power for this rail comes from the LDO segment of the TPS51116. The LDO supports 3A peak current and has 1.5A continuous current capabilities.

This LDO can sink/source current and meet the industry-standard specifications with only 2x10uF ceramic output capacitors. DDR2 allows the use of an LDO to power termination (V_{TT}) because of the reduction in required current, resulting from the implementation of ODT.

Figure 6: Typical Application Circuit for TPS51116



Line Regulation, Load Regulation, and Transient Response

DDR2 memory requires industry-standard power specifications. The voltage tolerances that need to be supported throughout the changes in input voltage (line regulation), output current (load regulation), and transient response are defined as:

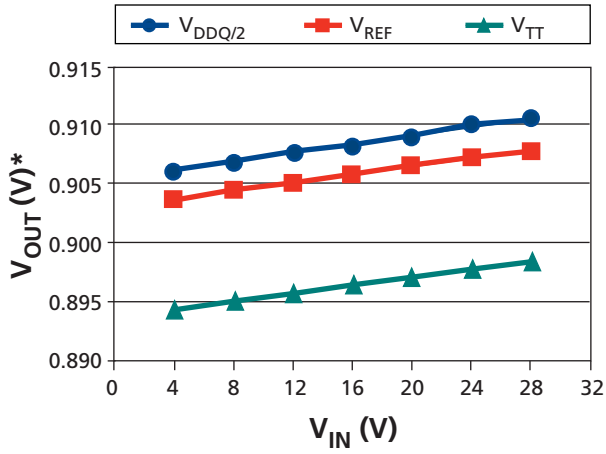
- V_{DDQ} = 1.8V ±100mV
- V_{REF} = 0.49 V_{DDQ}/0.51 V_{DDQ}
- V_{TT} = V_{REF} ±40mV

Line regulation ensures that the tolerances are maintained when the input voltage changes. Figure 7 on page 9 shows as the input voltage changes from 4V to 28V, V_{DDQ} changes by only a few millivolts (spec is ±100mV). V_{REF} tracks $V_{DDQ/2}$, and there is a difference of only about 10mV between V_{TT} and V_{REF} (spec is ±40mV).

Load regulation and transient response ensures the tolerances are maintained when the output current changes. Load regulation is a static test condition, while transient response is a dynamic test condition.

Figure 8 on page 9 shows V_{DDQ} with a static load change from 0A to 10A on V_{DDQ}, with its output voltage <35mV from 1.8V (specification is ±100mV). In Figure 9 on page 10, the load changes from -1.5A to 1.5A on V_{TT}, and V_{DDQ} is about 25mV from 1.8V (specification is ±100mV), with V_{TT}–V_{REF} near ±20mV (specification is V_{REF} ±40mV).

Figure 7: Line Regulation for All 3 Outputs



* Test was performed with a 7A load on $V_{DDQ/2}$ and a 0.3A load V_{TT}

Figure 8: Load Regulation V_{DDQ} Only (V_{IN} = 12V)

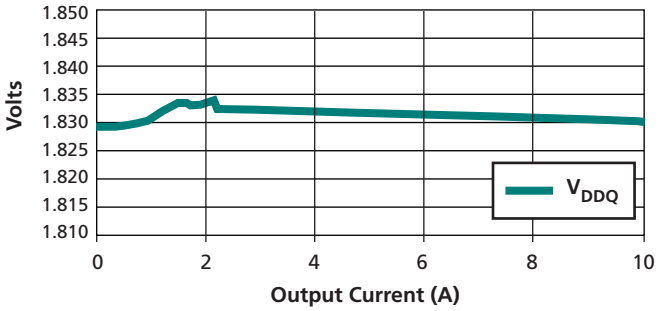
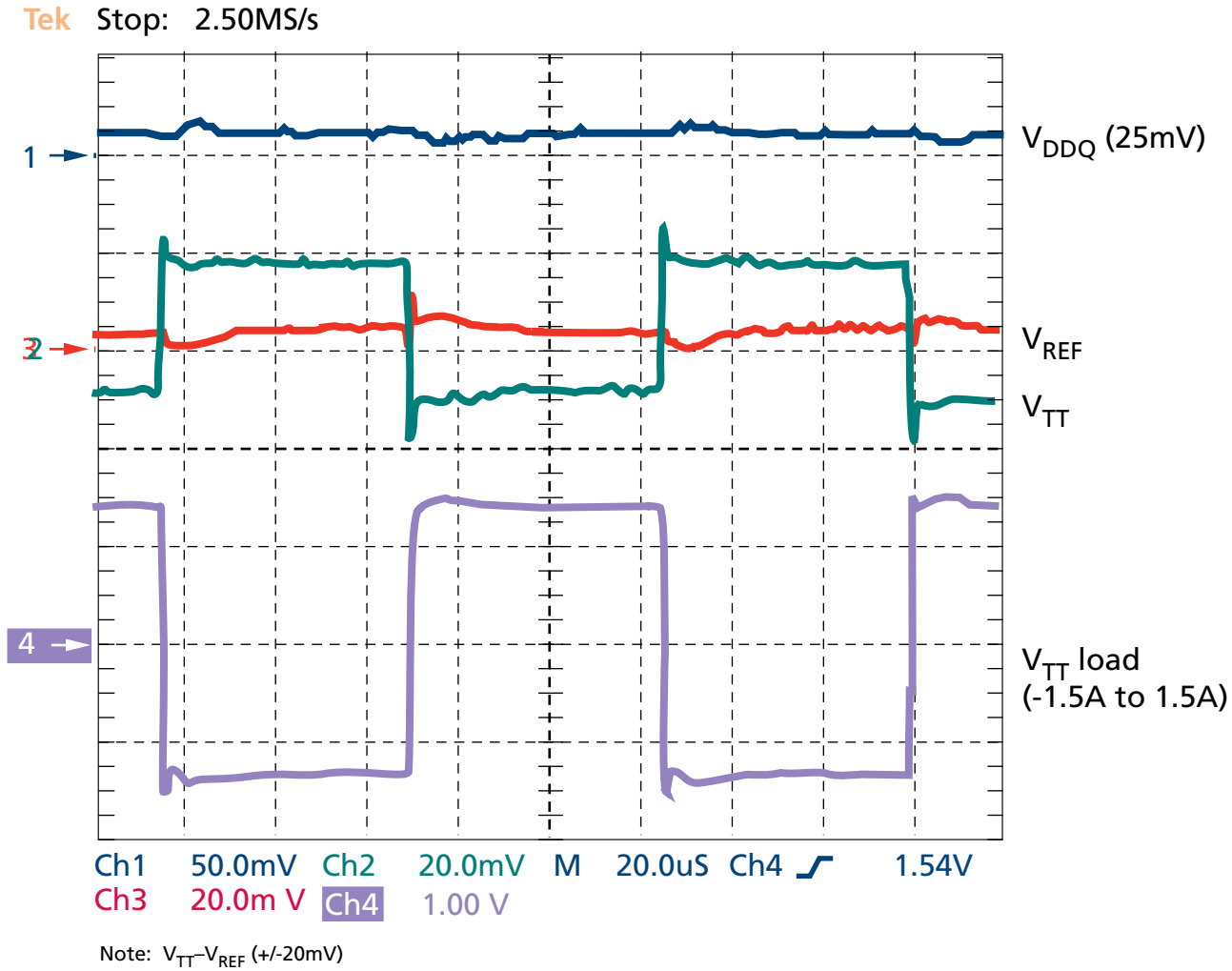


Figure 9: Transient Response (V_{IN} = 12V)



Note: V_{TT}–V_{REF} (+/-20mV)

TPS51116 Manages the Critical Relationship Between V_{TT}/V_{REF} and V_{DDQ}

TI's TPS51116 has a very important role in managing notebook sleep-state functions. For DDR2 memory, it is critical during both start-up and shutdown that V_{DDQ} is always higher than V_{TT}/V_{REF}. If V_{TT}/V_{REF} is greater than V_{DDQ} + 0.3V, the DDR2 memory could latch up.

TPS51116's integrated sleep-state functions help prevent this condition—the S3 and S5 pins on the TPS51116 are connected to the S3 and S4/S5 control signals in the notebook computer (Figure 2 on page 3), enabling the S3 and S5 pins to be used to manage all sleep-state functions:

- S0 = Full On
- S3 = Suspend-to-RAM (STR)
- S4/S5 = Suspend-to-Disk (STD)/Soft Off

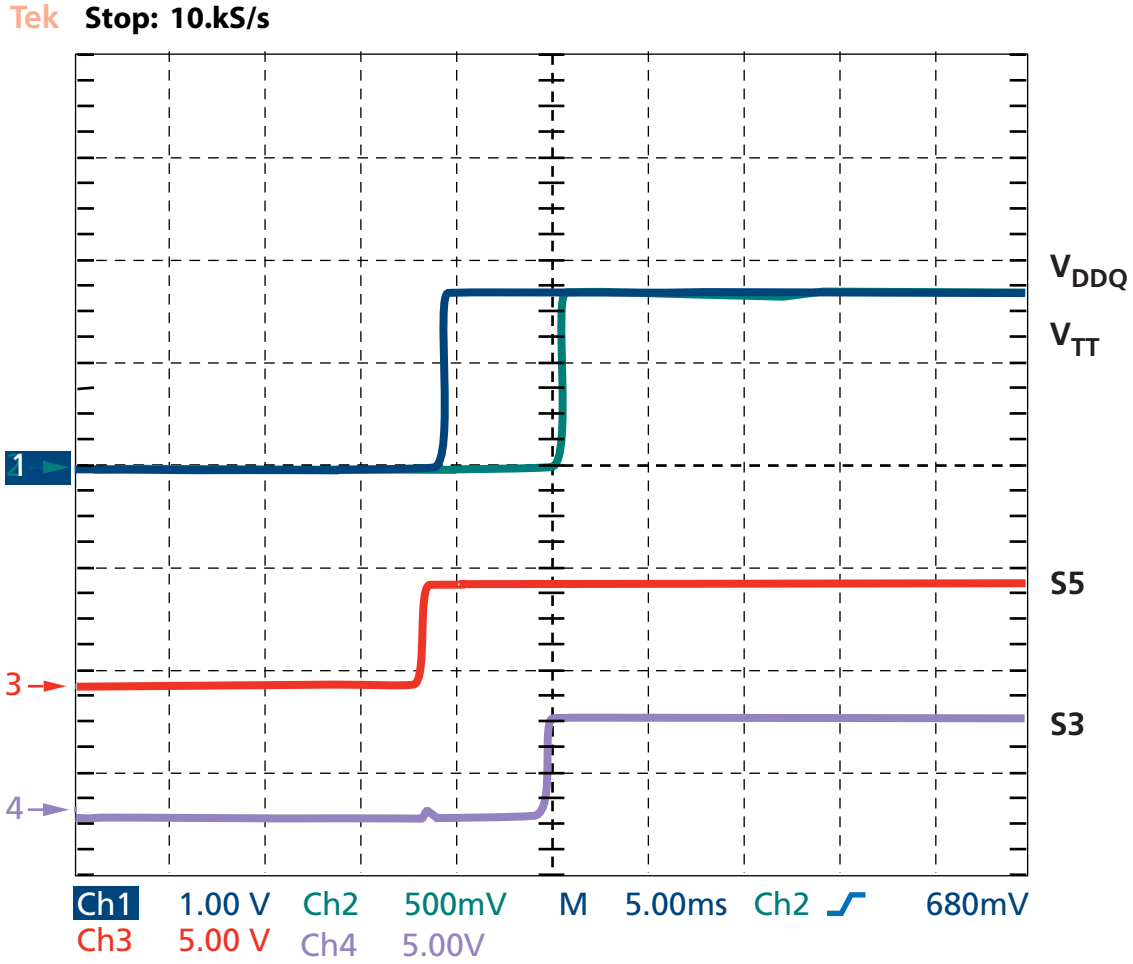
Table 1 summarizes how the TPS51116 handles the sleep-state modes.

When transitioning from an S4/S5 state (STD) to S0 (Full On), S5 will go HIGH first, and then S3 will go HIGH. Figure 10 on page 12 shows that when S5 goes HIGH, V_{DDQ} turns on, and when S3 goes HIGH, V_{TT} will turn on. During start-up, V_{TT} cannot turn on until a V_{DDQ} voltage exists; as soon as V_{DDQ} voltage turns on, the V_{TT} voltage will track V_{DDQ}. Therefore, during start-up, V_{DDQ} will always be greater than V_{TT}.

Table 1: S3 and S5 TPS51116 Input and Output Parameters

State	Status	Inputs		Outputs		
		S3	S5	V_{DDQ}	V_{REF}	V_{TT}
S0	Full On	HIGH	HIGH	On	On	On
S3	Suspend-to-RAM (STR)	LOW	HIGH	On	On	Off (High-Z)
S4/S5	Suspend-to-Disk (STD)/Soft Off	LOW	LOW	Off (Discharge)	Off (Discharge)	Off (Discharge)

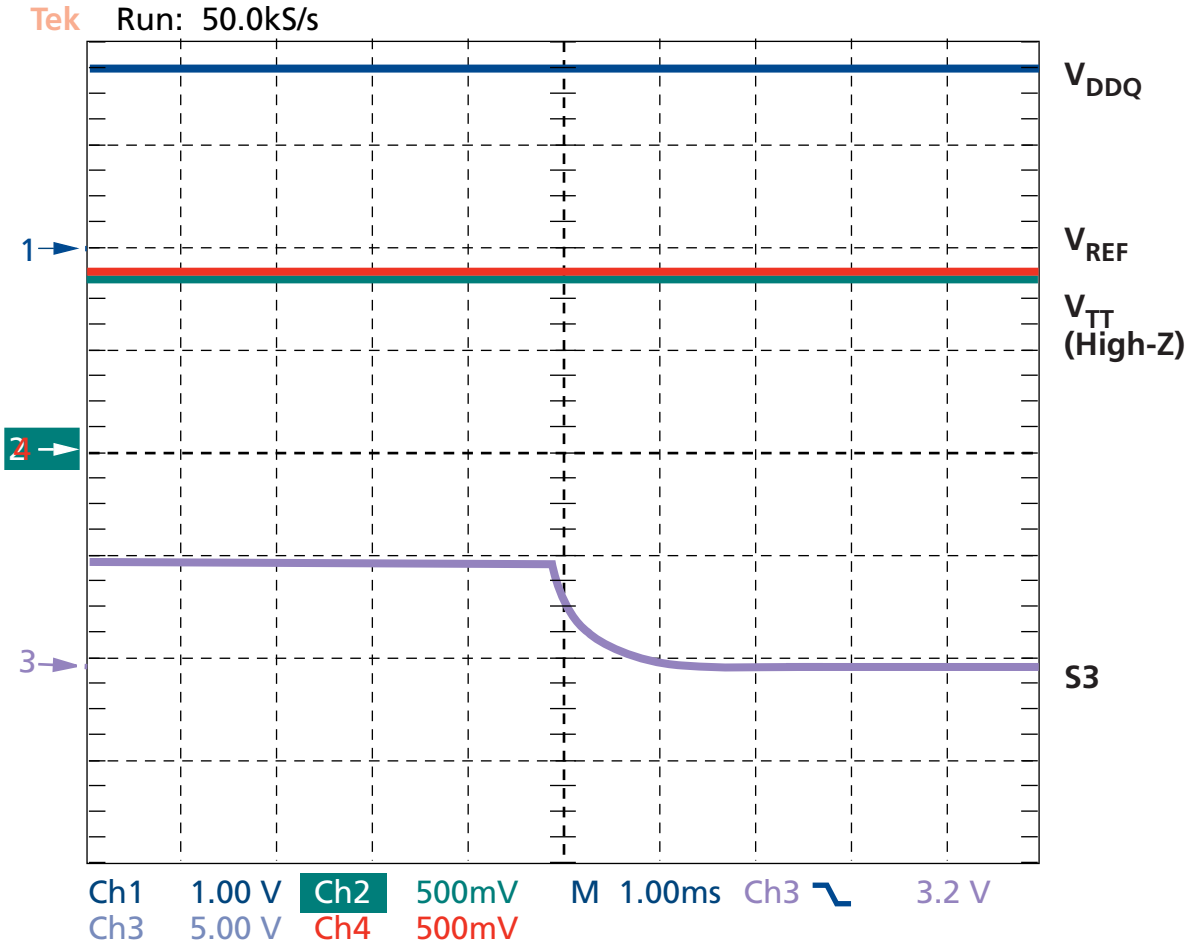
Figure 10: Full-On Power Ramp



During an S3 state, the S3 control signal goes LOW, and the system enters a Suspend-to-RAM state (STR). STR can occur only after the DRAM has been properly placed into self refresh mode. This requires a predefined series of command sequences (turn off ODT, precharge all banks, and then synchronously take CKE LOW with the AUTO REFRESH command). (See any Micron DDR2 data sheet for details on the required command sequence.)

The STR or self refresh mode is the lowest DRAM power state. If the proper command sequences are followed, and all supply voltages are kept within their specified limits, the DDR2 DRAM will preserve the data contents indefinitely. During this state, V_{DD}/V_{DDQ} and V_{REF} remain on, and V_{TT} enters a high-impedance state (High-Z). The V_{TT} output no longer sinks or sources current and is floating, as shown in Figure 11 on page 13.

Figure 11: Enter Suspend-to-RAM (STR)



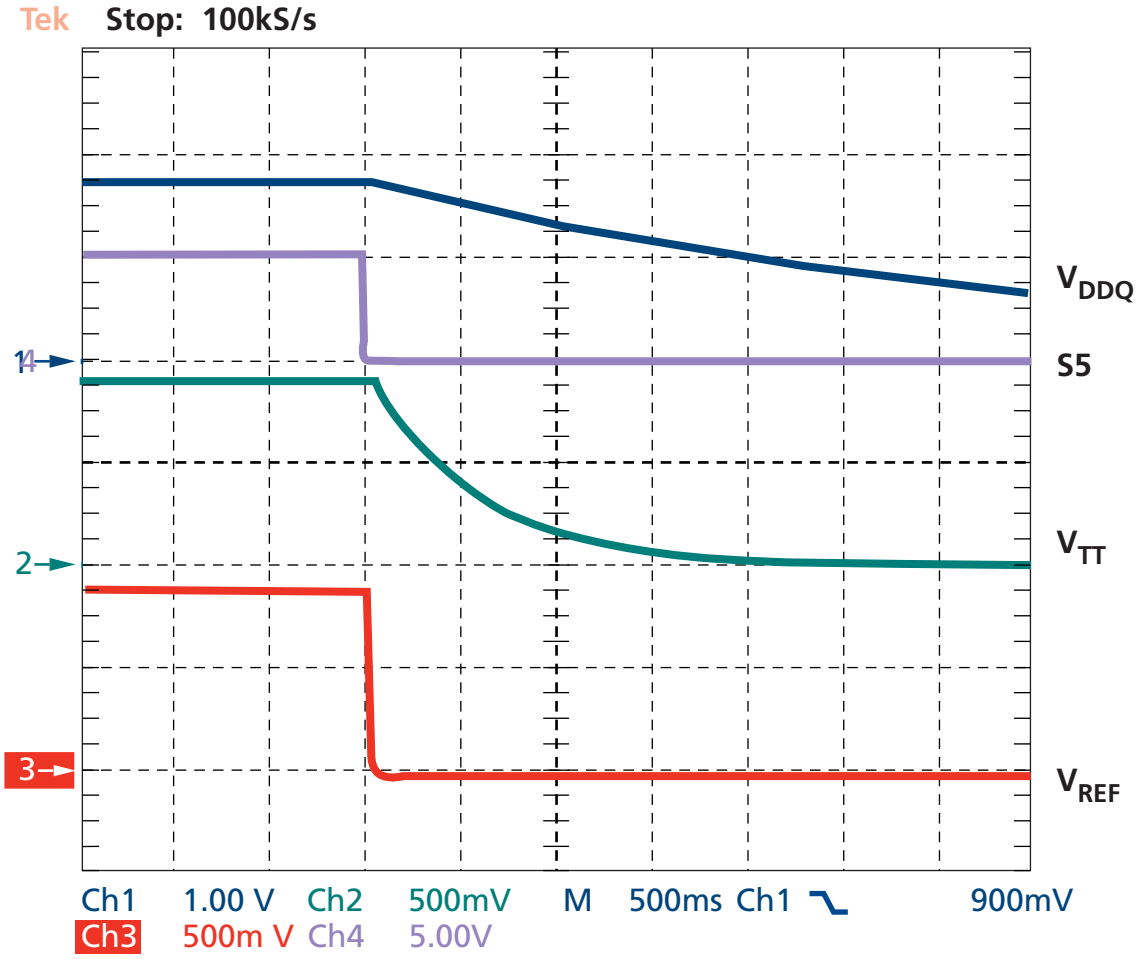
Note: During Suspend-to-RAM, all supply voltages must be maintained within specified data sheet values, including V_{REF}. V_{TT} is not required during STR.

For the TPS51116 to enter a Suspend-to-Disk (STD) state, the S5 signal must go LOW. During the STD (S4/S5 state), no power is supplied to the DRAM, and all DRAM data is lost. Upon exiting STD, it is critical that the DDR2 memory is powered up correctly, with a full initialization sequence. This includes the ramp-up of supply voltages and maintaining the required voltage relationships described previously.

After all supply voltages are steady, there must be 200µs of stable clocks before CKE goes HIGH, and the DRAM initialization sequence is started. (See any Micron DDR2 data sheet for expanded DRAM initialization requirements.)

During the STD, all TPS51116 outputs discharge to GND, including V_{DD}/V_{DDQ}, V_{TT}, and V_{REF}. The TPS51116 has been designed to ensure that V_{TT} and V_{REF} discharge more quickly than V_{DDQ} to guarantee that V_{DDQ} will always be greater than V_{TT}/V_{REF}, as shown in Figure 12 on page 14.

Figure 12: Suspend-to-DISK (STD)



Note: After the DRAM has been properly shut down, all supply voltages may be removed, and DRAM contents will be lost

Load Efficiency

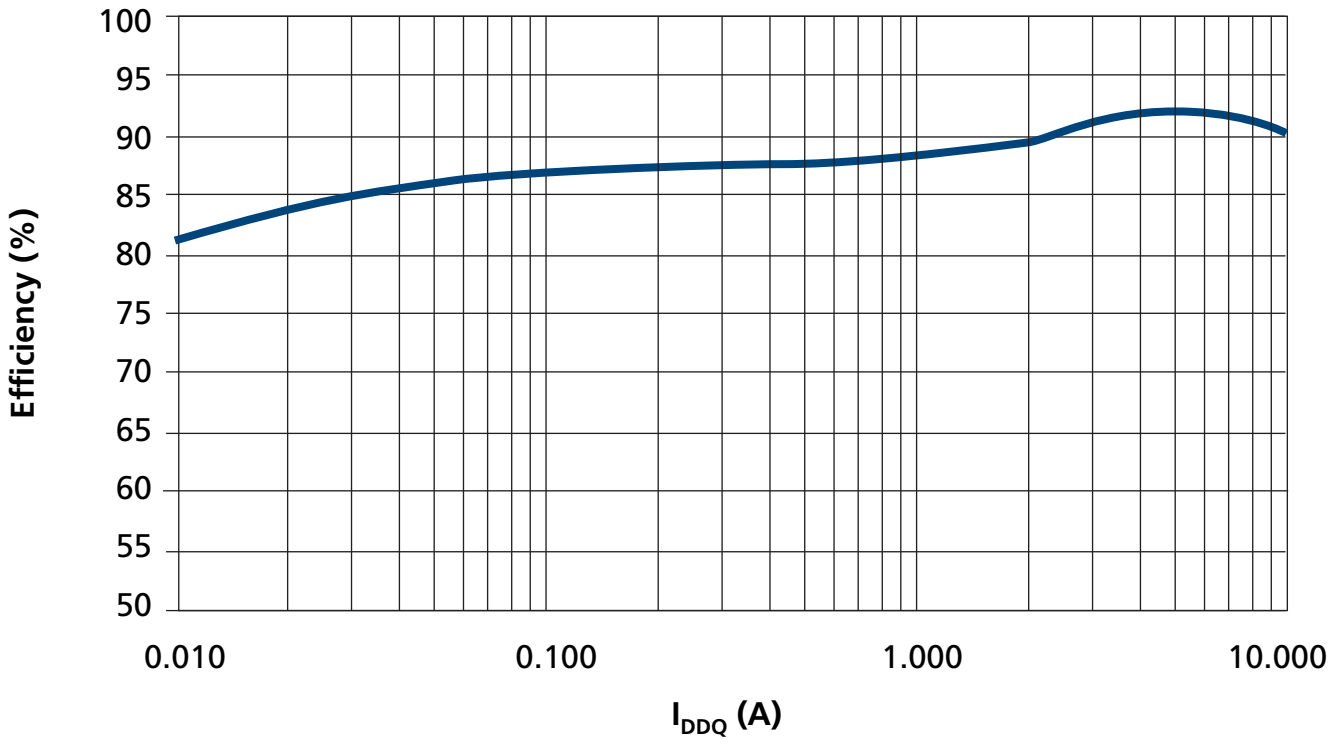
The TPS51116 has a high level of integration, making it easy to use and offering a smaller total solution size and lower total solution cost, without sacrificing performance. One of the most important performance features is the efficiency of the switcher, which is used to power V_{DD}. High efficiency at full loads—such as 10A—is important in reducing the total power dissipation and in extending battery life within the notebook computer.

A reduction in total power dissipation translates to a reduction in cost and size. The higher the efficiency, the longer the battery will last when the notebook is on or in an active state. The TPS51116 efficiency at 10A is 90% (input voltage at 12V), which is considered very high, as shown in Figure 13.

High efficiency at light loads—such as 10mA—is typically found during a standby condition and is critical in extending battery life when the notebook is in a standby mode. The higher the efficiency, the longer the battery will last while in standby. The TPS51116 has exceptional light-load efficiency that achieves greater than 80% (input voltage at 12V), as shown in Figure 13.

The TPS51116 can achieve this high level of efficiency at both 10A and 10mA because of its ability to adapt to the changes in load. At heavy loads—such as 10A—the high efficiency can be achieved because of the TPS51116's strong gate-drive capability and the gate drive's adaptive-dead-time control scheme. At light loads—such as 10mA—the TPS51116 enters skip mode, which significantly reduces the switching frequency.

Figure 13: Light-Load and Full-Load V_{DD}/V_{DDQ} Efficiency



Summary

DDR2 voltage requirements, solution, size, and efficiency are the most important considerations when designing power circuitry in a notebook computer. The TPS51116 is an ideal solution for powering Micron's DDR2 memory modules because it is optimized for low cost, is in a small total solution size, and provides high performance.

The TPS51116 high-level integration requires only 7 external resistors and capacitors, not including the power train for the switcher. Other solutions will use 18 or more external components, even if the switcher is integrated with the LDO. Typically, these notebooks require separate power-management ICs for V_{DDQ} and V_{TT}/V_{REF}.

Texas Instruments' power products can be found at www.ti.com.

For notebook applications, DDR2 is an excellent solution, providing ultra-fast data-transfer rates with extremely low operating-power requirements, dynamic ODT termination, and a small footprint.

With ODT, there is substantially less termination and signal routing on the motherboard. To ensure functionality, strict guidelines must be followed, making it a challenge to successfully integrate a power solution for a reliable DDR2 notebook design. This technical note identifies for the designer the critical DDR2 voltages and establishes a method to implement power to the DDR2 memory channel.

For the latest data sheets, please refer to Micron's Web site at www.micron.com/datasheets.