Technical Note

Mobile DRAM Power-Saving Features and Power Calculations

Introduction

It's important for today's mobile system designer to be aware of the power demands of the system DRAM. A key concern is the DRAM's average power consumption, which directly impacts overall battery life expectations for mobile systems.

This technical note addresses the power-saving features and power calculations of low-power Mobile DRAM memory. For in-depth power calculation information for standard DRAM products, refer to Micron's technical note TN-46-03, "Calculating Memory System Power for DDR," at www. micron.com/ddrsdram.

Mobile DRAM Power-Saving Features

Low-power Mobile DRAM products are designed to run at lower voltage supply levels to directly reduce power consumption. To provide even lower power consumption, three power management features have been added to reduce the voltage supply current (IDD) drawn from the system battery by the DRAM.

Micron and other JEDEC members have defined the following power-saving features:

Temperature Compensated Self Refresh (TCSR)

When the DRAM is in normal SELF REFRESH operation, power can be saved if the internal self refresh intervals can be adjusted for the ambient temperature of the DRAM component. This is accomplished using a temperature sensor. If the temperature sensor is on board the DRAM, the refresh intervals can be automatically adjusted for temperature at intervals specified in the product data sheet. If there is no on-board temperature sensor on a specific DRAM device, the memory controller can adjust the refresh intervals by utilizing its temperature sensor and programming the appropriate control bits specified in the product data sheet, based on the measured ambient temperature.

Partial Array Self Refresh (PASR)

When the DRAM is in SELF REFRESH operation, if all of the array is not needed to store data, the REFRESH operation can be limited to the portion of the memory's array where data will be stored. To take advantage of this power-saving mode, the data that needs to be preserved should be written to the portion of the array that will be refreshed. Specific details for this operation can be found in Micron's Mobile DRAM product data sheets.

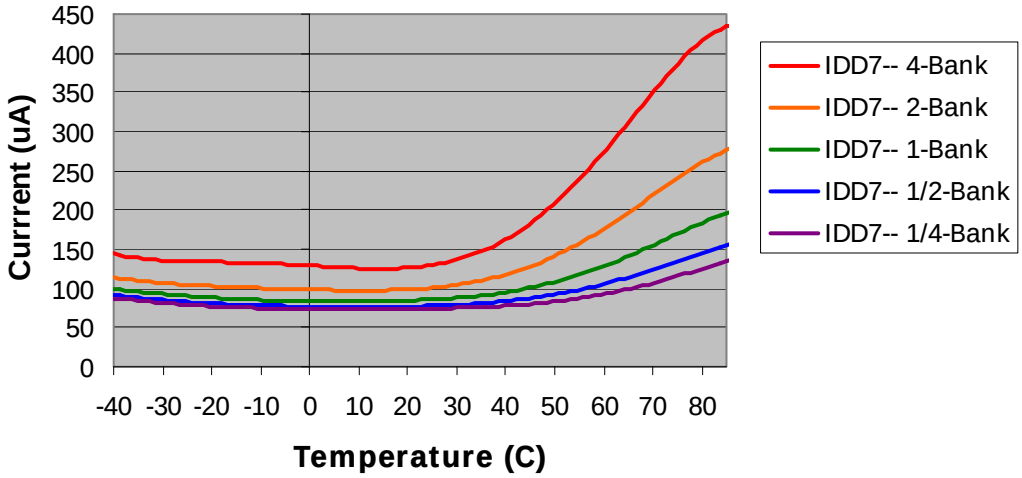
Deep Power-Down (DPD)

In some mobile applications, actual data retention in the DRAM is not required most of the time. However, power supply bias voltage cannot be removed when retention of its stored data is no longer needed. To maintain reduced DRAM power consumption during this time, the DRAM can incorporate DPD to turn off most or all of the on-board array

voltage generators. This feature is like a soft power-down switch for the DRAM, effectively cutting power to the array and drawing substantially less current than it would in any other state (See Table 2 on page 4).

Figure 1 illustrates how TCSR and PASR work together to reduce the self-refresh current, I_{DD6} (DDR) or I_{DD7} (SDR). For full array, I_{DD7} is approximately 450µA at 85°C; while at 25°C, it is less than 150µA.

Figure 1: Self Refresh Current vs. Operating Temperature



Mobile DDR SDRAM Power Calculations

To calculate overall Mobile DRAM power consumption averaged over time, a quantification of the relative amount of time the device spends in standard operational modes is necessary.

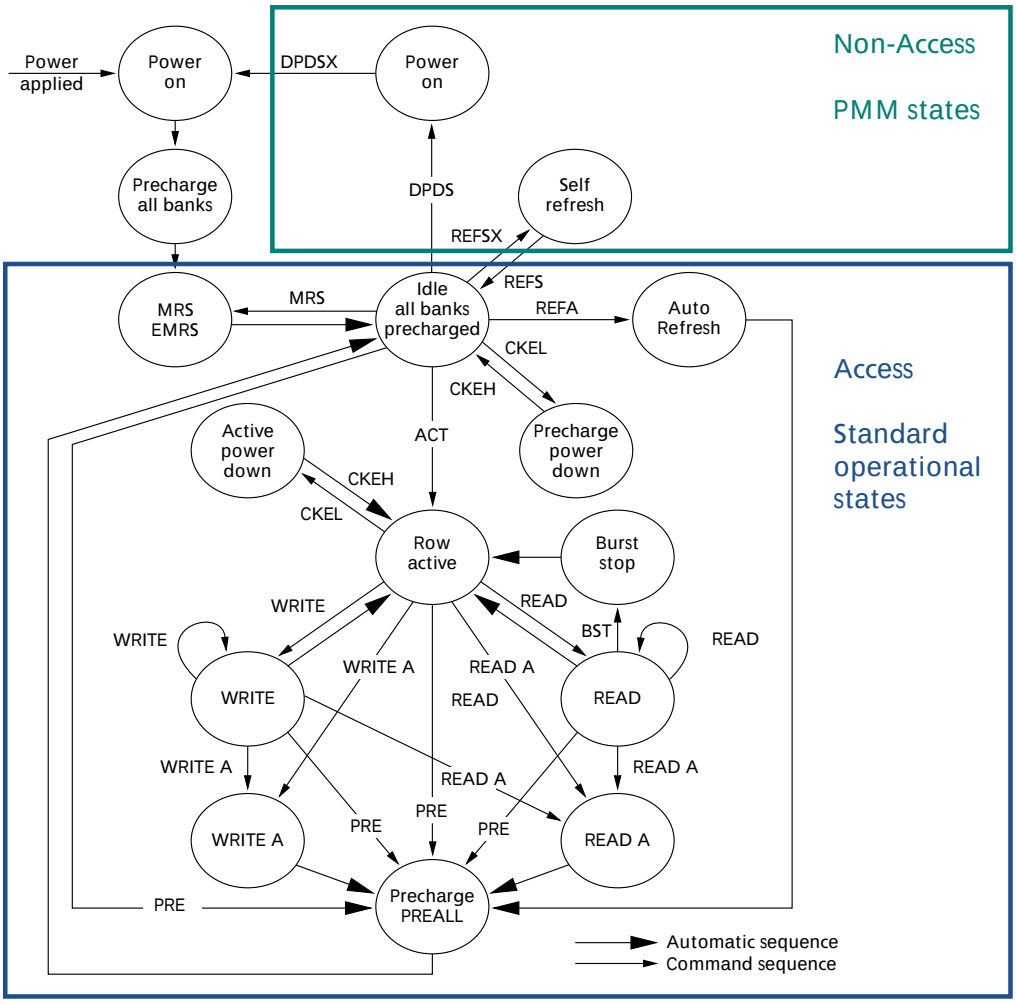
Table 1 on page 2 shows a typical Mobile DDR SDRAM operational scenario or use profile showing the device in power management modes (PMMs) 80 percent of the time (no access to the DRAM) and in standard (active) modes that do involve accesses to the DRAM 20 percent of the time. Figure 2 on page 3 illustrates the differences between standard and PMM operations.

Table 1: Typical Use Profile

Operation	Duty Cycle (Percentage of Clock Cycle)
Power Management Modes	
Deep Power-Down (DPD)	50%
Self Refresh (PASR)	30%
Standard SDRAM Modes	20%

Notes: 1. PASR and DPD are actual PMMs of operation that are entered through explicit commands to the DRAM. Details on how to enter these modes can be found in Micron's Mobile DRAM product data sheets.

Figure 2: Standard Access and PMM Non-Access



Power consumption for the PMMs is calculated by multiplying the power supply voltages (V_{DD}) by the I_{DD} values provided in an actual device data sheet. The values shown in Table 2 are examples for a x16, 133 MHz, Mobile DDR device. (See "Appendix A: Calculating DQ Power" on page 8 for Mobile SDR considerations.) To calculate power consumption for a specific Mobile DRAM device, designers must use the I_{DD} specifications provided in the product data sheet for that device.

Table 2: I_{DD} Specifications (V_{DD}/V_{DDQ} = 1.8V ±0.1V)

Description	Parameter	Max Current (at +85°C)	Units
Operating	I_{DD0}	80	mA
Prech_PD	I_{DD2P}	0.125	mA
Prech_NPD	I_{DD2PS}	0.125	mA
Prech_NPD	I_{DD2N}	25	mA
Prech_NPD (CK stopped)	I_{DD2NS}	15	mA
Act_PD	I_{DD3P}	3	mA
Act_PD (CK stopped)	I_{DD3PS}	3	mA
Act_NPD	I_{DD3N}	25	mA
Act_NPD (CK stopped)	I_{DD3NS}	20	mA
Read	I_{DD4R}	100	mA
Write	I_{DD4W}	90	mA
Auto Refresh (burst)	I_{DD5}	85	mA
Auto Refresh (distributed)	I_{DD5a}	5	mA
Self Refresh (4 bank)	I_{DD6a}	0.3	mA
DPD	I_{DD8}	0.01	mA

Calculating consumption for standard (non-PMM) operational modes is more complex. A thorough discussion of power calculations for standard operations is found in Micron's Technical Note, TN-46-03, "Calculating Memory System Power for DDR," along with a spreadsheet calculator that can be used to calculate power consumption based on actual product specifications. (See Example 3 in TN-46-03.)

The user inputs to the calculator in Table 3 are based on the product specifications provided in Table 2 for a hypothetical Mobile DDR product. In this example the system clock is always clocking the DRAM.

Table 3: Mobile DDR SDRAM Configuration and Data Sheet Parameters

	Condition	Value	Units
	DRAM Density	**512**	Mb
	Number of DQs per DRAM	**16**	
	Number of DQ Strobes (DQs) per DRAM	**2**	
	Speed Grade	**-75**	

Table 3: Mobile DDR SDRAM Configuration and Data Sheet Parameters (continued)

Parameter	Condition	Value	Units
	Maximum V_{DD}	**1.9**	V
	Minimum V_{DD}	**1.7**	V
I_{DD0}	Maximum active precharge	**80**	mA
I_{DD2P}	Maximum precharge power-down standby current	**0.125**	mA
$I_{DD2F/N}$	Maximum precharge standby current	**25**	mA
I_{DD3P}	Maximum active power-down standby current	**3**	mA
I_{DD3N}	Maximum active standby current	**25**	mA
I_{DD4R}	Maximum read burst current	**90**	mA
I_{DD4W}	Maximum write burst current	**85**	mA
I_{DD5A}	Maximum distributed refresh current	**5**	mA
	^{t}CK used for current measurement (see current notes)	**7.5**	ns
^{t}RRD	Minimum activate-to-activate timing (different bank)	**15**	ns
^{t}CK	Minimum activate-to-activate timing (same bank)	**75**	ns
	Minimum ^{t}CK cycle rate	**7.5**	ns
	Maximum ^{t}CK cycle rate	**100**	ns

The user inputs in Table 4 reflect actual operational use conditions specific to this particular Mobile DDR application example.

Table 4: Mobile DDR SDRAM Usage Conditions

Description	Value	Unit	Note
System V_{DD}	**1.8**	V	
System CK frequency	**133**	MHz	
DDR SDRAM output power per individual DQ	**17.3**	mW	The value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme. See Appendix A for more information.
Percentage of time that all banks on the DRAM are in a precharged state	**65%**		See TN-46-03, Example 3 values
Percentage of all bank precharge time that CKE is held LOW	**80%**		See TN-46-03, Example 3 values
Percentage of at least one bank active time that CKE is held LOW	**30%**		See TN-46-03, Example 3 values
The average time between ACT commands to this DRAM (includes ACT to same or different banks in the same DRAM device)	**400**	ns	See TN-46-03, Example 3 values
The percentage of clock cycles that are outputting read data from the DRAM	**10%**		See TN-46-03, Example 3 values
The percentage of clock cycles that are inputting write data to the DRAM	**5%**		See TN-46-03, Example 3 values

A summary of results calculated by the spreadsheet values in Tables 3 and 4 is provided in Table 5.

Table 5: Summary of Standard Operations Power Calculations

Parameter	Power Scaled for Actual System CK Frequency and Vcc	
P(PRE_PDN)	0.11	mW
P(PRE_STBY)	5.53	mW
P(ACT_PDN)	0.54	mW
P(ACT_STBY)	10.42	mW
P(REF)	8.31	mW
P(ACT)	17.59	mW
P(WR)	5.10	mW
P(RD)	11.06	mW
P(DQ)	31.14	mW
P(TOT)	**89.79**	**mW**

The following values must be averaged over time to calculate the overall average power usage for Mobile DRAM while in standard operation and PMMs:

P(Average) = P(Std_modes) × %Std + P(SRef) × %SRef + P(DPD) × %DPD

The above variables are defined as follows:

P(Std_modes) = P(TOT), as defined on in EQ 28 of TN-46-03, which is:
= P(PRE_PDN) + P(PRE_STDBY) + P(ACT_PDN) + P(ACT_STBY) + P(REF) + P(ACT) + P(WR) + P(RD) + P(DQ)
(See Table 5.)

P(SRef) = $I_{DD6a} \times V_{DD}$, where V_{DD} is nominal value for use conditions.
(See Table 2 on page 4 and Table 4 on page 5.)

P(DPD) = $I_{DD8} \times V_{DD}$, where V_{DD} is nominal value for use conditions.
(See Table 2 on page 4 and Table 4 on page 5.)

%Std: Percentage of system operating time the Mobile DRAM is in Std_modes

%SRef: Percentage of system operating time the Mobile DRAM is in PMM - Self Refresh

%DPD: Percentage of system operating time the Mobile DRAM is in PMM - Deep Power-Down

(These three percentages must equal 100% to account for all system operating time, as indicated in Table 1 on page 2.)

The average power consumption over time is:

P(Average) = P(Std_modes) × %Std + P(SRef – 4Bank) × %SRef + P(DPD) × %DPD
= 89.79mW × 20% + 0.3mA × 1.8V × 30% + 0.01mA × 1.8V × 50%
= 89.79mW × 0.20 + 0.54mW × 0.30 + 0.018mW × 0.50
= 17.95mW + 0.16mW + 0.009mW
= 18.12mW

By contrast, if the same Mobile DRAM device was used without the benefit of PMMs, the average power consumption could be something like:

$$\begin{aligned} P(\text{Average}) &= P(\text{Std\_modes}) \times \%\text{Std} \\ &= 89.79\text{mW} \times 100\% \\ &= 89.79\text{mW} \end{aligned}$$

As the equation illustrates, a Mobile DRAM device that does not use PMMs consumes an average of nearly five times more power compared to a device that does use PMMs.

The preceding example indicates how power is calculated for a particular Mobile DDR SDRAM device under specific system operating conditions. Power consumption for a given Mobile DRAM device can vary greatly, depending on how the system accesses the memory in standard operating modes and how the PMM features are used.

Conclusion

In this technical note we have demonstrated how the power calculator described in Micron's technical note TN-46-03 can be used to calculate power consumtpion for standard DRAM access modes. As with standard DRAM products, the manner and frequency with which a Mobile DRAM is accessed substantially impacts power consumption over time. Typical use profiles in mobile systems emphasize Mobile DRAM PMM operation over standard modes of operation.

Appendix A: Calculating DQ Power

Applications for standard DDR SDRAM generally incorporate a termination scheme on the DQ bus for optimizing bandwidth capability; however, termination is often not incorporated in Mobile DRAM applications. To conserve on power dissipation or board space, DQ termination may not be used, so the DQs on the Mobile DRAM only drive a capacitive load. Therefore, the output power for a single DQ is calculated as follows:

$P(\text{per DQ}) = C_{LOAD} \times V_{DDQ}^2 \times (2 \times {}^{f}CK)$,
where the DDR DQ data rate frequency is twice the system clock frequency.

For a 1.8V, 133 MHz, x16 Mobile (DQ) DDR SDRAM product driving a 20pF load:

$P(\text{per DQ}) = 20pF \times (1.8V)\ 2 \times (2 \times 133\ MHz)$
$= 17.3mW$

Total DQ power P(DQ) for all 16 DQs + 2 DQSs, this Mobile DRAM would have:

$P(DQ) = 18 \times P(\text{per DQ})$
$= 311mW$
(Worst case: READs performed 100% of system operating time)

In a realistic operating scenario, READs may only be performed 10 percent of the time. The P(DQ) would only be 31.1mW, as indicated in Table 5, averaged over 100 percent of the system operating time.

In many applications, only half of the DQs are switching per clock cycle. This reduces total power P(DQ) to 155.5mW, or 8.55mW per DQ, and is highly dependent on an application's data pattern reads from the DRAM.

Appendix B: Mobile SDR SDRAM Power Calculations

While this technical note focuses on calculating power for a Mobile DDR SDRAM device, the same techniques can be adapted for use with Mobile SDR SDRAM as well. First, two important differences must be addressed:

1. Calculation of I_{DD0} from I_{DD1}
2. Substitution of I_{DD4} for I_{DD4W} and I_{DD4R}

Industry data sheets for Mobile SDR DRAM often do not specify an I_{DD0} parameter. However, I_{DD1} is specified for a burst of 2 READ. Thus, I_{DD0} is two CK cycles of read current (based on I_{DD4} - I_{DD3}), subtracted from I_{DD1}. This can be calculated as follows:

$$I_{DD0} = I_{DD1} - [(I_{DD4} - I_{DD3N}) \times 2 \times {}^{t}CK / {}^{t}RC]$$

Once I_{DD0} is calculated, I_{DD0} is used in the DDR TN-46-03 equations the same way.

The second difference between the SDR and DDR device is the way I_{DD4} is specified. DDR has I_{DD4W} for WRITE and I_{DD4R} for READ; SDR specifies one I_{DD4} for both. Therefore, $I_{DD4W} = I_{DD4R} = I_{DD4}$.

One other item should be mentioned here. For DDR, self refresh current is referred to as I_{DD6}, while for SDR it is I_{DD7}.

DQ output power calculation for the SDR is calculated similar to the calculations in Appendix A for DDR. However, the equations are slightly altered:

$P(\text{per DQ}) = C_{LOAD} \times V_{DD}{}^{2} \times {}^{f}CK$,
where the DQ data rate is equal to the system clock for SDR, not $2 \times {}^{t}CK$.

Since there are no DQS pins on SDR SDRAM products, total power P(DQ) is calculated as follows:

$P(DQ) = \#\text{ of DQs} \times P(\text{per DQ})$,
where all DQs are switching per clock cycle or:

$P(DQ) = \#\text{ of DQs} \times P(\text{per DQ}) \times 50\%$,
where only half of the DQs typically switch per clock cycle on average.

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Revision History

Rev. B 5/09

- P(Average) equation, first line, bottom of page 6: Added equal sign after P(Average).
- “Appendix B: Mobile SDR SDRAM Power Calculations” on page 9: Updated first equation in section.

Rev. A 10/05

- First draft.