TECHNICAL NOTE

DECOUPLING CAPACITOR CALCULATION FOR A DDR MEMORY CHANNEL

Introduction

The fast switching rates of DDR memory devices require significantly more burst current than previous memory technologies, such as SDRAM. In a worst-case scenario, as many as 81 drivers (64 data, 8 ECC, 9 strobe) may be switching from one state to the other on a memory module. In a pipelined access , the controller may have an additional 28 signals transitioning at the same time. This large burst current generates noise in the supply voltages as charge is drained from decoupling capacitors. Furthermore, the burst current causes supply voltages to drop momentarily until the system power supply, or voltage regulator, can begin recharging the decoupling capacitors.

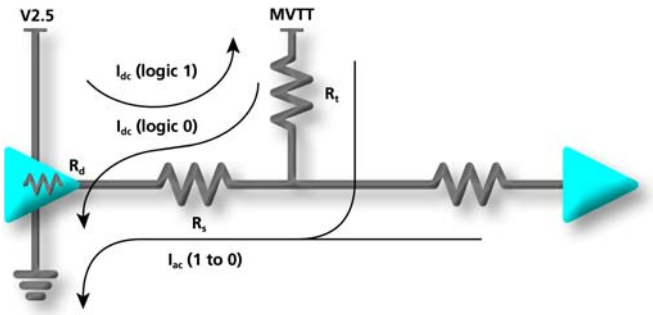
Traditional methods for providing power decoupling involve placing capacitors near the switching device in locations that are convenient based on the routing of the board, and applying some predetermined ratio of caps to driver pins. Unfortunately, the higher switching speeds of DDR may render such typical ratios less than useful. Careful planning and analysis should be performed to ensure that sufficient decoupling is provided.

The following analysis example and recommendations are based on a prototype PC motherboard that supports unbuffered DDR SDRAM. This board was designed and built by Micron Architecture Labs as a reference board for DDR memory.

Current Draw

Total current per net is the combination of steady state current through the termination resistors, I_{dc}, and the switching current through the driver, I_{ac}. I_{dc} is constant until the driver changes state. I_{ac} only flows during the state transition. Because the steady state current transitions from a positive (or negative) level to a negative (or positive) level during the time that I_{ac} is flowing through the driver, it must be accounted for at the same time (see Figure 1).

Figure 1: Current Flow During Logic Transition from 1 to 0



$I_{total} = I_{dc} + I_{ac}$; where I_{dc} = average steady state current through R_s, the series resistor, R_t, the parallel termination resistor, and R_d, the driver resistance. termination resistor. I_{ac} = switching current for one net to change logic states.

As an example, consider a memory channel that supports two double-sided, unbuffered DDR DIMMs, with R_s = 0 ohms, R_d = 13 ohms, and R_t = 39 ohms. Assume that the worst-case switching maintains a 1 V/ns edge rate (see Formula 1).

$$I_{dc} = \left(\frac{V_{DD} - MVTT}{R_s + R_d + R_t}\right) \quad \text{or} \quad I_{dc} = \left(\frac{2.5 - 1.25}{0 + 13 + 39}\right)$$

where:
MVTT = 1.25V
V_{DD} = 2.5V

$$I_{ac} = C\left(\frac{dv}{dt}\right) \quad \text{or} \quad I_{ac} = 30\left(\frac{1.875}{1.5}\right)$$

where:
C = load capacitance
dv = voltage range
dt = 10%–90% rise/fall time

Note: • DDR SDRAM worst-case input capacitance for DQ/DQS = 5pF
• Two double-sided DIMMs = 4 loads per net, 20pF. 2.5pF per inch for a 60 ohm PCB trace. 4 inches of trace would be 10pF. Trace capacitance plus DRAM capacitance is 30pF.
• Voltage switching range at load = 1.875V. 10% to 90% switching time, worst case = 1.5ns.

For this example:
I_{dc} = 24.0mA
I_{ac} = 37.5mA

(f 1)

Inductance

The critical limiting factor in designing a decoupling system is usually not the amount of capacitance. It is the amount of inductance in the capacitor leads and the vias that attach the caps to the power and ground planes. Using 0.1µF caps in a 0603 package should provide sufficient capacitance when the following calculations are used.

Via Inductance

Current flows through a via only to the depth of the plane to which it attaches. For example, on a 0.062" board with the ground plane only 0.004" below the top layer, the effective length of the via would be 0.004". Typically, each decoupling cap attaches to an internal power plane, as well as the ground plane. If the PCB stackup is symmetrical and the same diameter via is used for power and ground, using the length of a single via through the entire thickness of the board is equal to the sum of the via lengths for power and ground. This simplifies the calculation of the via inductance.

NOTE: If via structures for power and ground are different, e.g., two ground vias and one power via, then separate calculations for each structure should be done.

To calculate the via inductance, use the following equation from Johnson & Graham's *High-Speed Digital Design: A Handbook of Black Magic* (see Formula 2).

$$L_{via} = 5.08h\left[\ln\left(\frac{4h}{d}\right) + 1\right] \text{ or } L_{via} = 5.08h\left[\ln\left(\frac{4(0.050)}{0.013}\right) + 1\right]$$

Where:
h = via length
d = via diameter

For this example:
- 0.050" board
- 0.013" via
- L_{via} = 0.948nH

Note: Via sizes are different for the motherboard and DIMM module. For simplification we are using the same values for both.

(f 2)

Maximum Allowable Inductance

The fast switching current induces a voltage drop in the parasitic inductance of the capacitor and the vias that attach it to the voltage planes. From the standard equation V = L(di/dt), L_{max} can be calculated. There are two current paths that ultimately flow through the driver. In the case of a 1-to-0 transition, I_{dc} flows through R_d, R_s and R_t. I_{ac} flows from the charged input gates through R_d and R_s into the ground plane. In the case of a 0-to-1 transition, the same current flows in the other direction from V2.5. The tolerance of MVTT is much tighter than V2.5, therefore, L_{max} for the termination voltage MVTT, should be calculated separately from L_{max} for V2.5. For simplicity of calculations, assume that only I_{dc} flows from MVTT and I_{ac} flows from V2.5. In reality, MVTT contributes to the I_{ac} current flow during the edge transition, but estimating or calculating that contribution would likely not affect the results significantly.

Also note di for MVTT equals twice I_{dc}. This is because I_{dc} transitions from a positive value to a negative value of the same magnitude. I_{ac} transitions from 0 to its maximum value during dt, therefore di for V2.5 = I_{ac} (see Formula 3).

$$L_{max} = \frac{V(dt)}{N(di)} \text{ or } L_{max} = \frac{0.1(1.5 \times 10^{-9})}{109(2 \times 0.024)}$$

Where:
V = MAX allowable voltage drop
dt = 10%–90% switching time
di = current per net
N = number of nets switching simultaneously = 109

Note:
- For di use 2 x I_{dc} for MVTT and I_{ac} for V2.5
- Tolerance specification for MVTT is ±100mV
- Tolerance specification for V2.5 is ±200mV

For this example:
MVTT L_{max} = 0.029nH
V2.5 L_{max} = 0.073nH

(f 3)

Equivalent Inductance per Capacitor

Package inductance for a 0603 cap can vary from manufacturer to manufacturer and from one dielectric type to another. Designers should check component data sheets for the correct inductance value if available (see Formula 4).

For this example:
0603 cap was used with a package inductance of 0.87nH
0603 $L_{eq} = L_{package} + L_{via}$
0603 L_{eq} = 0.87nH + 0.948nH = 1.82nH

(f 4)

Number of Capacitors Needed

To calculate the number of capacitors needed, divide the equivalent inductance of each cap by the maximum allowable inductance, L_{max} (see Formula 5).

$$N_{cap} = L_{eq}/L_{max}$$

For this example:
MVTT N_{cap} = 1.82nH/0.029nH = 63
V2.5 N_{cap} = 1.82nH/0.073nH = 25

(f 5)

The capacitor count for MVTT may be reduced depending on implementation. Some designs may allow MVTT to be implemented on a surface layer island, in which case one terminal of the cap can be attached directly to the plane without a via. Additionally, the effective length of the ground via may be significantly reduced if the PCB stackup has the ground plane immediately below the surface layer. If this is the case (assuming h = .004"), L_{via} = 24.5pH, which is insignificant compared to the capacitor package inductance. Therefore, for surface plane decoupling, assume $L_{eq} = L_{package}$. Given this assumption, the 0603 capacitor count for MVTT would be 31. For internal planes, the 0603 capacitor count equals 63. Because the tolerance on MVTT is so tight, it is recommended that a surface plane or some other method of lowering via inductance be used.

Exceptions and Variations

The equations presented here use a linear approximation of differential quantities such as di/dt. More in-depth calculations can be done to get more accurate predictions. Additionally, each net was assumed to be equally loaded and of the same type. In an unbuffered DDR channel, address, control, and clock signals will be more heavily loaded than data or strobes. These signals are also unidirectional from controller to RAM, and they run at half the speed of data and strobes. Separate calculations can be done to more accurately predict the current flow for these nets.

The capacitor quantities in this example are very dependent on the device parameters used in the calculation. This analysis should be done for each new design as device parameters may be different and will significantly affect the results. For instance, these calculations were based on using R_d = 13 ohms and R_t = 39 ohms. Changing the resistor values to 22 and 29, for example, will increase the amount of I_{dc} per net to 24.5mA. This reduces MVTT_L_{max} and increases the MVTT capacitor count and the V2.5 capacitor count.

Although difficult to predetermine, lower series resistance, R_s will also speed up signal edges, resulting in a larger di/dt quantity. This will increase the number of decoupling caps needed for V2.5.

It is also difficult to predict what value should be used for dt. This is highly dependent on the strength of the driver being used and will vary greatly from one product family to another. Even in a fully loaded configuration, some devices have been measured to have edge rates of 2 V/ns, effectively switching in half the time. These devices meet all of the minimum specs for DDR SDRAMs and might run in the same system with devices that only drive 1 V/ns. But the faster devices switch the same amount of current over a lower dt time, hence they generate significantly more switching noise and, consequently, may require additional decoupling to compensate for the driver strength.

It is recommended that some experimentation be done to determine the right amount of decoupling needed. Use the equations and the most accurate data sheet information available to design a first prototype. Then, measure noise levels on MVTT and V2.5, and edge rates of data and strobes to correlate noise with decoupling amounts. New calculations based on these new measurements will give a more accurate estimate of the decoupling needs of the design.

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