Technical Note

DDR3 Dynamic On-Die Termination

Introduction

DDR3 SDRAM technology has the ability to transfer data at a much higher rate than previously possible. With these improved data rates, designers need options to improve the signal integrity of the data bus, while still maintaining performance. This technical note will describe dynamic on-die termination (ODT), which is a new feature introduced with DDR3 and provides systems with increased flexibility to optimize termination values for different loading conditions.

For optimum signaling, a typical dual-slot system will have a module terminate to a LOW impedance value (30Ω or 40Ω) when in an idle condition. When the module is being accessed during a WRITE operation, greater termination impedance is desired, for example, 60Ω or 120Ω. Dynamic ODT enables the DRAM to switch between HIGH or LOW termination impedance without issuing a mode register set (MRS) command. This is advantageous because it improves bus scheduling and decreases bus idle time.

Mode Register

Table 1: MR1 Settings

A9	A6	A2	Rtt_Nom
0	0	0	Nominal ODT disabled
0	0	1	RZQ/4 (60Ω)
0	1	0	RZQ/2 (120Ω)
0	1	1	RZQ/6 (40Ω)
1	0	0	RZQ/12 (20Ω
1	0	1	RZQ/8 (30Ω)
1	1	0	Reserved
1	1	1	Reserved

Table 2: MR2 Settings

A10	A9	Rtt_WR
0	0	Dynamic ODT disabled
0	1	RZQ/4 (60Ω)
1	0	RZQ/2 (120Ω)
1	1	Reserved

Notes: 1. RZQ is a precision 240Ω calibration resistor that is connected on the DRAM from the ZQ ball to VSSQ.

Operation

When ODT is enabled in the mode register (either Rtt_Nom or Rtt_WR) and the ODT pin is HIGH, the DRAM will terminate DQS, DQS#, DM, and all of the DQ. For a x8 device with TDQS enabled, TDQS and TDQS# pins will also terminate.

ODT consists of two different mode register settings. The primary setting is nominal ODT (Rtt_Nom). This termination value can be used in standby conditions and during WRITE operations. However, with DDR3, termination is not allowed during READ operations. When Rtt_Nom is used during a WRITE operation, only RZQ/2, RZQ/4, and RZQ/6 are available.

Dynamic ODT (Rtt_WR) is only applicable during WRITE cycles. If Rtt_Nom and Rtt_WR are enabled, the DRAM will change termination from the Rtt_Nom value to the Rtt_WR value upon issuing the WRITE command. When the WRITE burst is complete, the termination will change back to the Rtt_Nom value. These termination changes are performed without having to issue additional MRS commands.

Rtt_Nom does not have to be enabled to use dynamic ODT. Rtt_Nom and Rtt_WR may be used independently. If Rtt_Nom is disabled and Rtt_WR is enabled via the MR, the DRAM will only terminate during WRITE operations. This ability to operate independently is particularly useful in DDR3 quad-rank configurations, where the ODT pin is tied HIGH on two of the ranks.

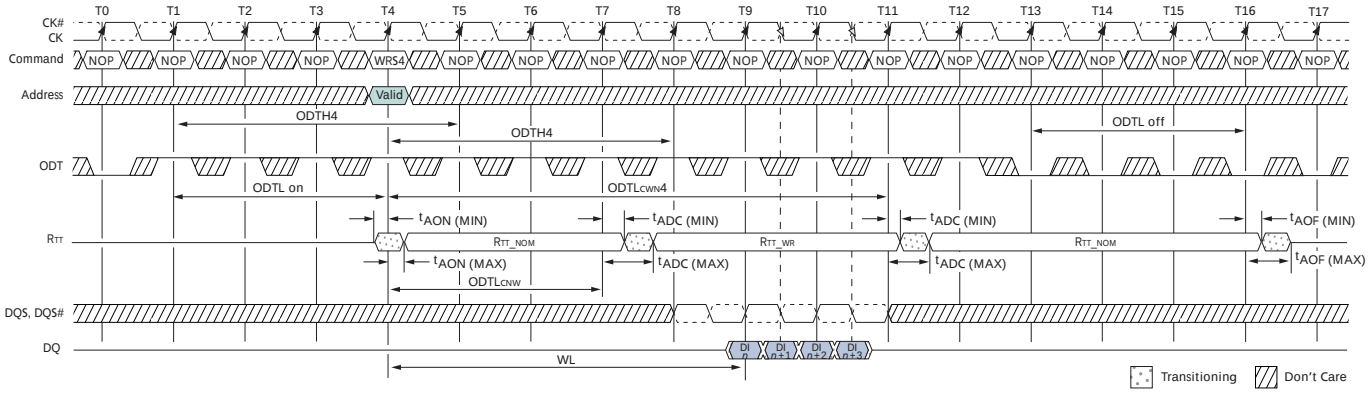
Timing

Table 3: Dynamic ODT Specific Timing

Symbol	Description	Begins At	Defined To	Definition for all DDR3 Speed Bins	Units
ODTLCNW	Change from Rtt_Nom to Rtt_WR	Write registration	Rtt switched from Rtt_Nom to Rtt_WR	WL - 2	^{t}CK
ODTLCNW4	Change from Rtt_WR to Rtt_Nom (BC4)	Write registration	Rtt switched from Rtt_WR to Rtt_Nom	4^{t}CK + ODTLoff	^{t}CK
ODTLCNW8	Change from Rtt_WR to Rtt_Nom (BL8)	Write registration	Rtt switched from Rtt_WR to Rtt_Nom	6^{t}CK + ODTLoff	^{t}CK
^{t}ADC	Rtt change skew	ODTLCNW complete	Rtt transition complete	0.5^{t}CK ±0.2^{t}CK	^{t}CK

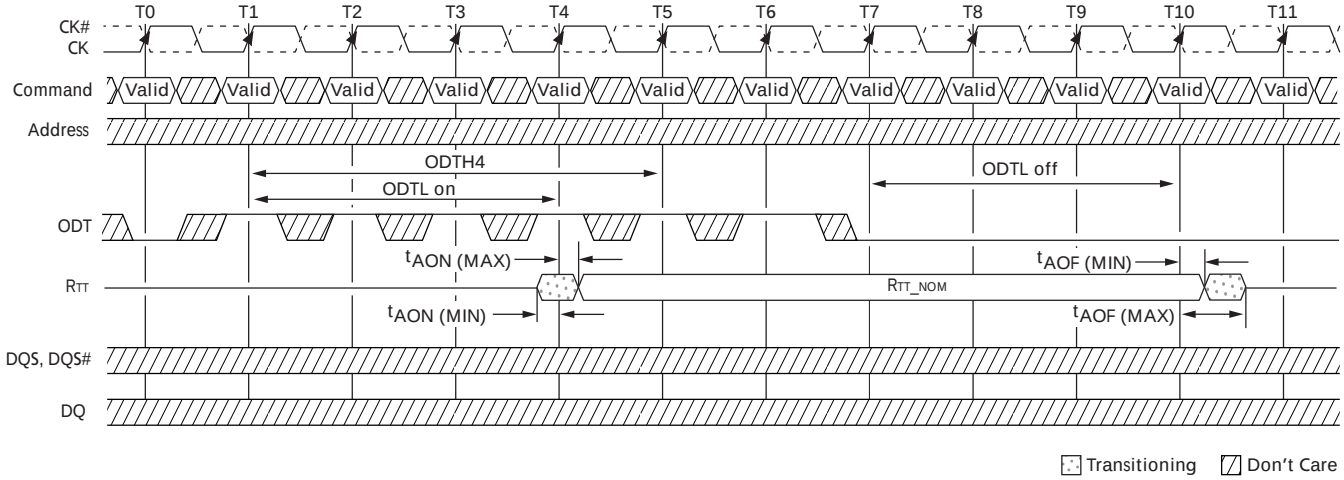
Figure 1 on page 3 shows a typical timing sequence using both nominal ODT and dynamic ODT. Both Rtt_Nom and Rtt_WR are enabled via the mode register. At T1, the ODT pin is asserted HIGH and the Rtt synchronous turn-on delay (ODTLon) begins.

Figure 1: Dynamic ODT – ODT Asserted Before and After WRITE, BC4



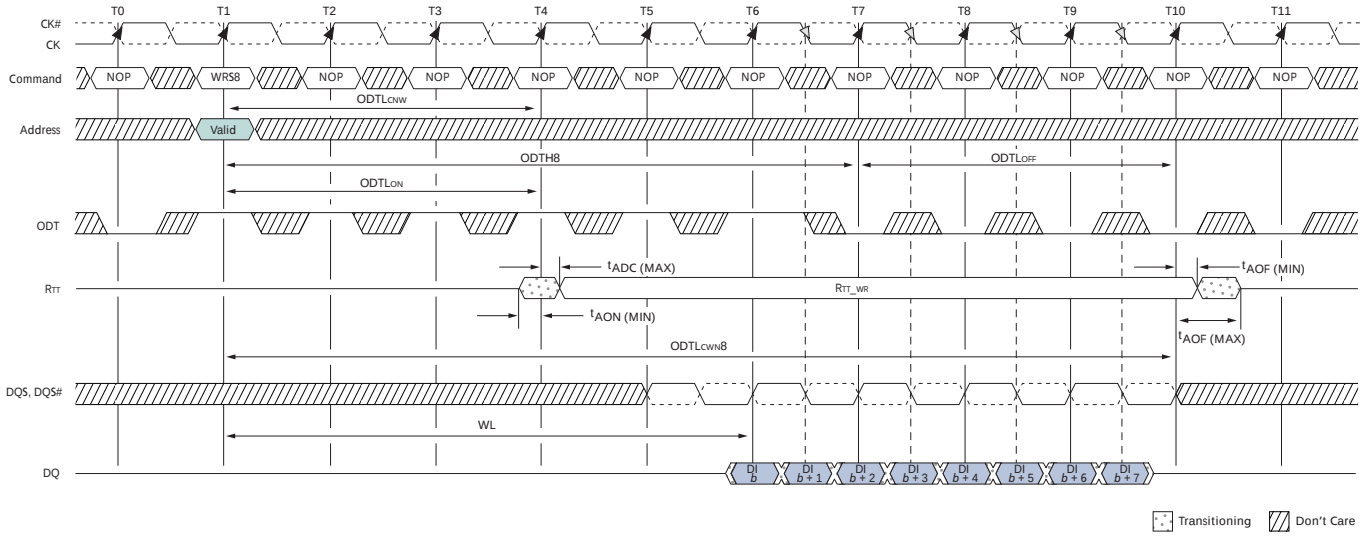
Notes:
1. Via MRS or OTF. AL = 0, CWL = 5. Rtt_Nom and Rtt_WR are enabled.
2. ODTH4 applies to first registering ODT HIGH and then to the registration of the WRITE command. In this example, ODTH4 is satisfied if ODT goes LOW at T8 (four clocks after WRITE command).

Figure 2: Dynamic ODT – Without WRITE



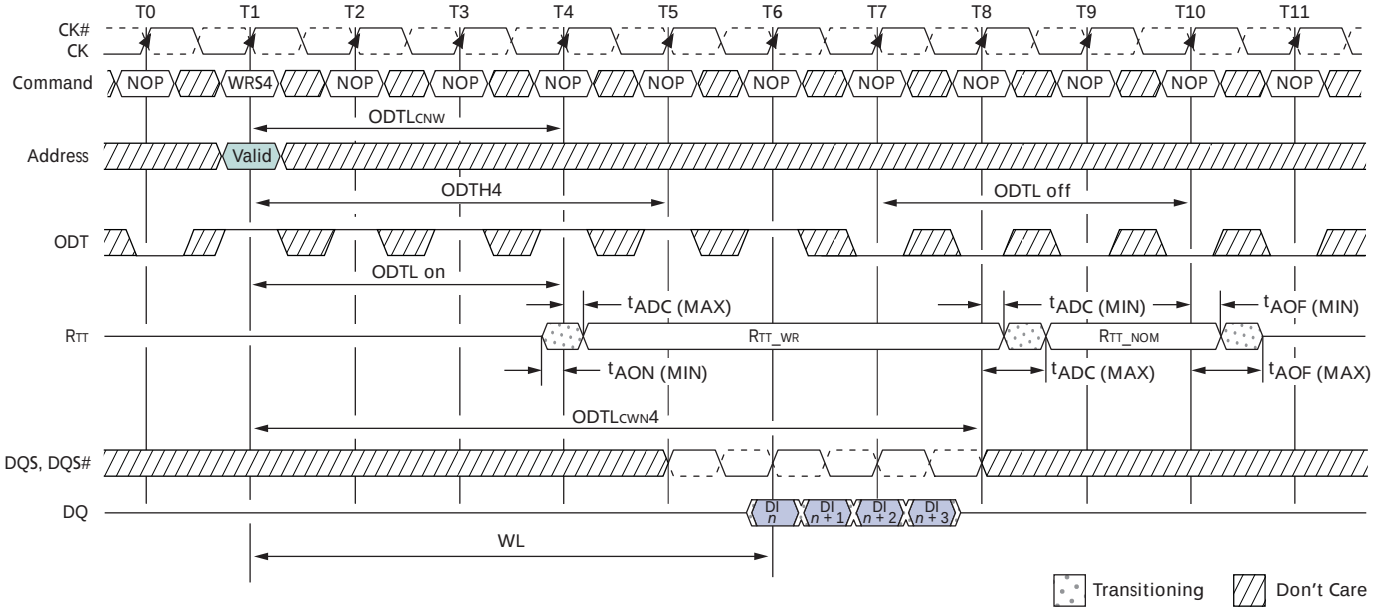
Notes:
1. AL = 0, CWL = 5. Rtt_Nom is enabled, and Rtt_WR either is enabled or disabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW. In this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

Figure 3: Dynamic ODT – ODT Pin Asserted With WRITE for 6 Clock Cycles, BL8



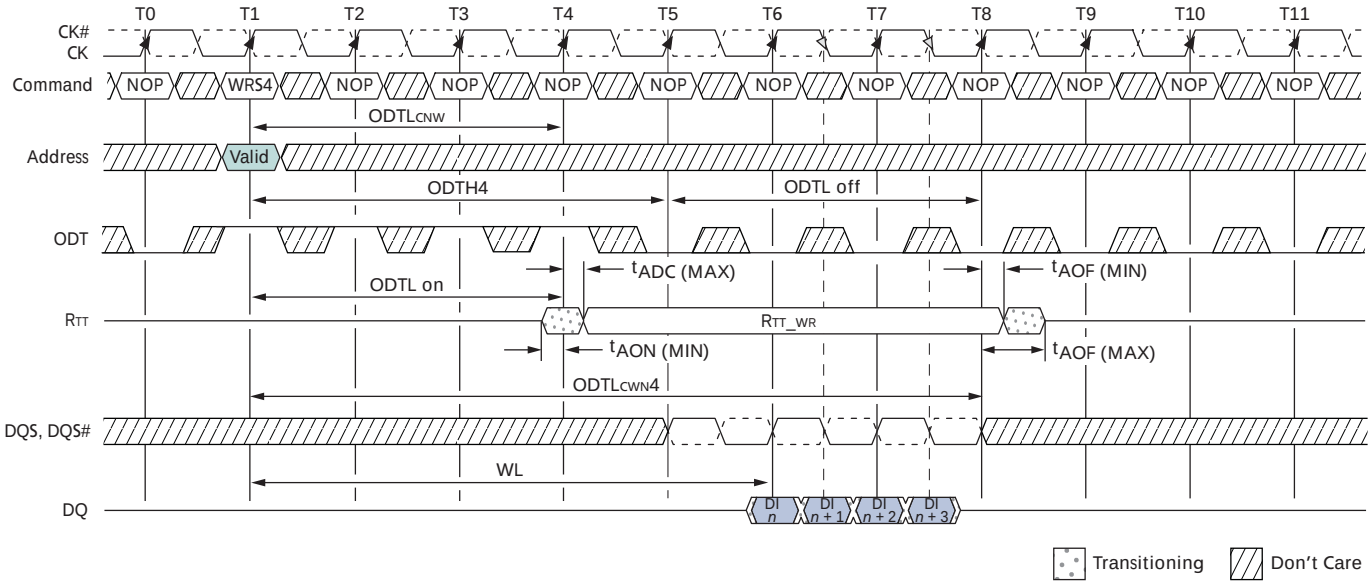
Notes:
1. Via MRS or OTF. AL = 0, CWL = 5. If Rtt_Nom either can be enabled or disabled, ODT can be HIGH. Rtt_WR is enabled.
2. In this example, ODTH8 = 6 is satisfied exactly.

Figure 4: Dynamic ODT – ODT Pin Asserted With WRITE for 6 Clock Cycles, BC4



Notes:
1. Via MRS or OTF. AL = 0, CWL = 5. Rtt_Nom and Rtt_WR are enabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW. In this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

Figure 5: Dynamic ODT – ODT Pin Asserted With WRITE for 4 Clock Cycles, BC4



Notes:
1. Via MRS or OTF. AL = 0, CWL = 5. Rtt_Nom either can be enabled or disabled. If disabled, ODT can remain HIGH. Rtt_WR is enabled.
2. In this example, ODTH4 = 4 is satisfied.

Conclusion

ODT reduces the amount of jitter at the module being accessed and decreases reflections from any secondary modules. This improvement in signal integrity ensures a more predictable, open data eye. Dynamic ODT improves bus scheduling with seamless transitions between nominal and write termination values without having to perform MRS commands.

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