Verilog Model: M25Pxx memory

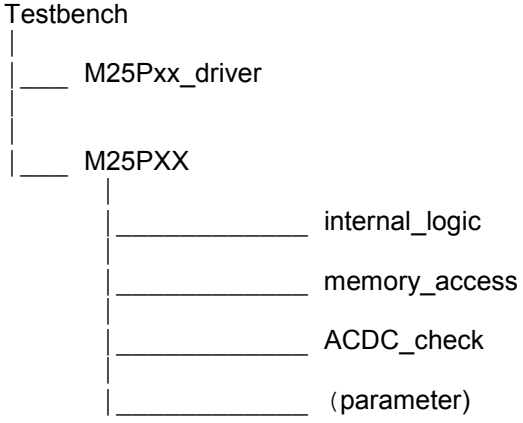
WARNING:
These Verilog models are provided "as is" without warranty of any kind, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose.

PROJECT ARCHITECTURE

a) The Verilog simulation of the M25Pxx SERIAL FLASH is the *M25Pxx.v* file.
b) In order to offer an example of a complete Verilog project, some other Verilog files are offered and this project is based on two blocks:

- the *M25Pxx_driver* block which defines the instructions to transmit to the M25Pxx memory
- the *M25Pxx* block which simulates the behaviour of the M25Pxx memory.

These two blocks are called by *Testbench.v*.



When compiling all blocks, the project must compile them with the following order:

- parameter.v
- internal_logic.v
- memory_access.v
- ACDC_check.v
- M25Pxx.v
- M25Pxx_driver.v
- Testbench.v

VERILOG BLOCKS DESCRIPTION

Parameter.v
Defines the M25PXX memory device: memory size, page size and AC/DC parameters Min/Max values..

internal_logic.v
Decodes the SPI protocol and prepares actions for further operations to be performed in the memory array.

memory_access.v
Simulates the memory array contents. This contents can be initialized (with the initialization file, see the last paragraph of this document).

ACDC_check.v
Performs all checks to be done on received AC values.

M25PXX.v
Defines the M25Pxx memory device: calls the internal_logic.v, memory_access.v and parameter.v modules.

M25Pxx_driver.v
Simulates an SPI bus Master transmitting instructions to the M25Pxx. Stimuli of instructions are defineded in *M25Pxx_driver.v*

Testbench.v
Links the *M25Pxx_driver.vhd* to the *M25Pxx.v (simulates SPI Master-Memories communications)*.

MESSAGES WHEN RUNNING A SIMULATION

When running a simulation, the M25Pxx Verilog model might send warning messages with several severity levels, as commonly used in most Verilog simulators:

Lowest severity

- Note
  - A note message is only informative.
- Warning
  - A warning message informs the user that the M25Pxx Verilog model is not properly driven (through the SPI bus) and that the SPI sequence is not compliant with the M25Pxx specification
- Error
  - An error message also informs the user that the M25Pxx Verilog model is not properly driven (through the SPI bus) and that the SPI sequence is not compliant with the M25Pxx specification.
  - An ERROR message stops the simulation.

Highest severity

Note: although most Verilog development packs offer the possibility to change the severity level in the options menu, it is recommended to keep the initial severity levels (above) as this will insure the safest application check under Verilog.

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HOW TO USE THE INITIALIZATION FILE

Default state

An initialization file (*initmemory.txt*) is offered to define the content of the memory array before the simulation starts.

Initialize the memory with your own content

The *initmemory.txt* file is a parameter of the *M25Pxx.v* memory model and can be customized in the *Testbench.vhd* module.

The example hereafter shows how to define two M25Pxx memories (connected to the same SPI bus) with a different initialization content (named in this example: *initmemory1.txt* and *initmemory2.txt*).

```
-------------------------------------------------------
-----------  Testbench module Declaration    ------------
-------------------------------------------------------
module testbench();

   wire clock;
   wire data;
   wire w;
   wire hold;
   wire out;
   wire select;

defparam memory.mem_access.initfile = "initmemory1.txt";
m25p05a    memory1(.c(clock),.data_in(data),.s(select),.w(w),.hold(hold),.data_out(out));

defparam memory1.mem_access.initfile = "initmemory2.txt";
m25p05a    memory2(.c(clock),.data_in(data),.s(select),.w(w),.hold(hold),.data_out(out));


m25p05a_driver
tester(.clk(clock),.din(data),.cs_valid(select),.hard_protect(w),.hold(hold));

endmodule
```

The format used to define this *Initmemory.txt* initialization file is:

- Each byte is defined in Hexadecimal, using two ASCII characters.
- Bytes are separated by a " " blank character.
- Bytes are packed into lines of N bytes, N being the 25Pxx page size
- Each line (page) ends with a <CR> (carriage return).

The M25Pxx Verilog model package provides a software tool to convert .BIN files into .txt initialization files. The use of the converter1.1 utility is illustrated below:

- Launch converter1.1 (double click on converter1.1.exe as an example),
- Enter .BIN file name (init.bin as an example)
- Enter .TXT destination file for memory model initialization (initmemory.txt as an example)
- When conversion is finished, the tool window is automatically closed and the .TXT file is available in the converter1.1 directory.