IBIS/HSpice Model Quality Report

Design ID: **Z01B**
Description: **8Gb DDR4 SDRAM**
Marketing device name(s): **MT40A2G4WE, MT40A1G8WE, MT40A512M16LY, MT40A2G4Z01B, MT40A1G8Z01B, MT40A512M16Z01B**
Valid speed grades: **DDR4-1600, DDR4-1866, DDR4-2133, DDR4-2400, DDR4-2666, DDR4-2933, DDR4-3200** [1]
Zip filename: **z01b_ibis.zip**
IBIS filename (Version 4.2): **z01b.ibs** **File rev:** **1.1**
IBIS filename (Version 5.0): **z01b_v5p0.ibs** **File rev:** **1.1**
HSpice filename: **z01b_hspice.zip** **File rev:** **1.1**
EBD filename (if applicable): **File rev:**
Die rev: **D**
Date: **October 18, 2016**
Datasheet link: **NA**

E-mail modelsupport@micron.com for questions regarding Quality Report.

Device Parameters

VDDQ – Slow: **1.140V** **Typical:** **1.200V** **Fast:** **1.260V**
VDD – Slow: **1.140V** **Typical:** **1.200V** **Fast:** **1.260V**
Junction Temperature (Commercial) - Slow: **110C** **Typical:** **50C** **Fast:** **0C**
VDDQ/VSSQ Decoupling Capacitance: **18.61nF**
Included in HSPICE DQ/DQS models? **Yes** **Amount per DQ/DQS model:** **846pF/1.692nF**
Included in IBIS DQ/DQS/DM models? **No, must be included with separate Spice subcircuit.**
VDDQ/VSSQ Decoupling Capacitance Series Resistance: **1.2 Ohms/DQ**

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IBIS Quality Summary

1. ☒ Include the IBIS Quality Specification 2.0 Overall IBIS Quality level. For details on IBIS Quality, reference the quality specification and quality checklist on IBIS quality webpage http://www.eda.org/pub/ibis/quality_wip/.

   Overall IBIS Quality Level: IQ3SX
   Exceptions: V-t length in Version 5.0 model is excessive due to inclusion of [Composite Current] I-t data.

2. ☒ Include the filename of the IBIS Quality Checklist that accompanies this report.

   Filename for Version 4.2 file: z01b_ibis_quality_checklist.xls
   Filename for Version 5.0 file: z01b_v5p0_ibis_quality_checklist.xls

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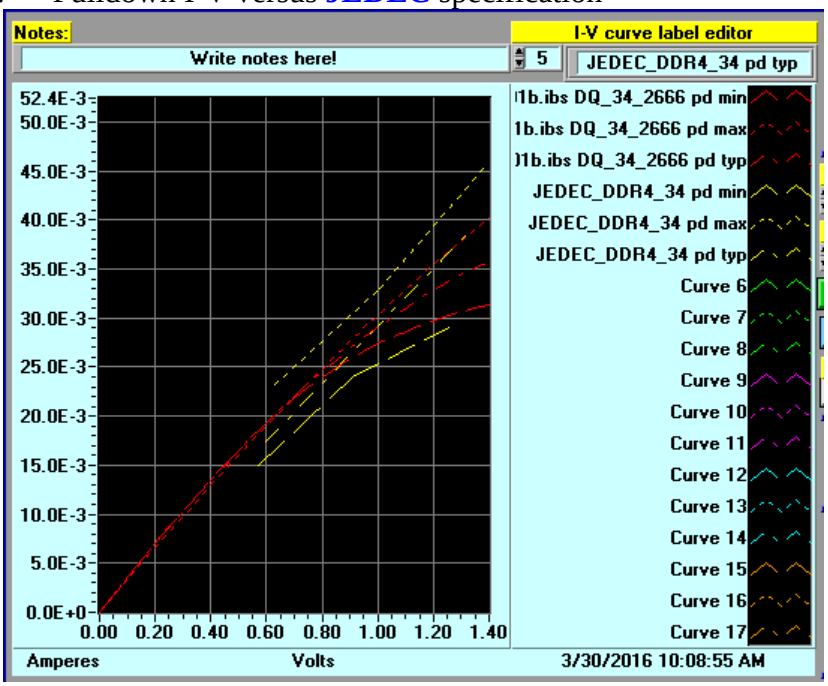
IBIS MODEL Correlation

Datasheet Correlation

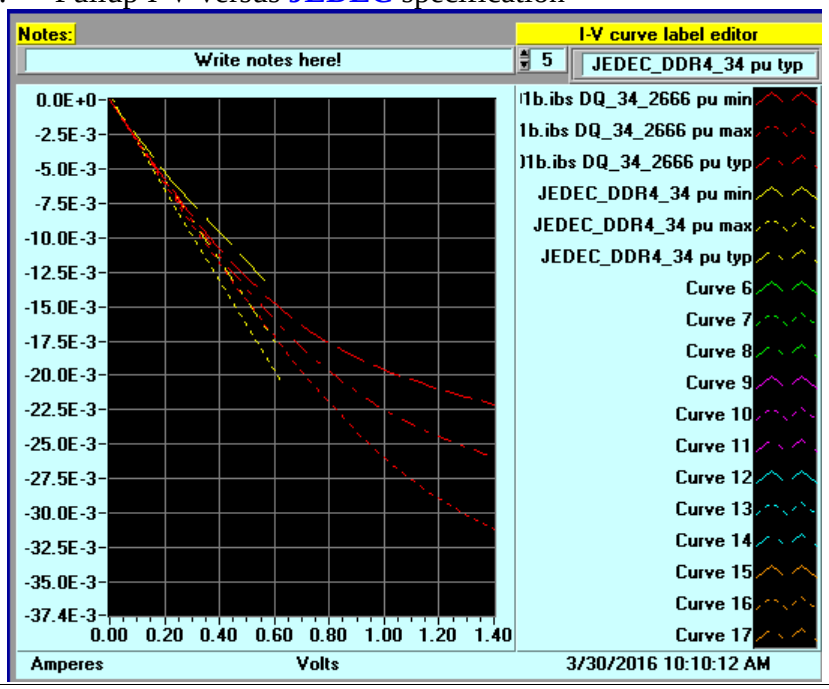
1. ☒ For Output or I/O model compare datasheet IOH/IOL data with IBIS pullup/pulldown data.

a) Model name: **DQ_34_2666**

i. Pulldown I-V versus **JEDEC** specification



ii. Pullup I-V versus **JEDEC** specification



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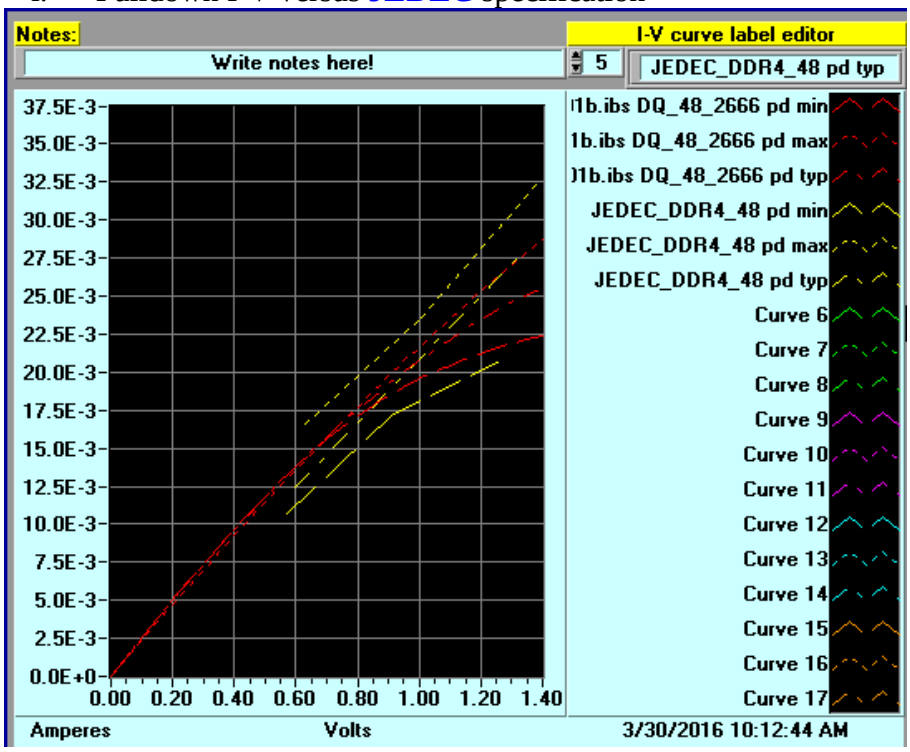
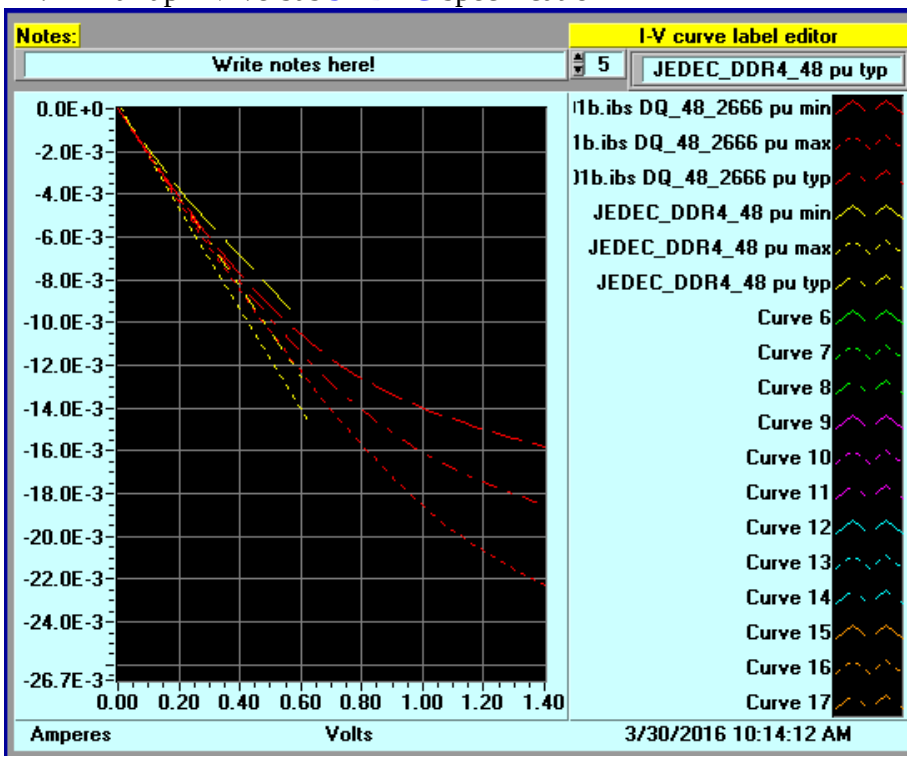
b) Model name: **DQ_48_2666**

i. Pulldown I-V versus **JEDEC** specification



ii. Pullup I-V versus **JEDEC** specification



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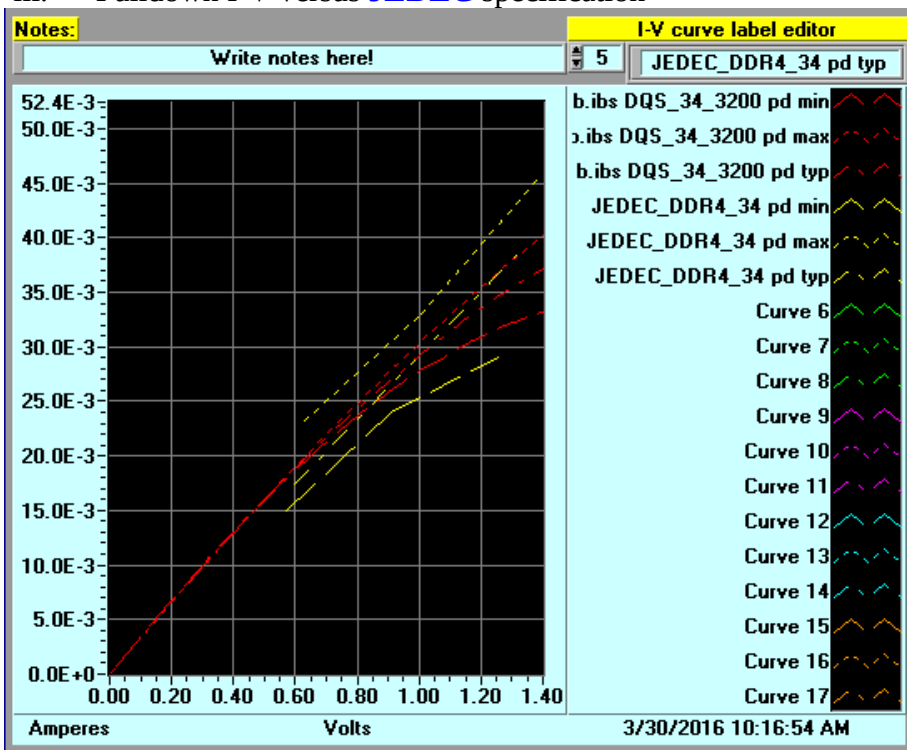
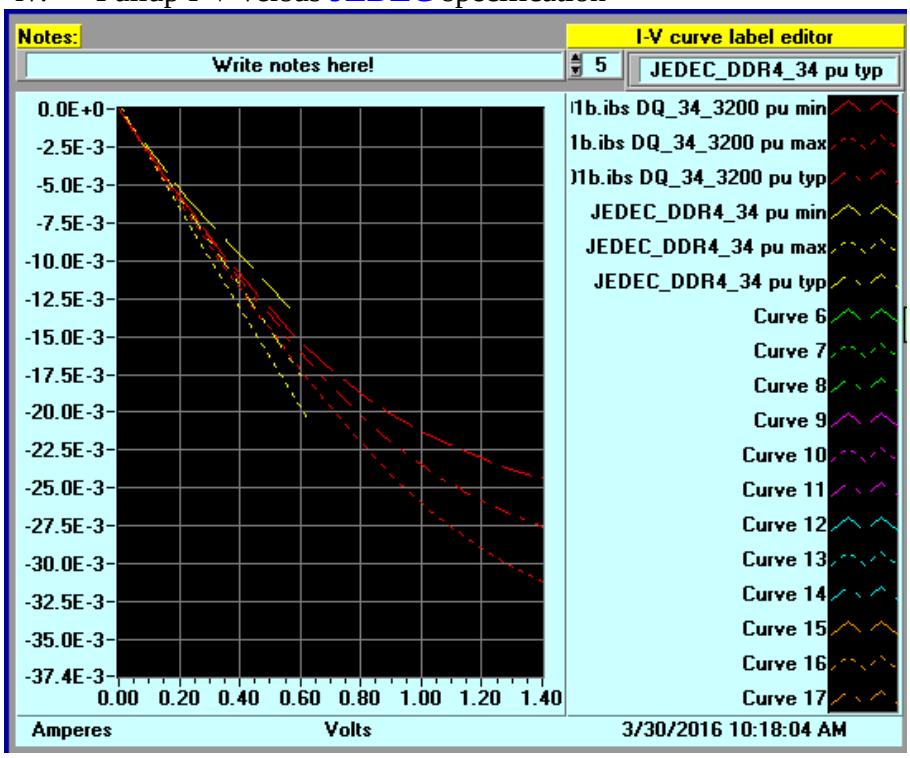
c) Model name: **DQ_34_3200**

iii. Pulldown I-V versus **JEDEC** specification



iv. Pullup I-V versus **JEDEC** specification



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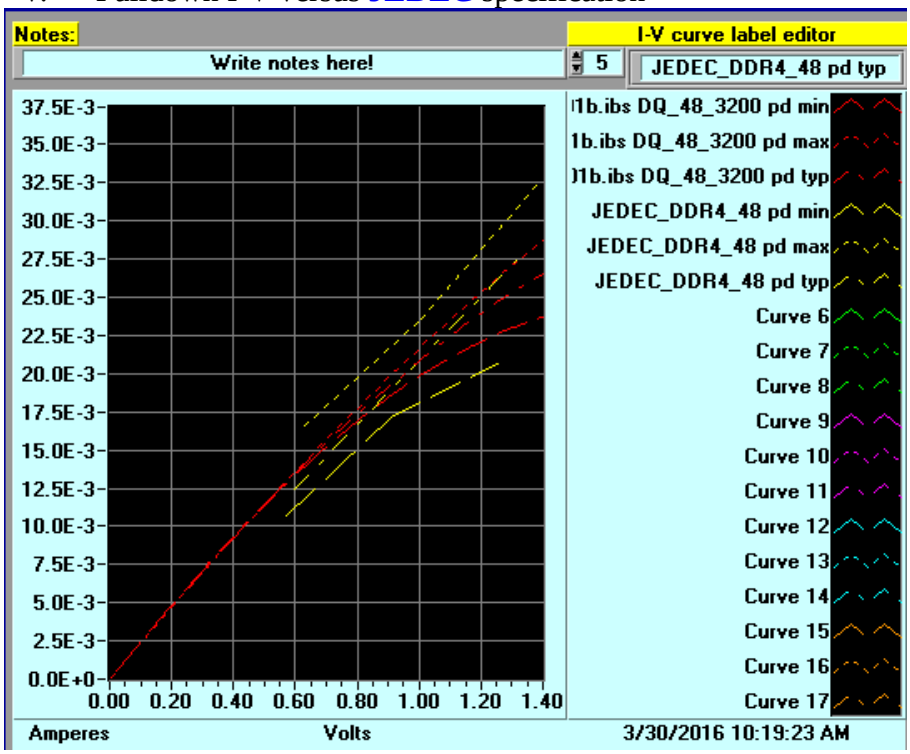
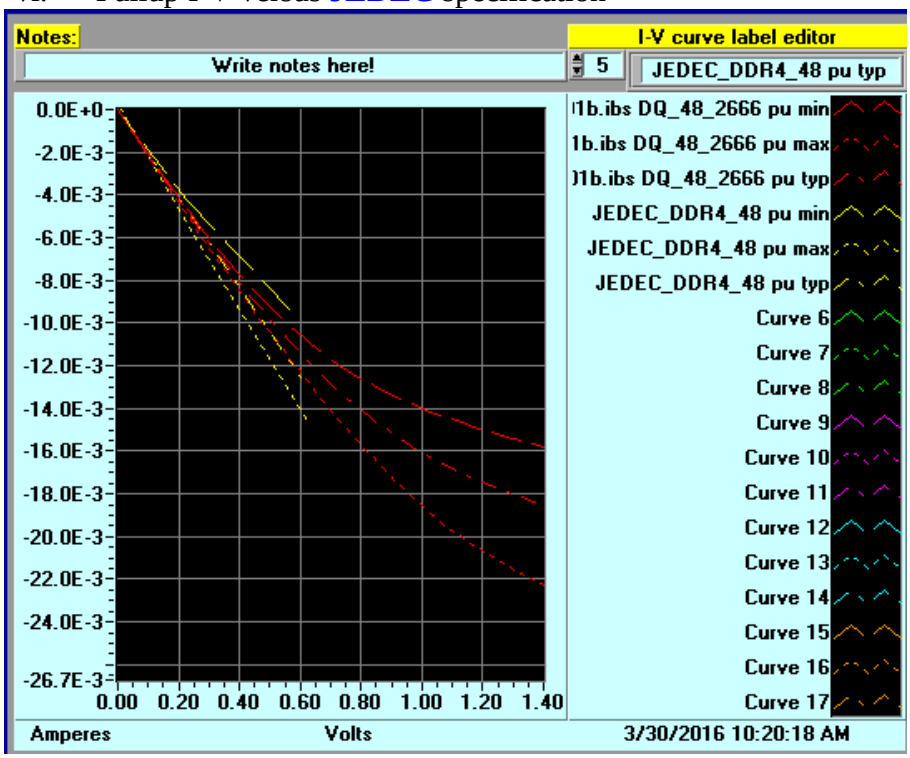
d) Model name: **DQ_48_3200**

v. Pulldown I-V versus **JEDEC** specification



vi. Pullup I-V versus **JEDEC** specification



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2. ☒ Compare C_comp with datasheet Input C. Provide C_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16).

Component name: **Bare Die**

	C_comp IBIS (pF)		Cin Datasheet (pF)	
	min	max	min	max
DQ	0.824	0.924	0.70	1.40
INPUT	0.369	0.469	0.20	0.80
CLK	0.385	0.485	0.20	0.80
ALERT	0.856	0.956	0.50	1.50

3. ☒ Compare package impedance and time delay with datasheet specifications. Provide comparison table for all package combinations.

Component name: **MT40A1G8WE, MT40A2G4WE (78-Ball, x4/x8)**

	Z_pkg IBIS (Ω)		Z_pkg Datasheet (Ω)		Td_pkg IBIS (ps)		Td_pkg Datasheet (ps	
	min	max	min	max	min	max	min	max
IO	56.4	66.8	50	85	28.4	32.4	14	37
ADD/CMD	55.3	77.1	55	90	28.8	40.4	14	36
CTRL	70.2	73.5	55	90	31.0	32.4	14	36
CLK	64.6	65.3	60	90	31.7	31.7	14	34
ALERT	55.3	55.3	40	100	40.4	40.4	20	55

Component name: **MT40A512M16LY (96-Ball, x16)**

	Z_pkg IBIS (Ω)		Z_pkg Datasheet (Ω)		Td_pkg IBIS (ps)		Td_pkg Datasheet (ps	
	min	max	min	max	min	max	min	max
IO	56.4	66.8	50	85	28.4	32.4	14	37
ADD/CMD	69.1	77.1	55	90	28.8	32.8	14	36
CTRL	70.2	77.1	55	90	31.0	32.4	14	36
CLK	64.6	65.3	60	90	31.7	31.7	14	34
ALERT	55.3	55.3	40	100	40.4	40.4	20	55

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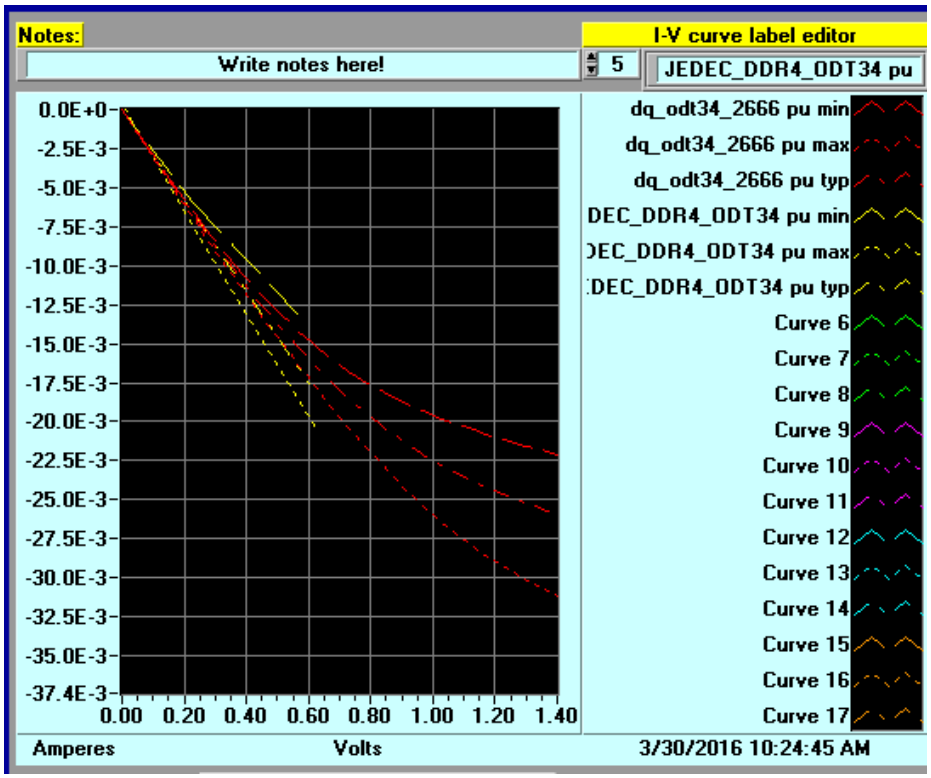
4. ☒ If slew rate specifications (rise/fall slew) are available from the datasheet, complete Spice simulations to generate slew rate data and provide a comparison table.

		IBIS simulation			Datasheet	
Model	**Slew Rate (V/ns)**	**min**	**typ**	**max**	**min**	**max**
DQ_34_2666	Rising	4.39	6.66	8.89	4.00	9.00
	Falling	4.52	6.86	8.72	4.00	9.00
DQ_34_3200	Rising	5.49	7.35	8.66	4.00	9.00
	Falling	5.54	7.19	8.76	4.00	9.00

5. ☒ Compare ODT data with datasheet.

a. **ODT34**



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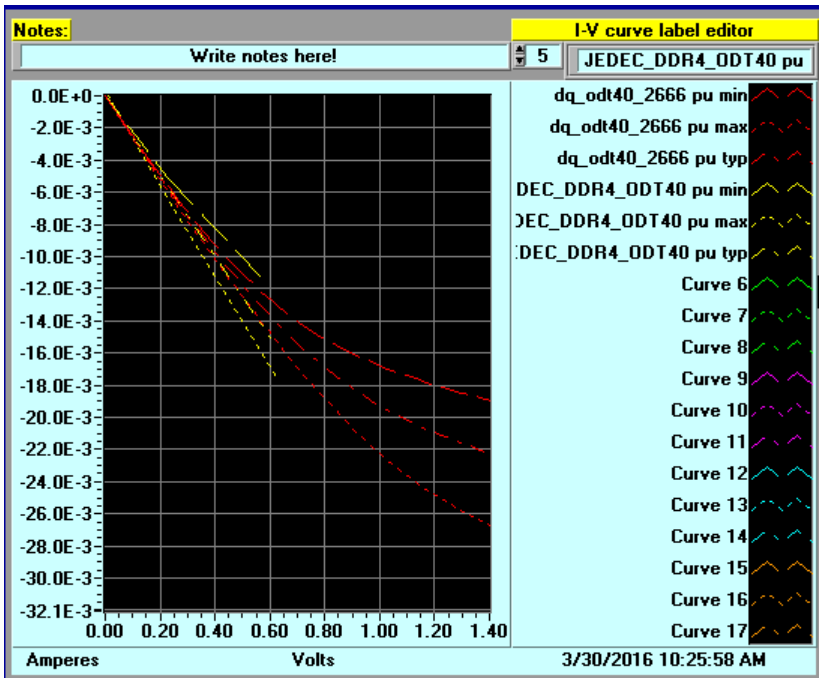
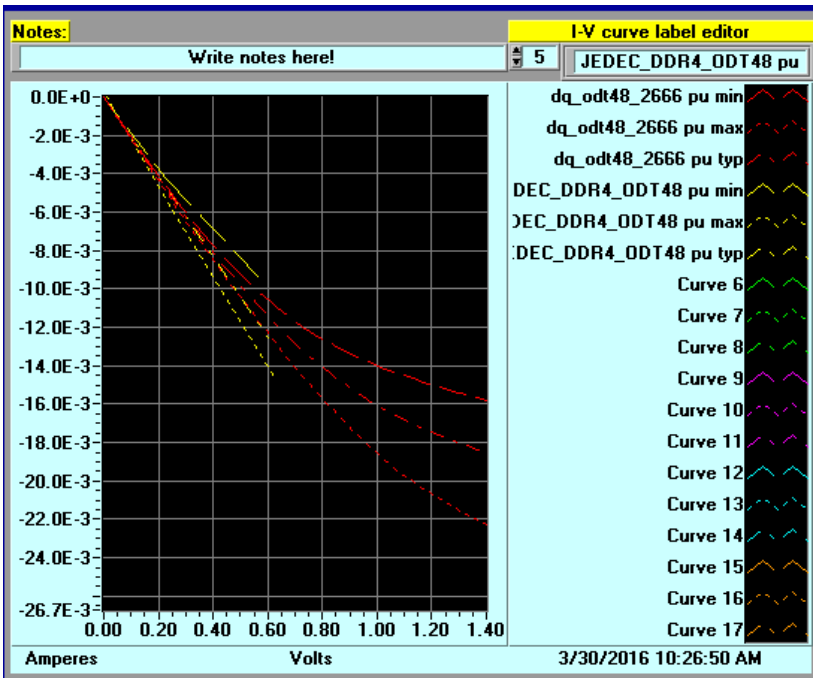
b. **ODT40**



c. **ODT48**



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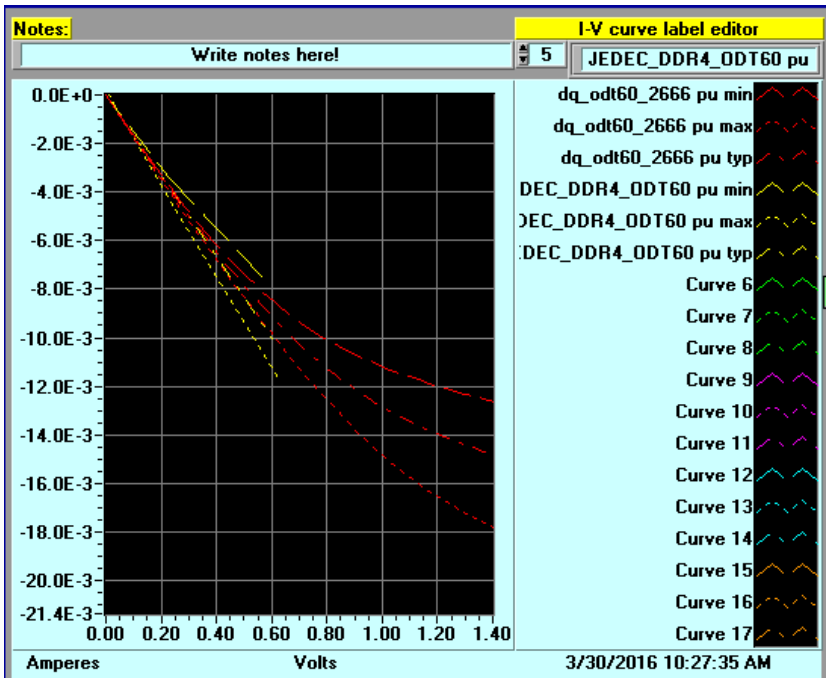
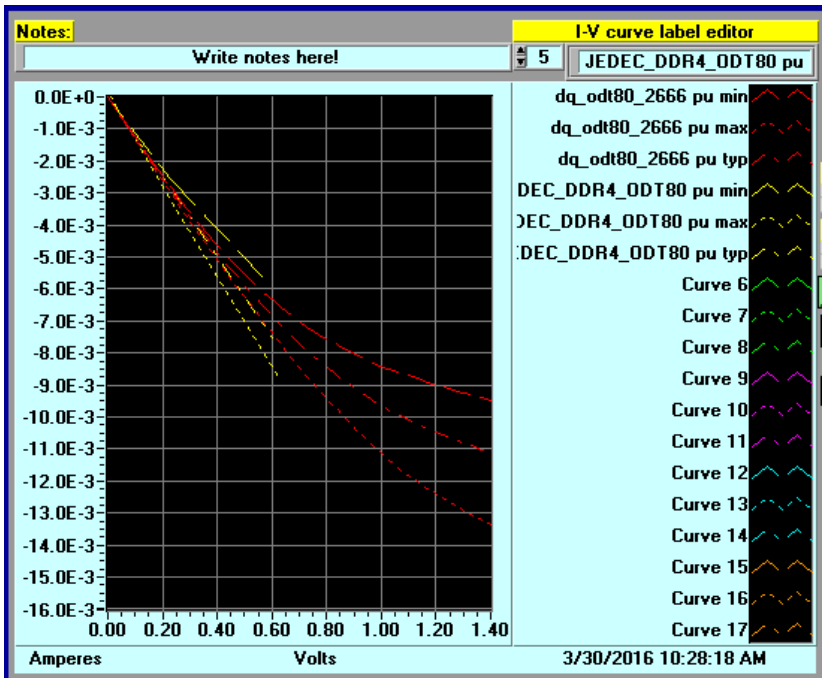
d. **ODT60**



e. **ODT80**



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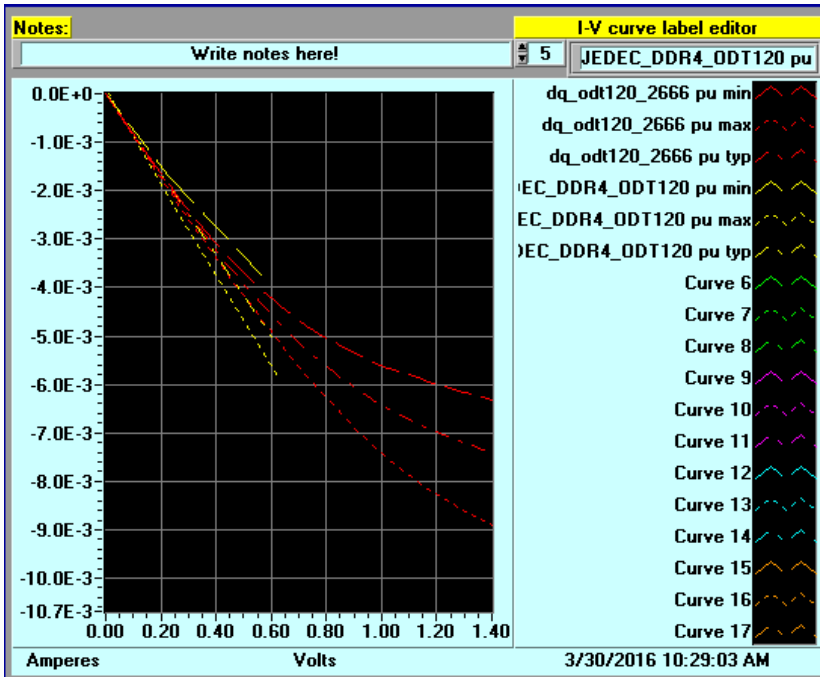
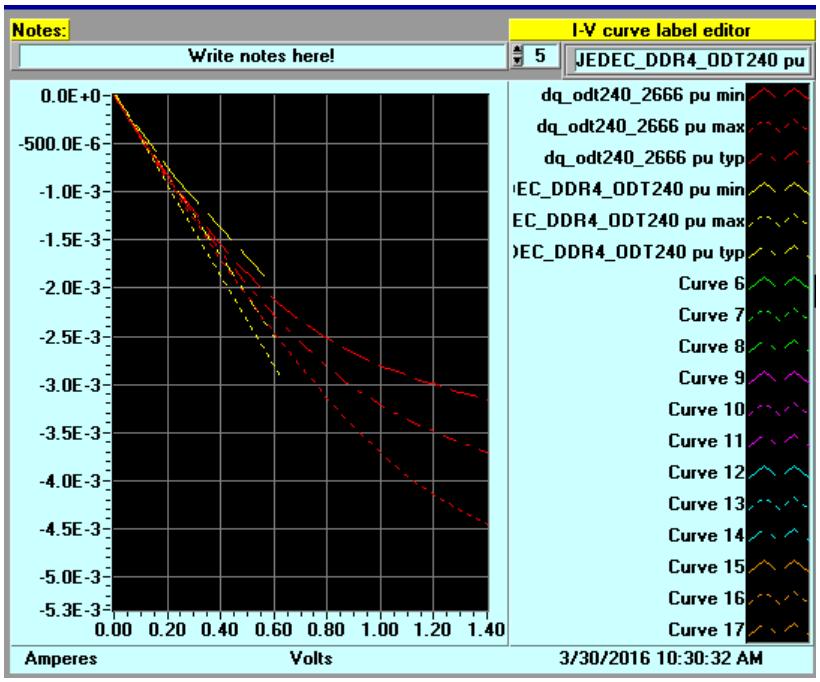
f. **ODT120**



g. **ODT240**



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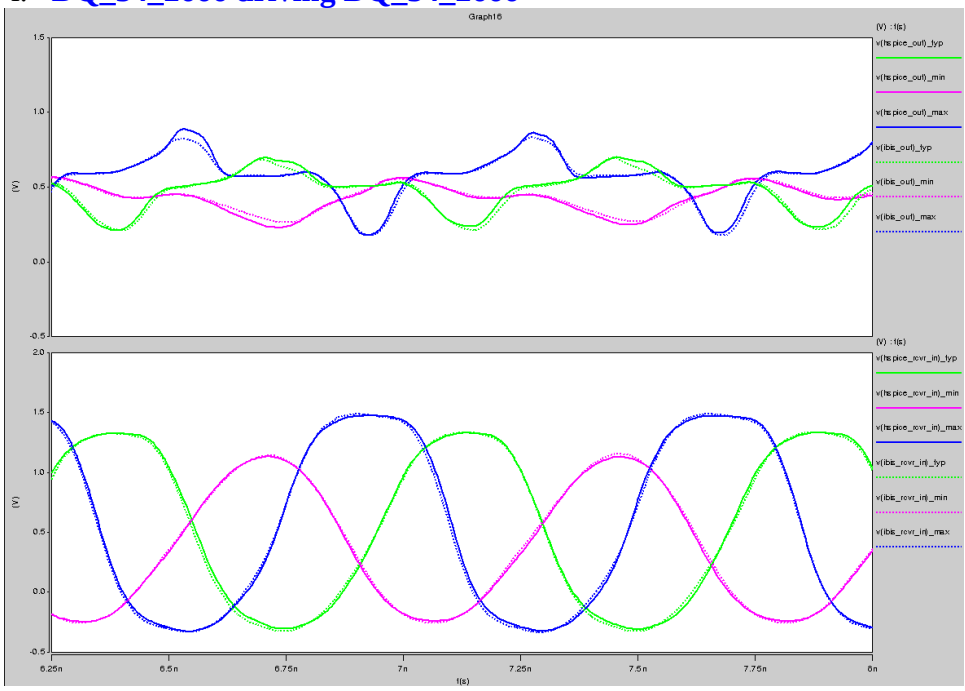
IBIS vs Spice Correlation

1. ☒ For all Output or I/O models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element).
   a. ☒ Use the setup and node naming conventions shown below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations: **HSPICE 2013.03-SP1**
   b. ☒ Run simulations for all corners cases and at fastest speed grades, testing ODT models as loads when applicable.

      i. **DQ_34_2666 driving DQ_34_2666**



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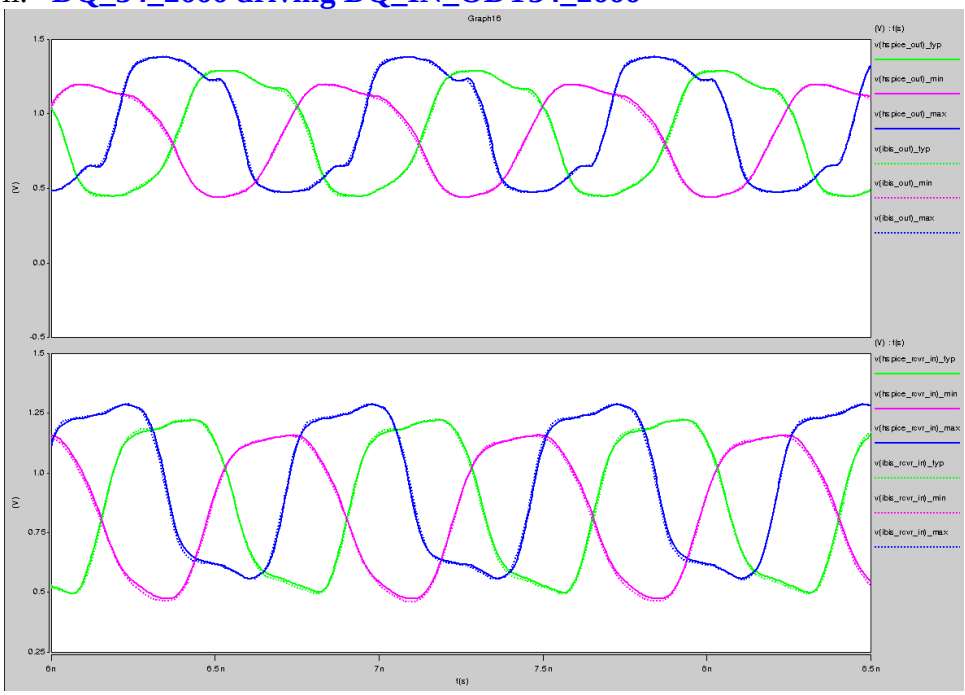
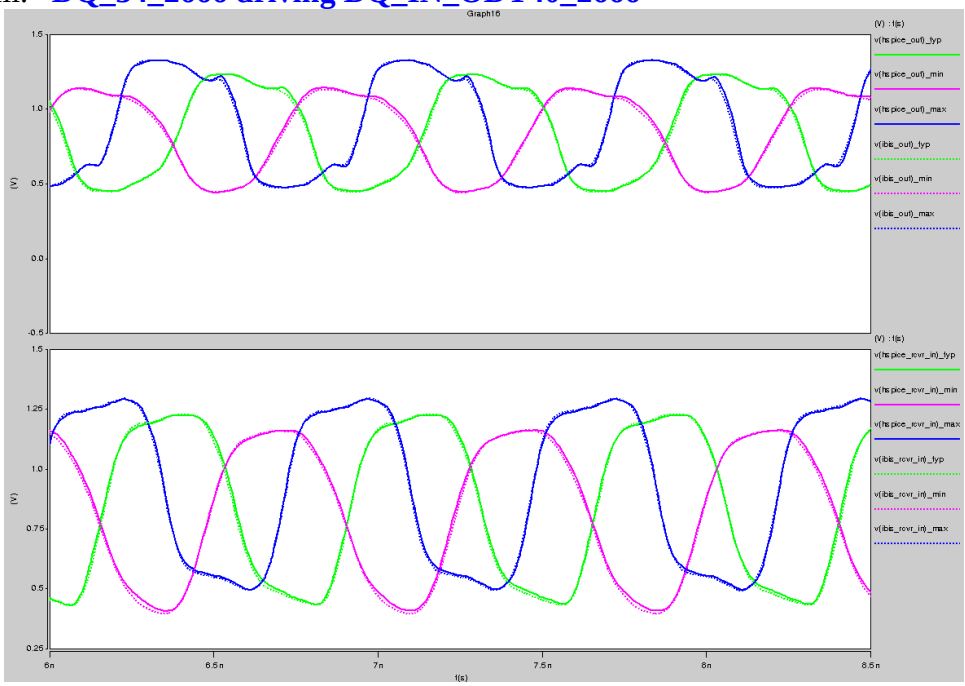
ii. **DQ_34_2666 driving DQ_IN_ODT34_2666**



iii. **DQ_34_2666 driving DQ_IN_ODT40_2666**



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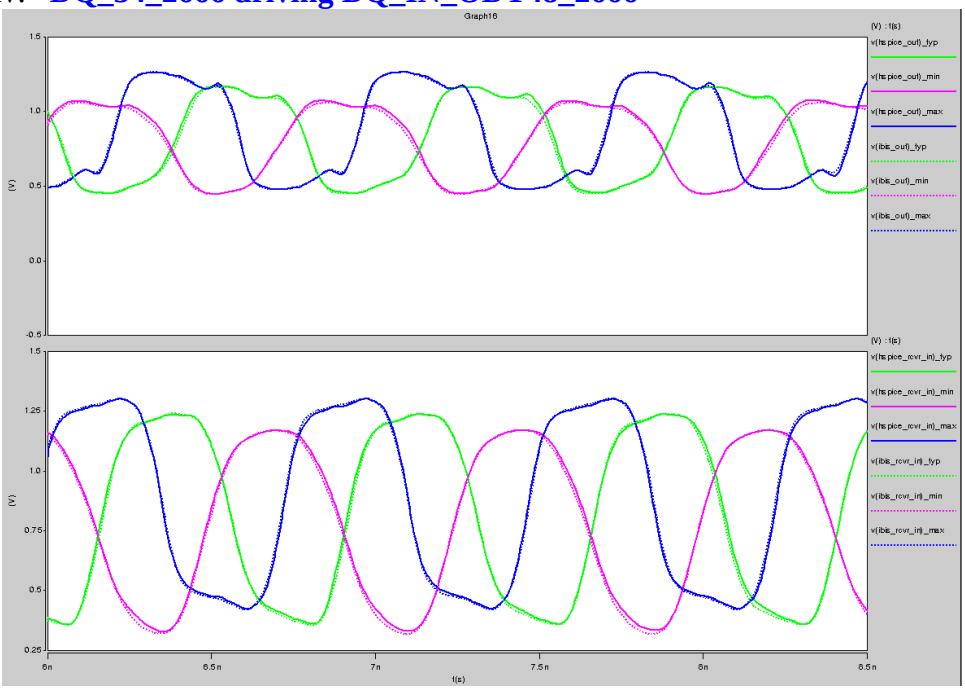
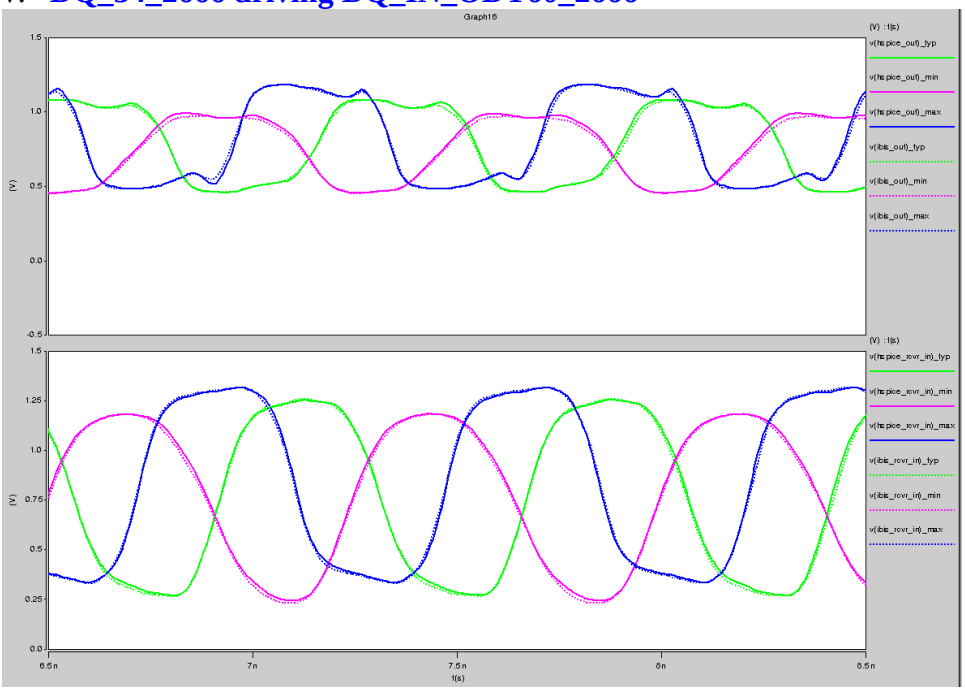
iv. **DQ_34_2666 driving DQ_IN_ODT48_2666**



v. **DQ_34_2666 driving DQ_IN_ODT60_2666**



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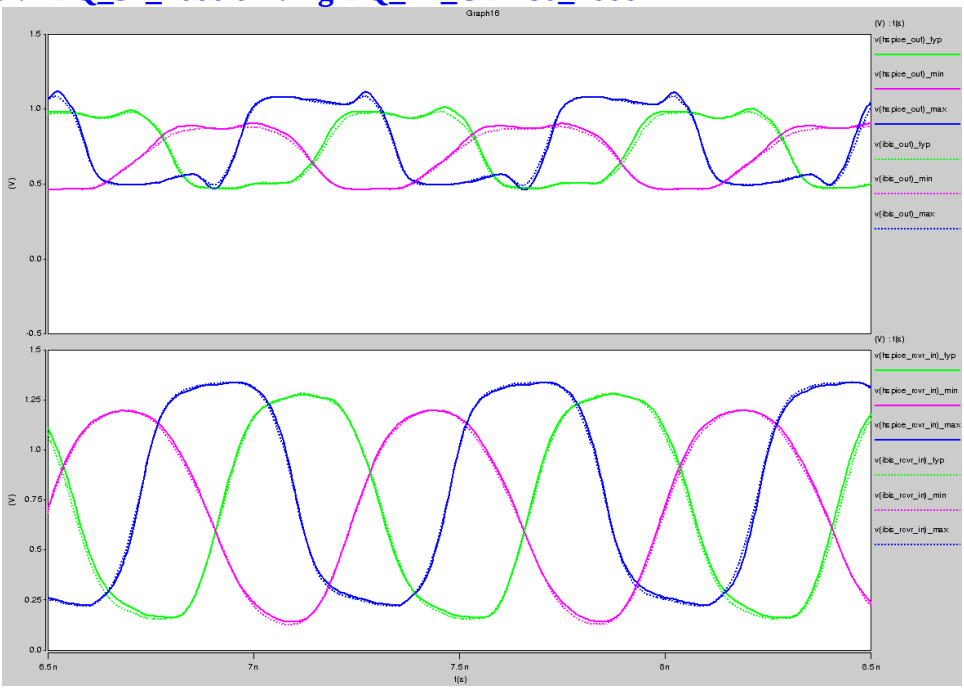
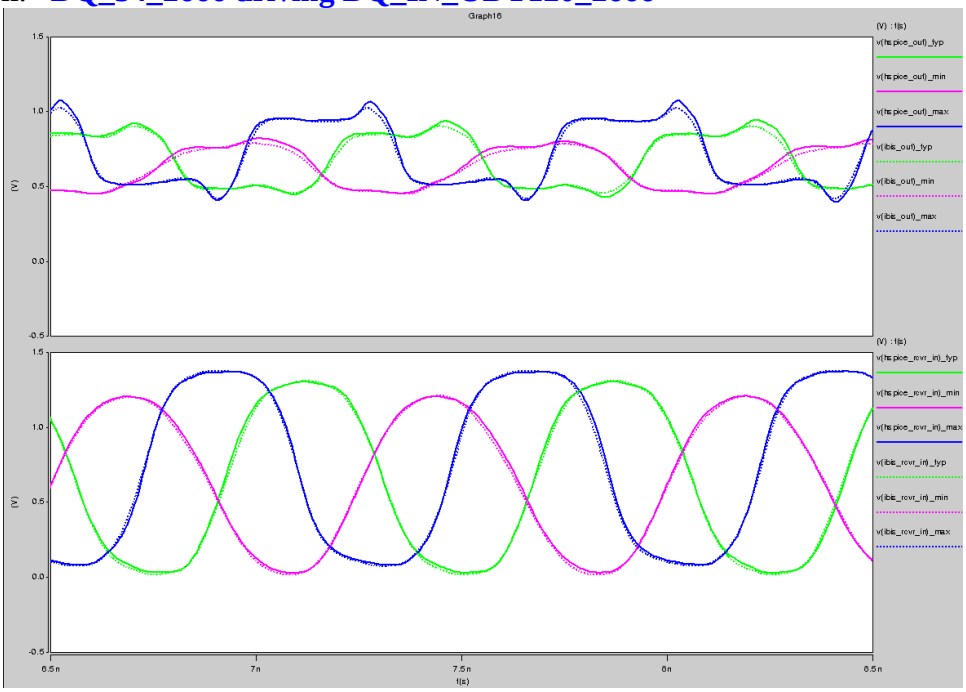
vi. **DQ_34_2666 driving DQ_IN_ODT80_2666**



vii. **DQ_34_2666 driving DQ_IN_ODT120_2666**



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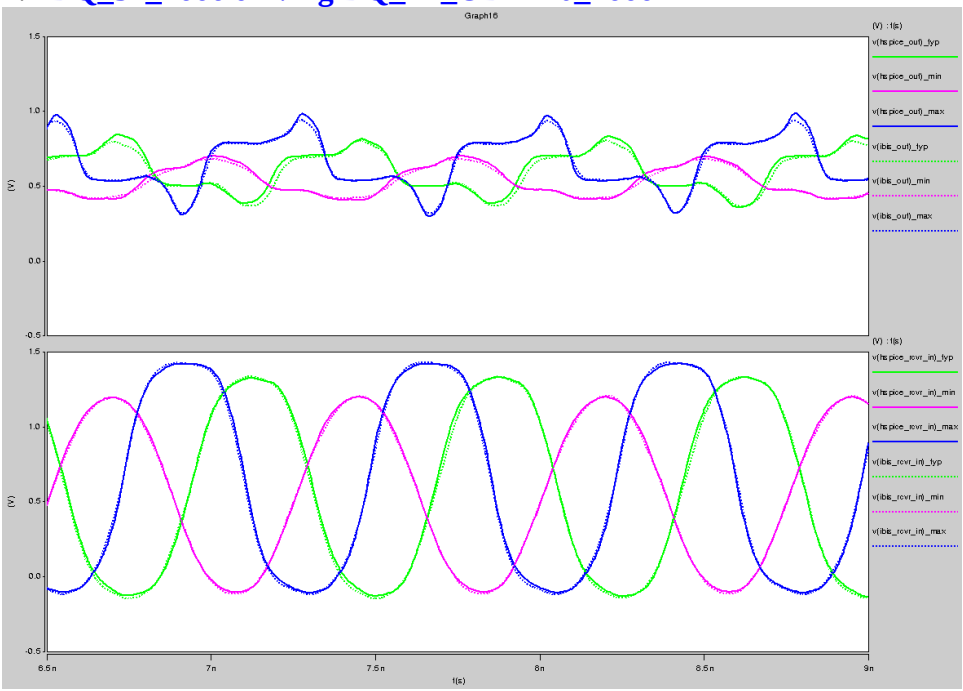
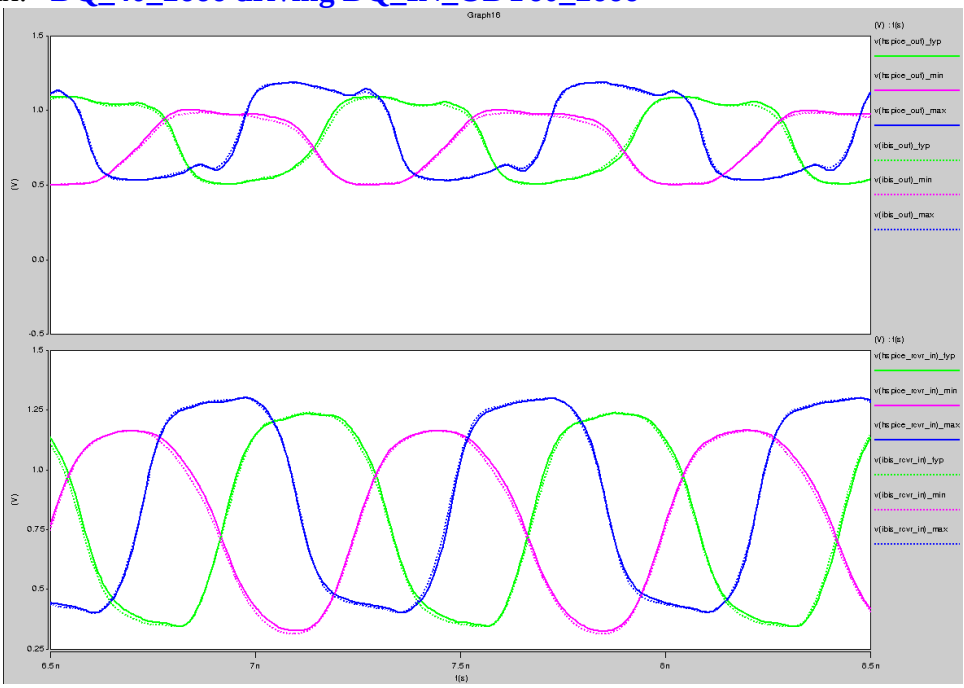
viii. **DQ_34_2666 driving DQ_IN_ODT240_2666**



ix. **DQ_40_2666 driving DQ_IN_ODT60_2666**



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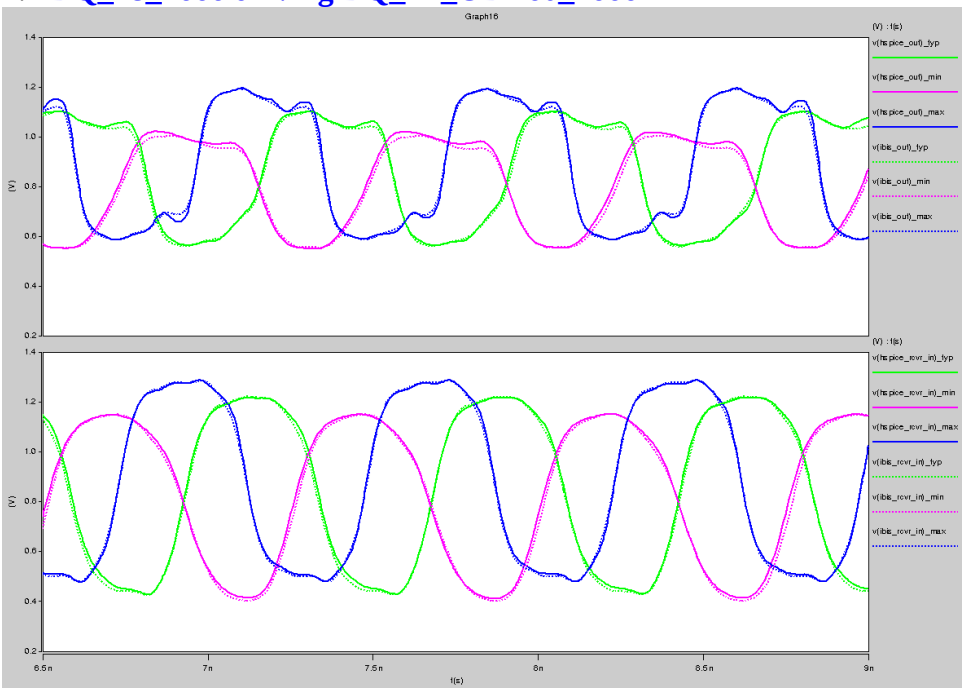
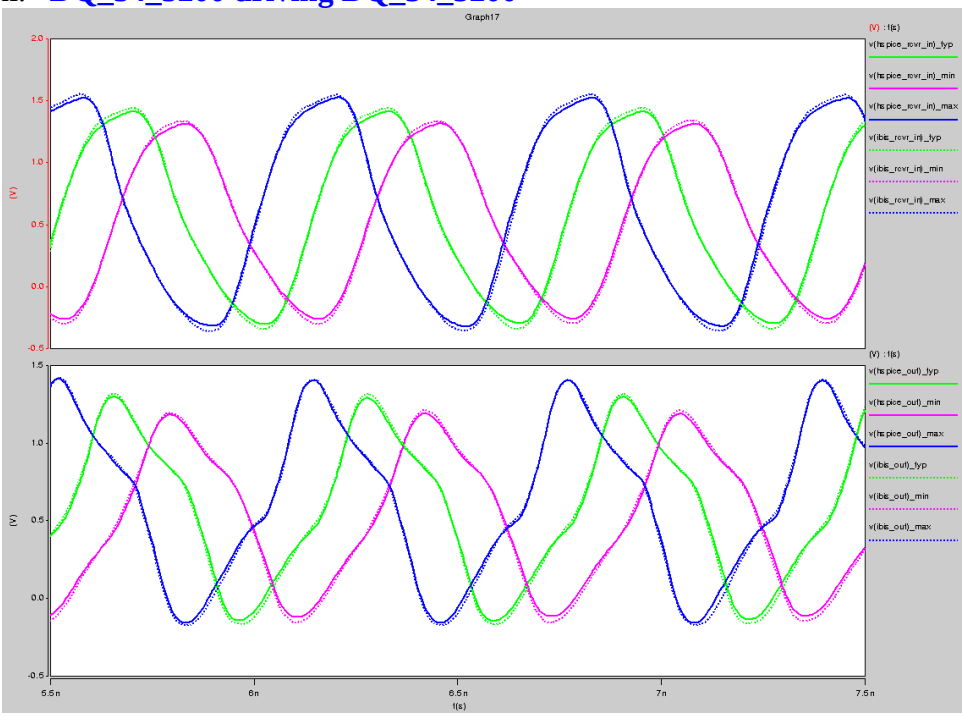
x. **DQ_48_2666 driving DQ_IN_ODT60_2666**



xi. **DQ_34_3200 driving DQ_34_3200**



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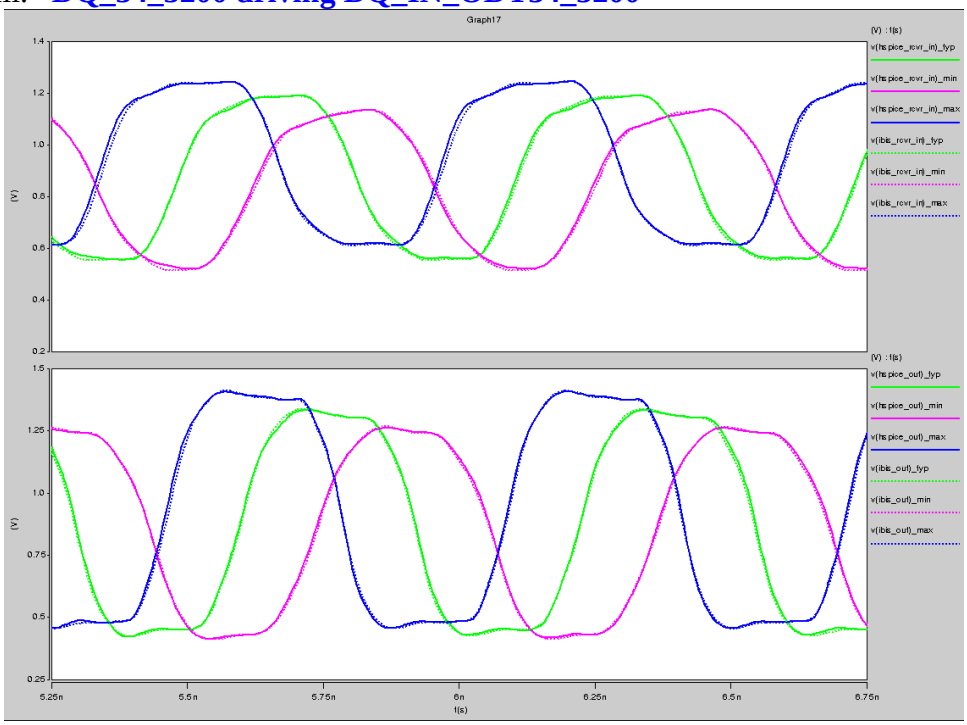
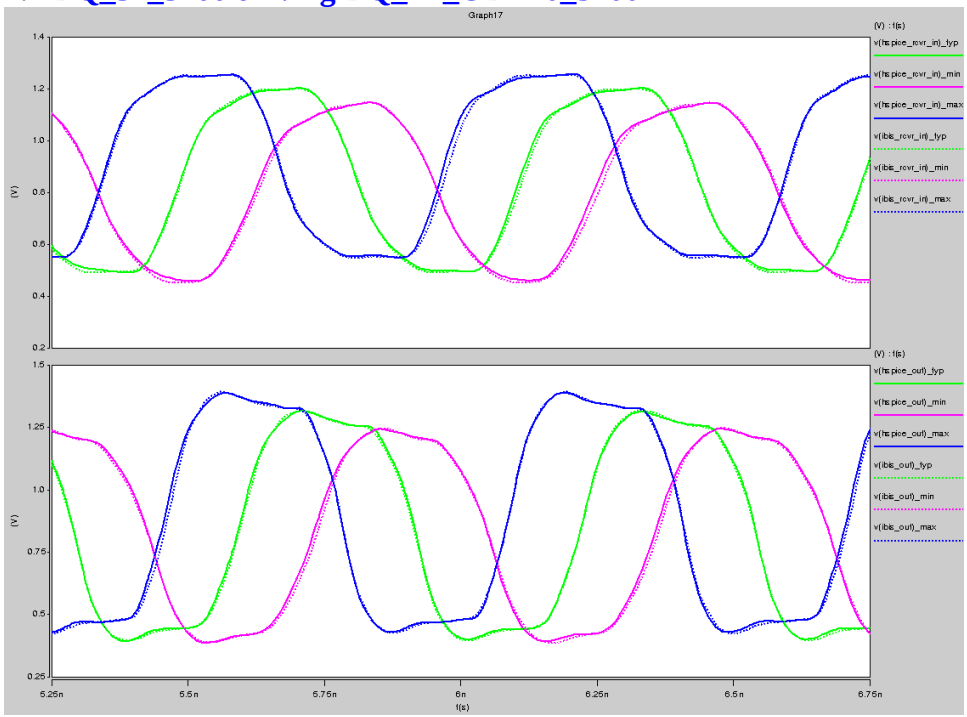
xii. **DQ_34_3200 driving DQ_IN_ODT34_3200**



xiii. **DQ_34_3200 driving DQ_IN_ODT40_3200**



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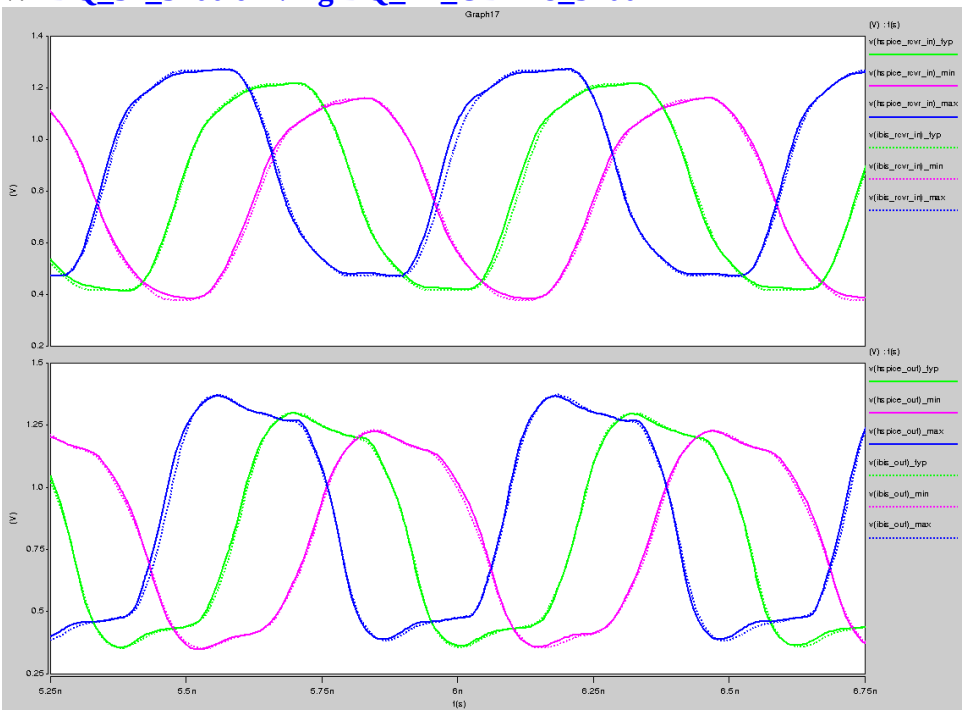
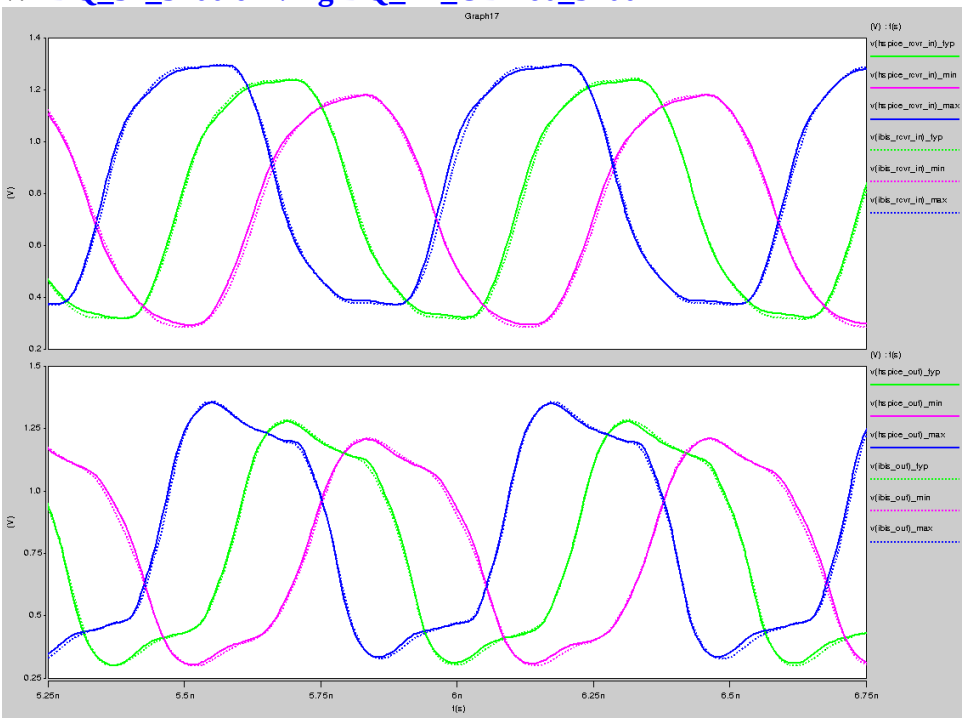
xiv. **DQ_34_3200 driving DQ_IN_ODT48_3200**



xv. **DQ_34_3200 driving DQ_IN_ODT60_3200**



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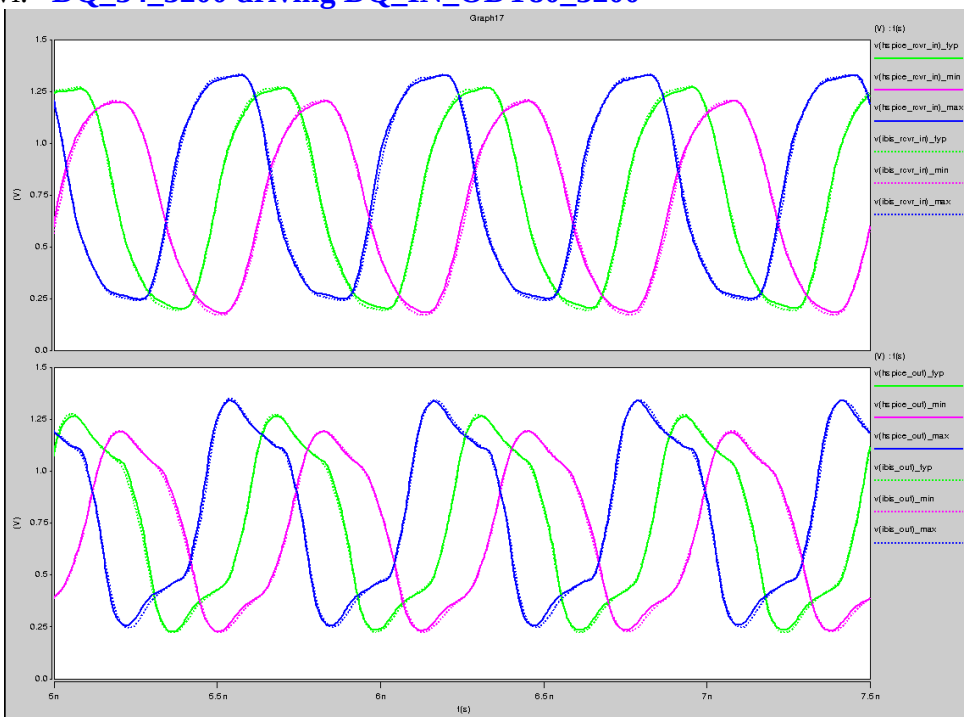
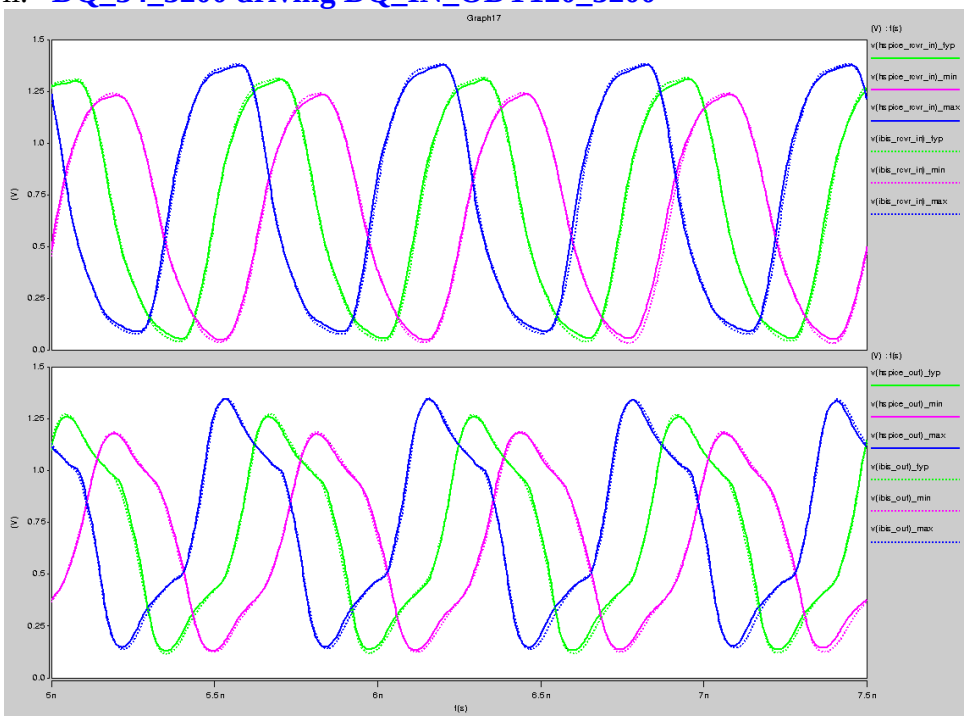
xvi. **DQ_34_3200 driving DQ_IN_ODT80_3200**



xvii. **DQ_34_3200 driving DQ_IN_ODT120_3200**



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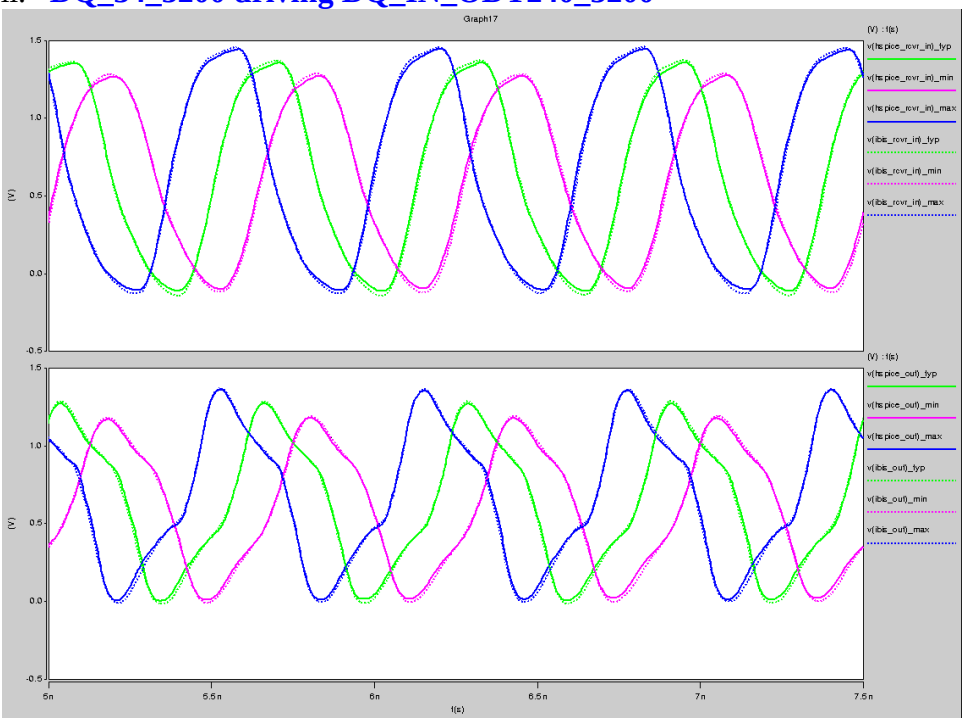
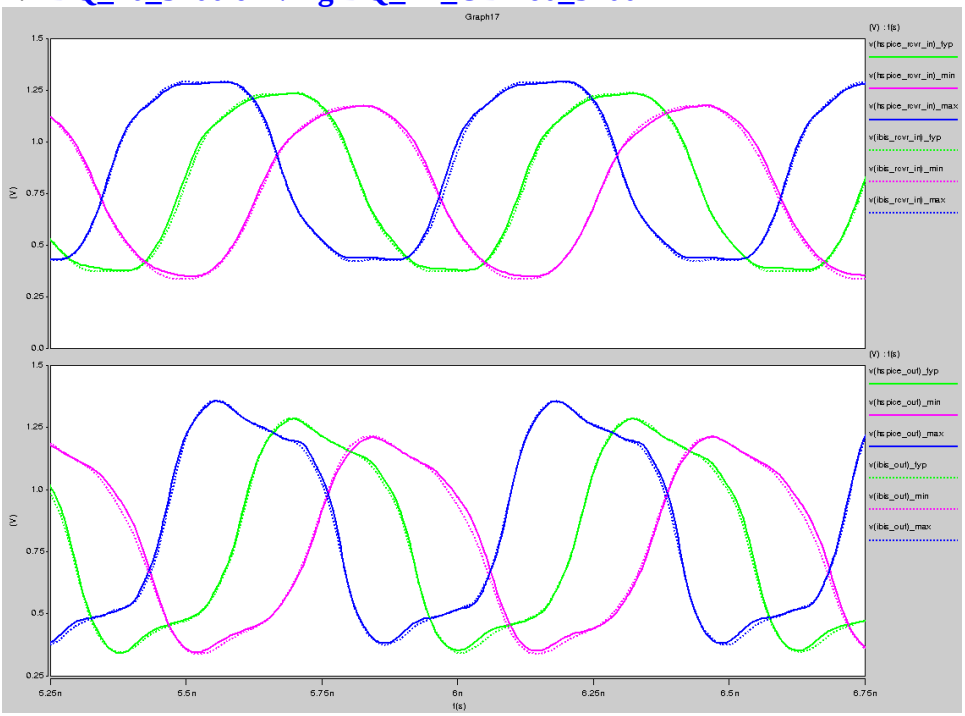
xviii. **DQ_34_3200 driving DQ_IN_ODT240_3200**



xix. **DQ_40_3200 driving DQ_IN_ODT60_3200**



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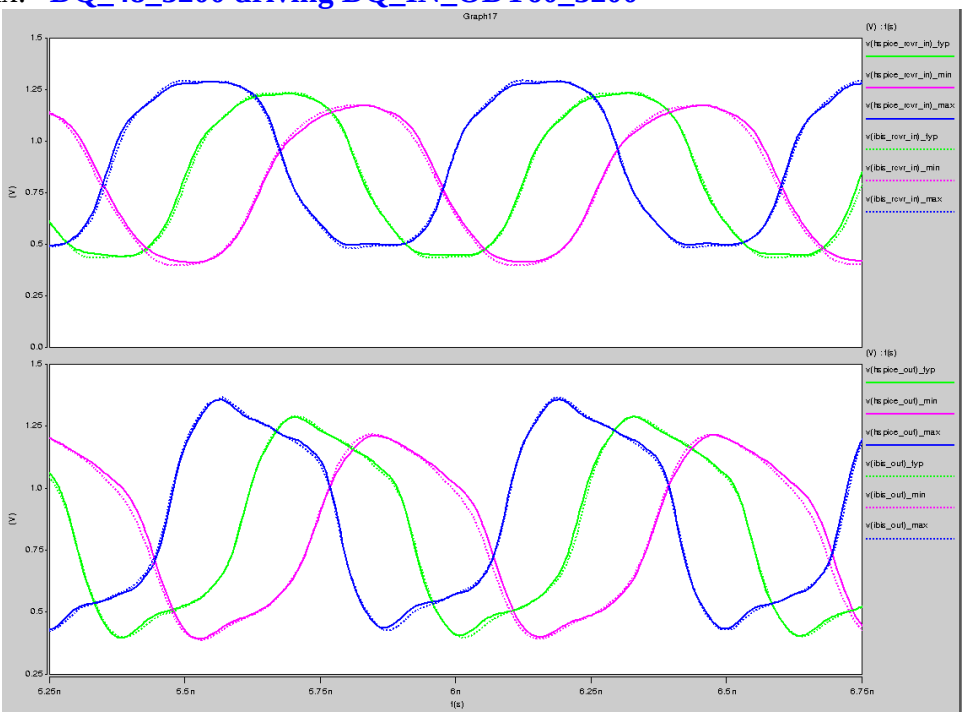
xx. **DQ_48_3200 driving DQ_IN_ODT60_3200**



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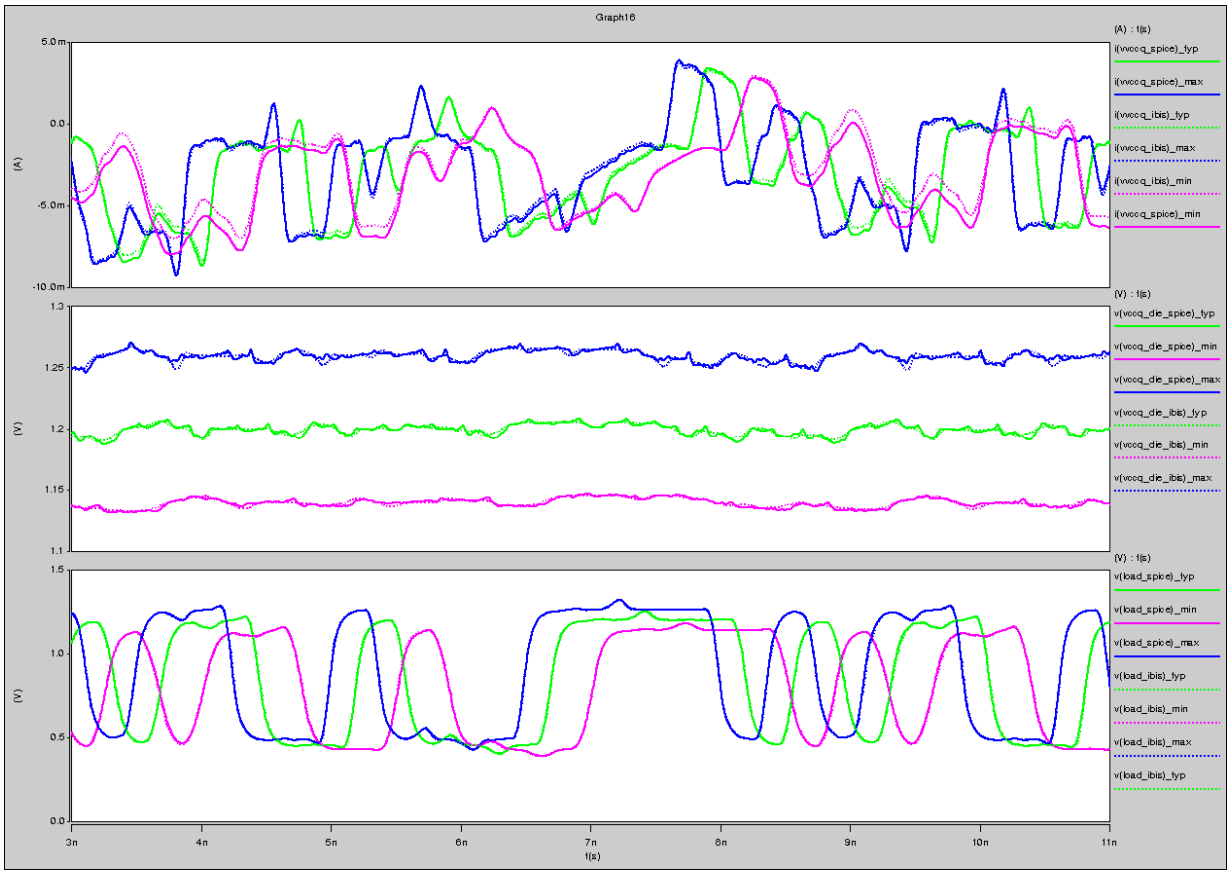
2. ☒ For all Output or I/O IBIS Version 5.0 power-aware models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element) with a non-ideal power supply connection.
   a. ☒ Use the setup and node naming conventions shown in Setup B below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations: **2014.09**
   b. ☒ Run simulations for all corner cases and at fastest speed grades.

      i. **DQ_34_2666**



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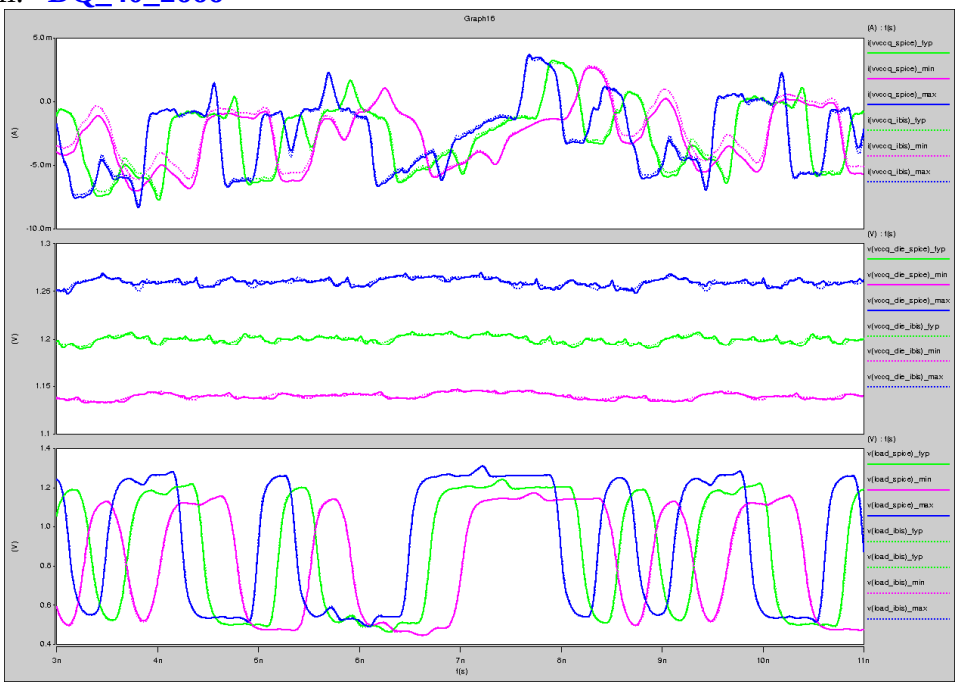
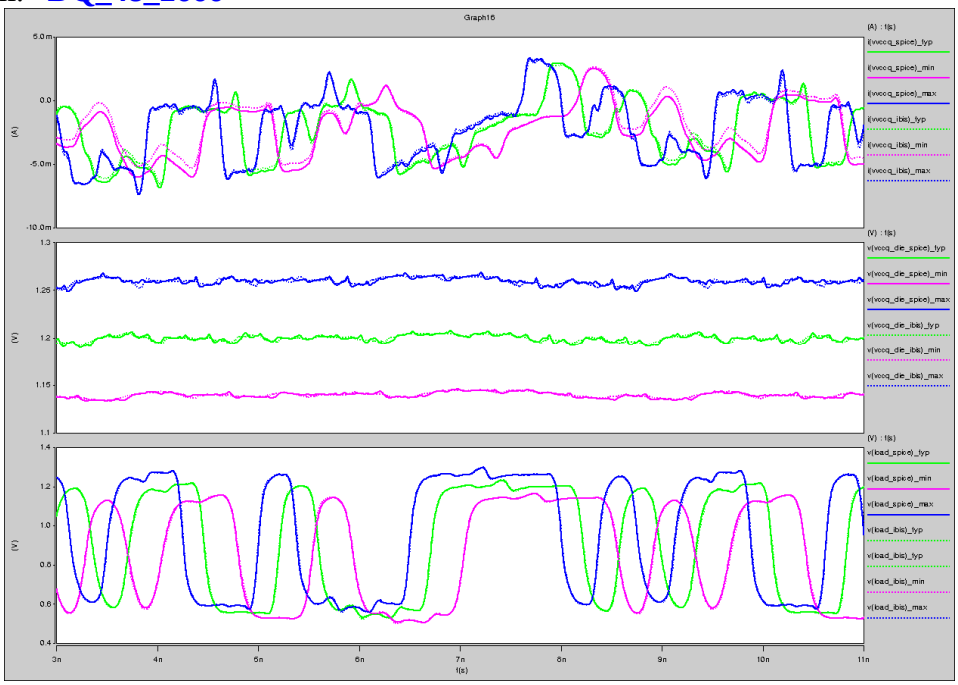
ii. **DQ_40_2666**



iii. **DQ_48_2666**



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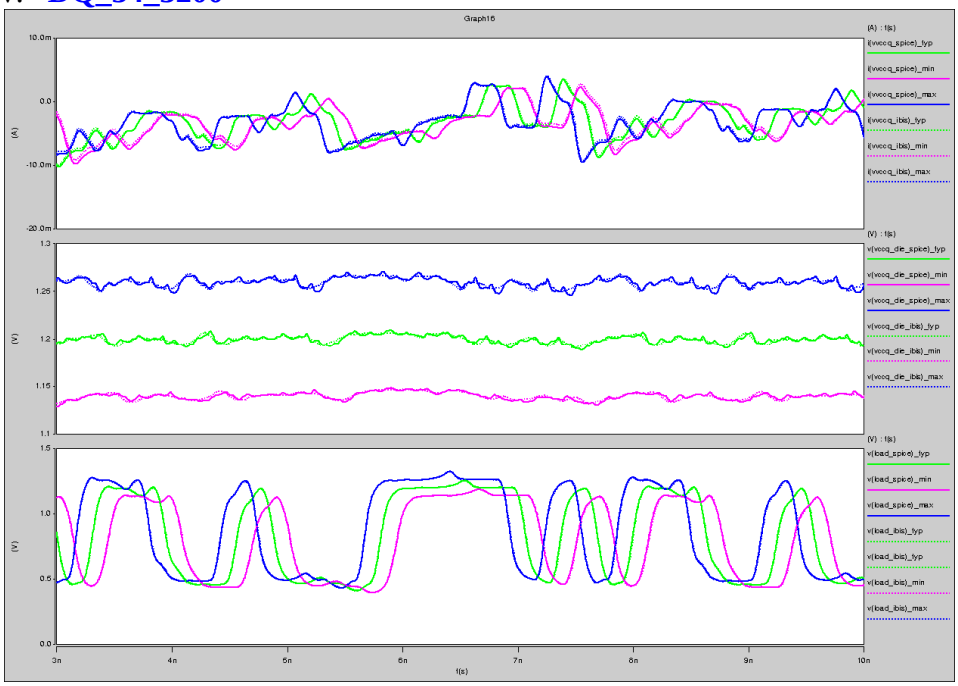
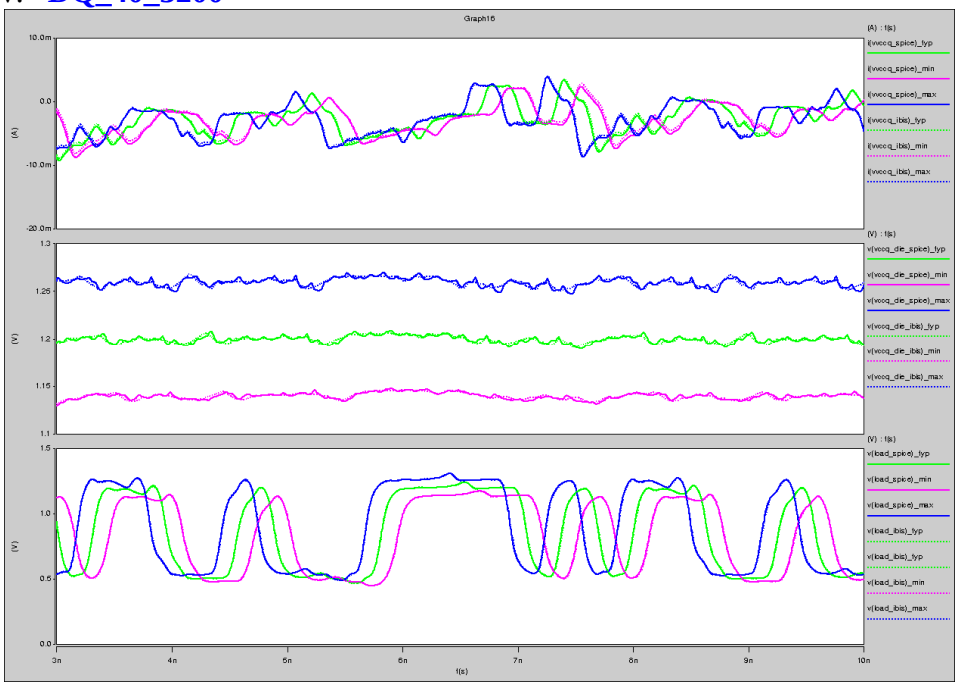
iv. **DQ_34_3200**



v. **DQ_40_3200**



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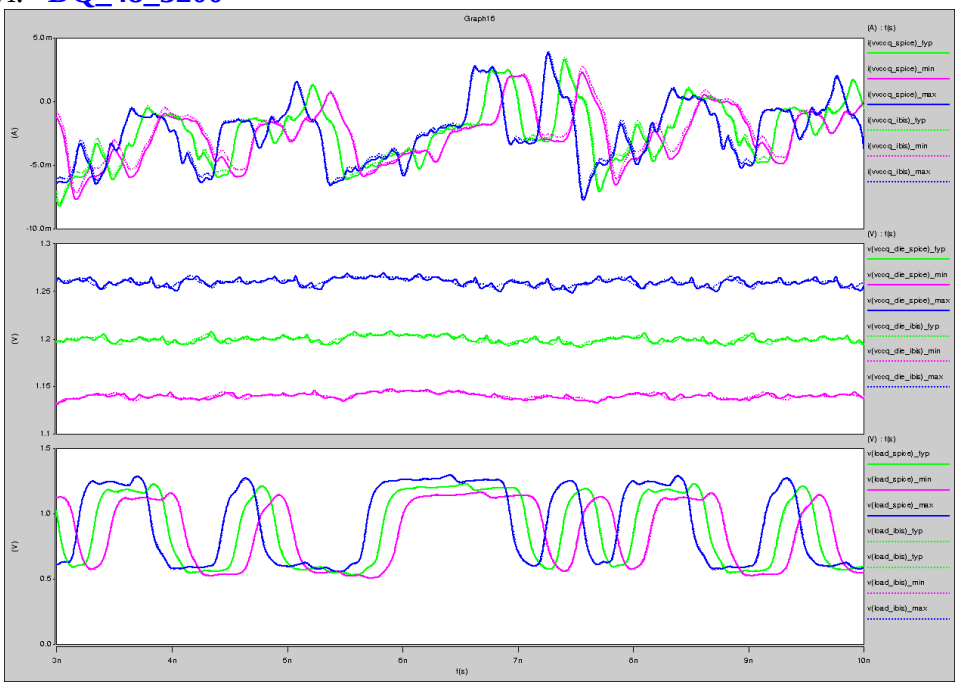
vi. **DQ_48_3200**



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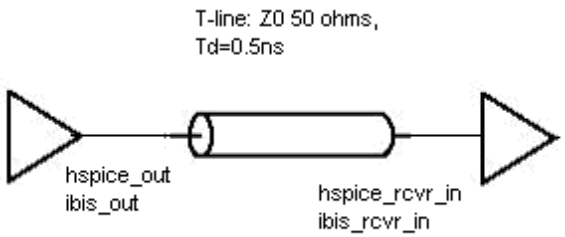
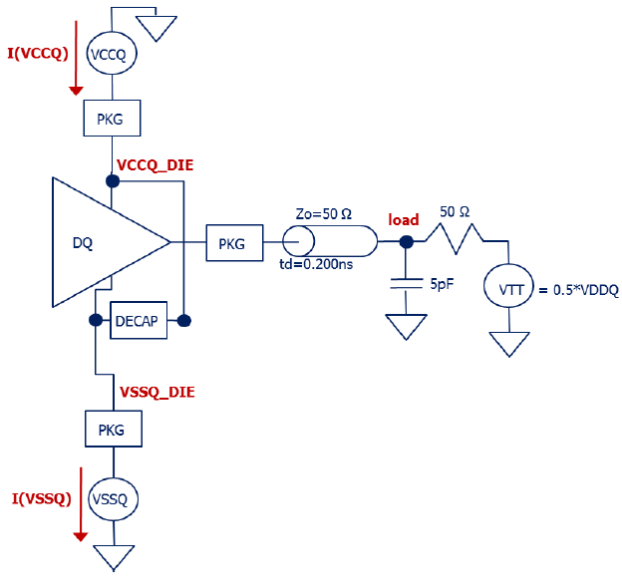
Setup

A:



B:




```
* Package Model used for correlation
lpkg PAD BALL 1.25e-9 R=0.25
lpkg_vccq vccq_die vccq_ball 1.25e-9 R=0.25
lpkg_vcc vcc_die vcc_ball 0.25e-9 R=0.25
rpkg_vcc vcc_die vcc_ball 0.01
lpkg_vss vss_die vss_ball 0.10e-9 R=0.05
k1 lpkg_vccq lpkg_vss 0.20
k2 lpkg_vcc lpkg_vss 0.10
k3 lpkg lpkg_vccq 0.40
k4 lpkg lpkg_vss 0.20
cpkg_vccq BALL vccq_ball 0.20e-12
cpkg_vss BALL vss_ball 0.20e-12
cpkg_vccq_vss vccq_ball vss_ball 0.400e-12
cpkg_vcc_vss vcc_ball vss_ball 0.400e-12
```

Comments:

1. IBIS model may not reflect current speed grade availability.
2. C_comp is compared with the DDR4-1600 specification only.
3. Slew rate is based on HSPICE simulation with a 50ohm load to VDDQ. This includes simple package parasitics for pin and power/gnd nets.

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Document Revision History

Rev **1.0** - Date **4/8/2016**

a. IBIS revision (Version 4.2) **1.0**
b. IBIS revision (Version 5.0) **1.0**
c. HSpice revision **1.0**

Rev **1.1** - Date **10/18/2016**

a. IBIS revision (Version 4.2) **1.1**
b. IBIS revision (Version 5.0) **1.1**
c. HSpice revision **1.1**

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