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## **IBIS/HSPICE Model Quality Report**

Design ID: **V90B**

Description: **4Gb DDR3L SDRAM**

Marketing device name(s): **MT41K1G4RG, MT41K512M8RG, MT41K256M16LY, MT41K1G4V90B, MT41K512M8V90B, MT41K256M16V90B**

Valid speed grades: **DDR3L-1066, DDR3L-1333, DDR3L-1600, DDR3L-1866, DDR3L-2133<sup>1</sup>**

Zip filename: **v90b\_1p35\_ibis.zip**

IBIS filename: **v90b\_1p35.ibs** File rev: **2.0**

HSpice filename: **v90b\_1p35\_hspice.zip** File rev: **2.0**

EBD filename (if applicable): File rev:

Die rev: **N**

Date: **August 15, 2014**

Datasheet link: **Not Available**

E-mail [modelsupport@micron.com](mailto:modelsupport@micron.com) for questions regarding Quality Report.

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### **Device Parameters**

VDDQ – Slow: **1.283V** Typical: **1.350V** Fast: **1.425V**

VDD – Slow: **1.283V** Typical: **1.350V** Fast: **1.425V**

Junction Temperature (Commercial) - Slow: **90C** Typical: **45C** Fast: **0C**

VDDQ/VSSQ Decoupling Capacitance: **5.80nF**

Included in HSPICE DQ/DQS models? **Yes** Amount per DQ/DQS model: **264pF/526.6pF**

VDDQ/VSSQ Decoupling Capacitance Series Resistance: **~0.1ohms**

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### **IBIS Quality Summary**

1. ☒ Include the IBIS Quality Specification 2.0 Overall IBIS Quality level. For details on IBIS Quality, reference the quality specification and quality checklist on IBIS quality webpage [http://www.eda.org/pub/ibis/quality\\_wip/](http://www.eda.org/pub/ibis/quality_wip/).

Overall IBIS Quality Level: **IQ3MS**

Exceptions: **N/A**

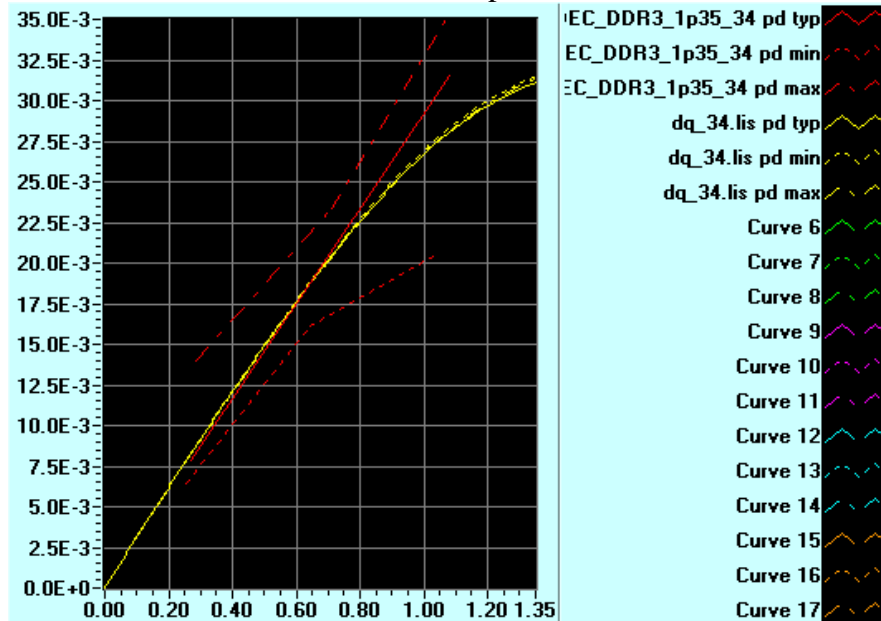
2. ☒ Include the filename of the IBIS Quality Checklist that accompanies this report.

Filename: **v90b\_1p35\_ibis\_quality\_checklist.xls**

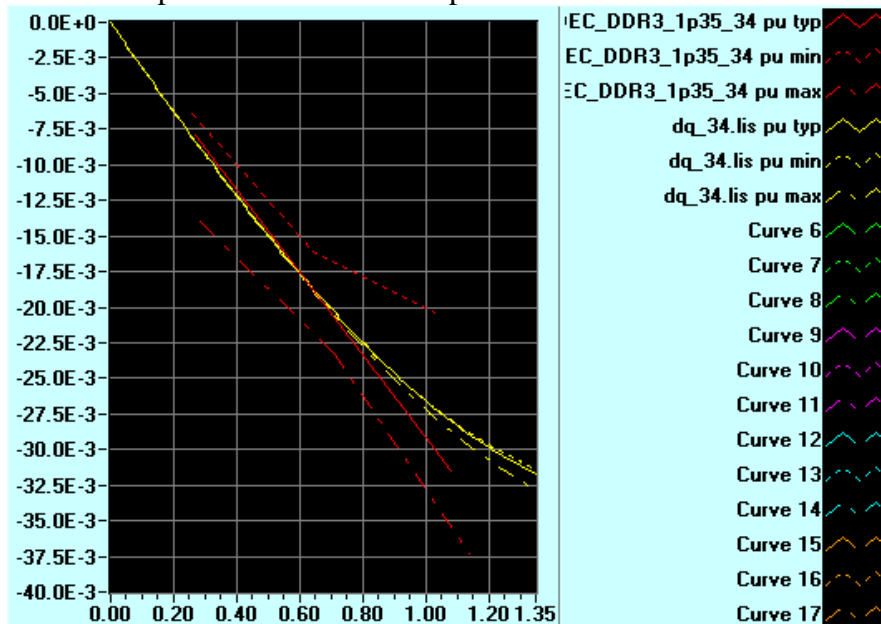
## IBIS MODEL Correlation

### Datasheet Correlation

1. ☒ For Output or I/O model compare datasheet IOH/IOL data with IBIS pullup/pulldown data.
  - a. Model name: **DQ\_34**<sup>2</sup>
    - i. Pulldown I-V versus **JEDEC** specification

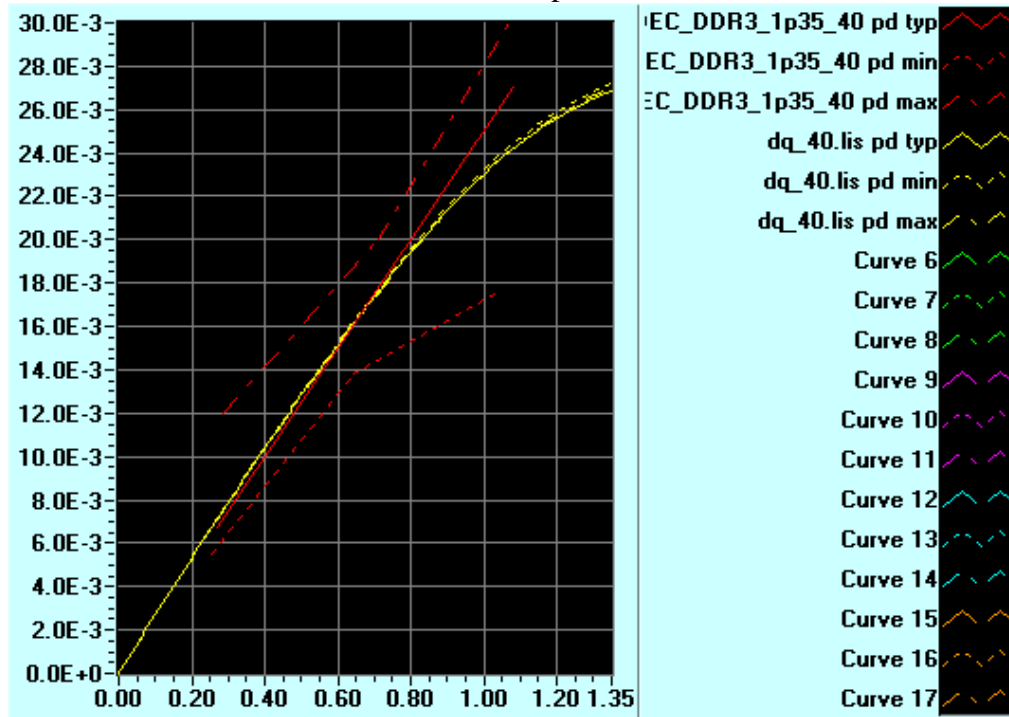


- ii. Pullup I-V versus **JEDEC** specification

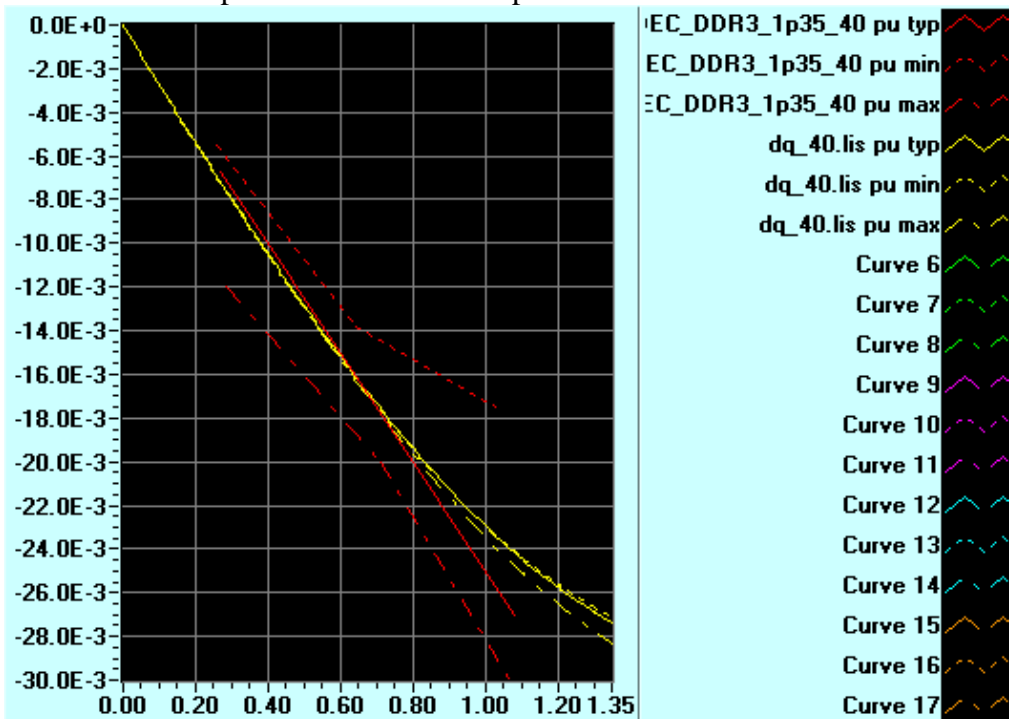


b. Model name: **DQ\_40<sup>2</sup>**

i. Pulldown I-V versus **JEDEC** specification



ii. Pullup I-V versus **JEDEC** specification



2. ☒ Compare C\_comp with datasheet Input C. Provide C\_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16).

Component name: **MT41K512M4RG, MT41K256M8RG (78b, x4/x8)**

		IBIS		Datasheet	
		min	max	min	max
<b>DQ</b>	C_comp	0.90	1.00	NA	NA
	C package	0.47	0.51	NA	NA
	C_total	1.37	1.51	1.50	2.30
<b>DQS</b>	C_comp	1.00	1.10	NA	NA
	C package	0.47	0.48	NA	NA
	C_total	1.47	1.58	1.50	2.30
<b>INPUT</b>	C_comp	0.50	0.60	NA	NA
	C package	0.32	0.40	NA	NA
	C_total	0.82	1.00	0.75	1.30
<b>CLK</b>	C_comp	0.61	0.69	NA	NA
	C package	0.32	0.33	NA	NA
	C_total	0.93	1.02	0.80	1.40

Component name: **MT41K128M16LY (96b, x16)**

		IBIS		Datasheet	
		min	max	min	max
<b>DQ</b>	C_comp	0.90	1.00	NA	NA
	C package	0.47	0.53	NA	NA
	C_total	1.37	1.53	1.50	2.30
<b>DQS</b>	C_comp	1.00	1.10	NA	NA
	C package	0.47	0.49	NA	NA
	C_total	1.47	1.59	1.50	2.30
<b>INPUT</b>	C_comp	0.50	0.60	NA	NA
	C package	0.37	0.46	NA	NA
	C_total	0.87	1.06	0.75	1.30
<b>CLK</b>	C_comp	0.61	0.69	NA	NA
	C package	0.32	0.35	NA	NA
	C_total	0.93	1.04	0.80	1.40

3. ☒ If slew rate specifications (rise/fall slew) are available from the datasheet, complete Spice simulations to generate slew rate data and provide a comparison table.

Model	Slew Rate (V/ns)	IBIS			Datasheet	
		min	typ	max	min	max
DQ_34	Rising	3.26	3.72	4.66	2.50	6.00
	Falling	3.53	3.84	4.66	2.50	6.00
DQ_40	Rising	2.79	3.34	4.31	2.50	6.00
	Falling	3.10	3.60	4.48	2.50	6.00
DQS_34	Rising	3.20	3.68	4.61	2.50	6.00
	Falling	3.45	3.79	4.61	2.50	6.00
DQS_40	Rising	2.76	3.31	4.25	2.50	6.00
	Falling	3.03	3.52	4.40	2.50	6.00

4. ☒ Compare ODT data with datasheet.

ODT calculated using the formula  $RTT = (V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IH(ac)}) - I(V_{IL(ac)}))$

ODT20	TYP	MIN	MAX
Vil (V)	0.515	0.4815	0.5525
Vih (V)	0.835	0.8015	0.8725
Ivil (A)	-6.79E-03	-6.94E-03	-7.05E-03
Ivih (A)	6.87E-03	7.05E-03	6.53E-03
	TYP	MAX	MIN
Rtt (Model)	23.42	22.87	23.56
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	20	32	18

ODT30	TYP	MIN	MAX
Vil (V)	0.515	0.4815	0.5525
Vih (V)	0.835	0.8015	0.8725
Ivil (A)	-4.62E-03	-4.73E-03	-4.78E-03
Ivih (A)	4.64E-03	4.76E-03	4.41E-03
	TYP	MAX	MIN
Rtt (Model)	34.57	33.72	34.82
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	30	48	27

ODT40	TYP	MIN	MAX
Vil (V)	0.515	0.4815	0.5525
Vih (V)	0.835	0.8015	0.8725
Ivil (A)	-3.50E-03	-3.59E-03	-3.62E-03
Ivih (A)	3.50E-03	3.59E-03	3.33E-03
	TYP	MAX	MIN
Rtt (Model)	45.72	44.57	46.07
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	40	64	36

ODT60	TYP	MIN	MAX
Vil (V)	0.515	0.4815	0.5525
Vih (V)	0.835	0.8015	0.8725
Ivil (A)	-2.36E-03	-2.42E-03	-2.44E-03
Ivih (A)	2.35E-03	2.41E-03	2.23E-03
	TYP	MAX	MIN
Rtt (Model)	68.03	66.28	68.58
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	60	96	54

ODT120	TYP	MIN	MAX
Vil (V)	0.515	0.4815	0.5525
Vih (V)	0.835	0.8015	0.8725
Ivil (A)	-1.19E-03	-1.22E-03	-1.23E-03
Ivih (A)	1.18E-03	1.21E-03	1.12E-03
	TYP	MAX	MIN
Rtt (Model)	134.94	131.40	136.12
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	120	192	108

## Measurement Correlation

- ☐ For Output or I/O models compare measured IOH/IOL data with IBIS pullup/pulldown data. If the measurement conditions are different than the IBIS conditions, run Spice simulations using the same measurement conditions such as VCC, temperature, and process. Include measurement conditions in the image labels.

Not Available

2. ☒ Compare C\_comp with measured C\_comp. Provide C\_comp comparison table for all models and for all package combinations (i.e x4, x8 and x16).

Component name: **MT41K512M4RG, MT41K256M8RG (78b, x4/x8)**

		IBIS			Measured		
		min	typ	max	min	typ	max
<b>DQ</b>	C_comp	0.90	0.95	1.00	NA	NA	NA
	C package	0.47	0.48	0.51	NA	NA	NA
	C_total	1.37	1.43	1.51	1.36	1.41	1.51
<b>DQS</b>	C_comp	1.00	1.05	1.10	NA	NA	NA
	C package	0.47	0.47	0.48	NA	NA	NA
	C_total	1.47	1.52	1.58	1.47	1.50	1.53
<b>INPUT</b>	C_comp	0.50	0.55	0.60	NA	NA	NA
	C package	0.32	0.35	0.40	NA	NA	NA
	C_total	0.82	0.90	1.00	0.83	0.97	1.22
<b>CLK</b>	C_comp	0.61	0.65	0.69	NA	NA	NA
	C package	0.32	0.33	0.33	NA	NA	NA
	C_total	0.93	0.98	1.02	0.95	0.97	0.99

Component name: **MT41K128M16LY (96b, x16)**

		IBIS			Measured		
		min	typ	max	min	typ	max
<b>DQ</b>	C_comp	0.90	0.95	1.00	NA	NA	NA
	C package	0.47	0.50	0.53	NA	NA	NA
	C_total	1.37	1.45	1.53	1.38	1.45	1.53
<b>DQS</b>	C_comp	1.00	1.05	1.10	NA	NA	NA
	C package	0.47	0.48	0.49	NA	NA	NA
	C_total	1.47	1.53	1.59	1.49	1.53	1.57
<b>INPUT</b>	C_comp	0.50	0.55	0.60	NA	NA	NA
	C package	0.37	0.41	0.46	NA	NA	NA
	C_total	0.87	0.96	1.06	0.89	0.97	1.06
<b>CLK</b>	C_comp	0.61	0.65	0.69	NA	NA	NA
	C package	0.32	0.33	0.35	NA	NA	NA
	C_total	0.93	0.98	1.04	0.96	0.99	1.02

3. ☐ If measured clamp current data is available, provide an IBIS versus measurement comparison for all models. Include measurement conditions in the image labels.

**Not Available**

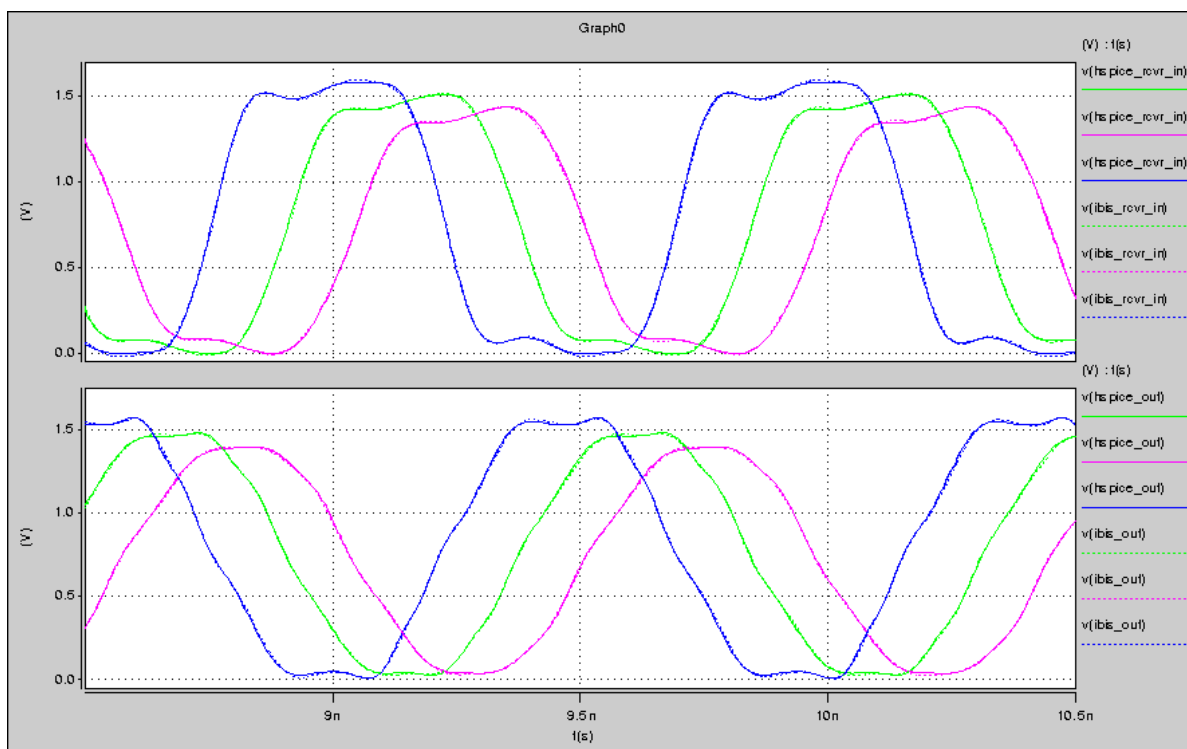
4. ☐ If slew rate data (rise/fall slew) is available from measurements, complete Spice simulations to generate slew rate data and provide a comparison table.

**Not Available**

### IBIS vs Spice Correlation

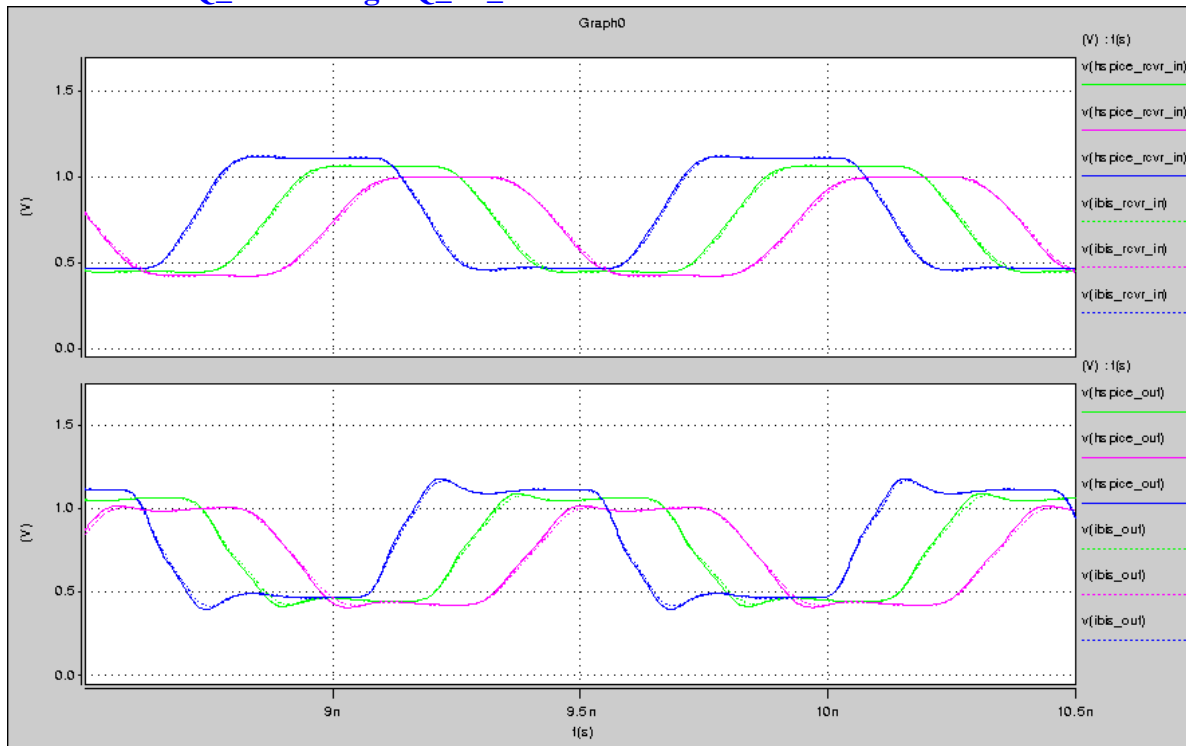
1. ☒ For all Output or I/O models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element).
  - a. ☒ Use the setup and node naming conventions shown below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations: **HSPICE 2013.12-SP1**
  - b. ☒ Run simulations for all corners cases and at fastest speed grades, testing ODT models as loads when applicable.

#### i. **DQ\_34 driving DQ\_34**

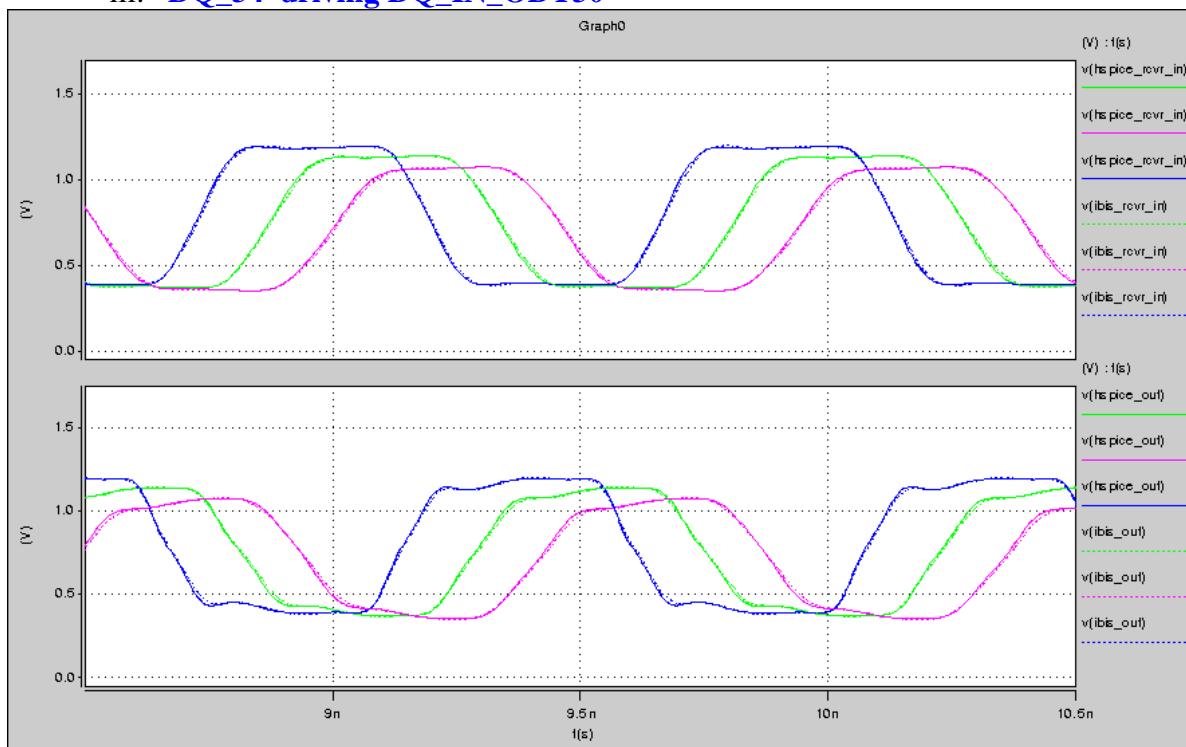




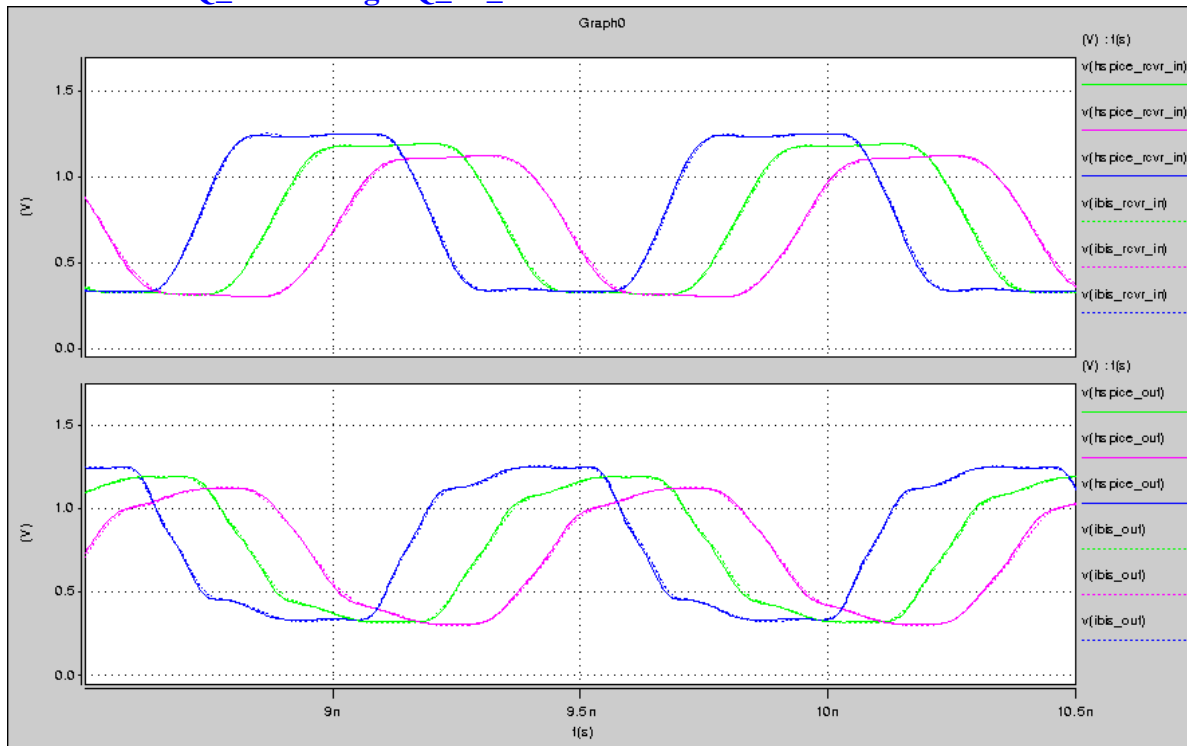
## ii. DQ\_34 driving DQ\_IN\_ODT20



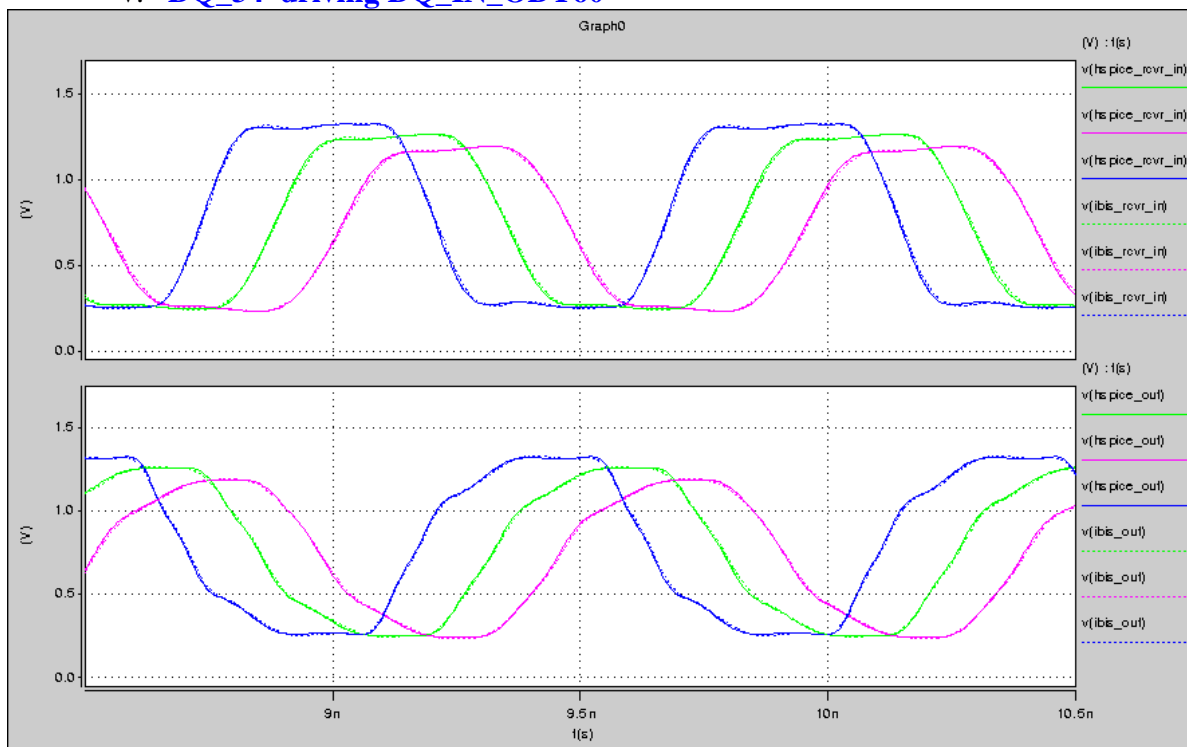
## iii. DQ\_34 driving DQ\_IN\_ODT30



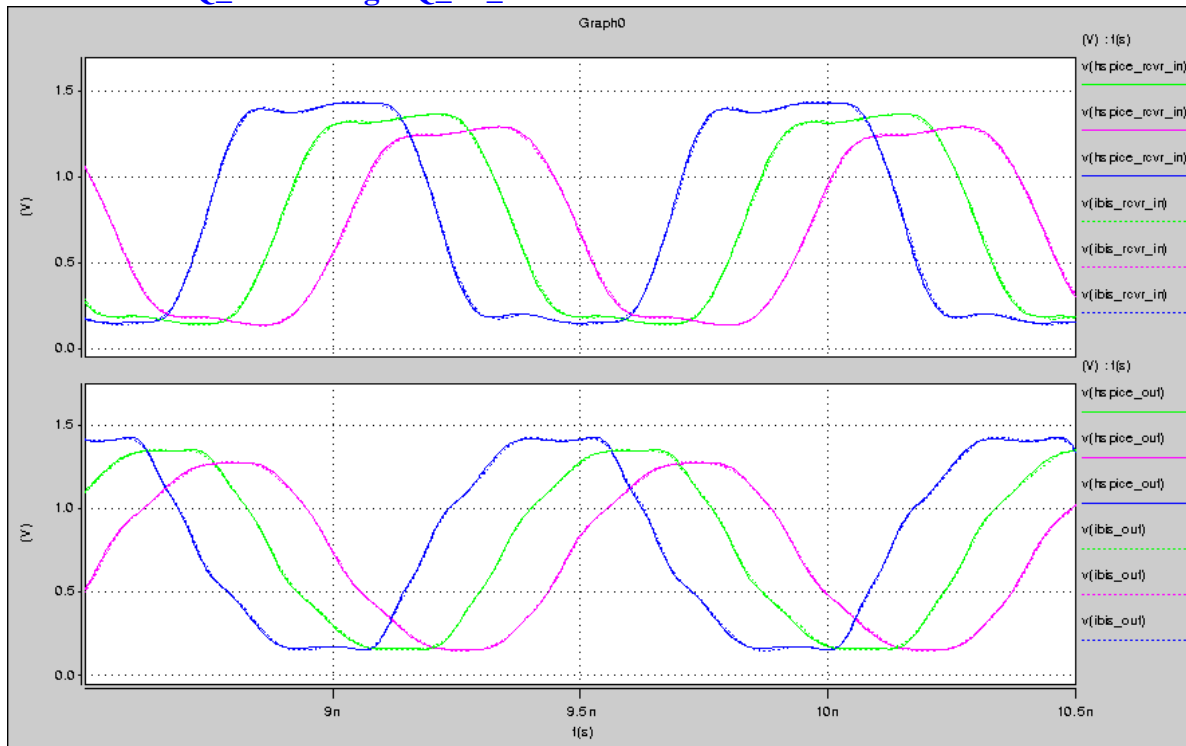
#### iv. DQ\_34 driving DQ\_IN\_ODT40



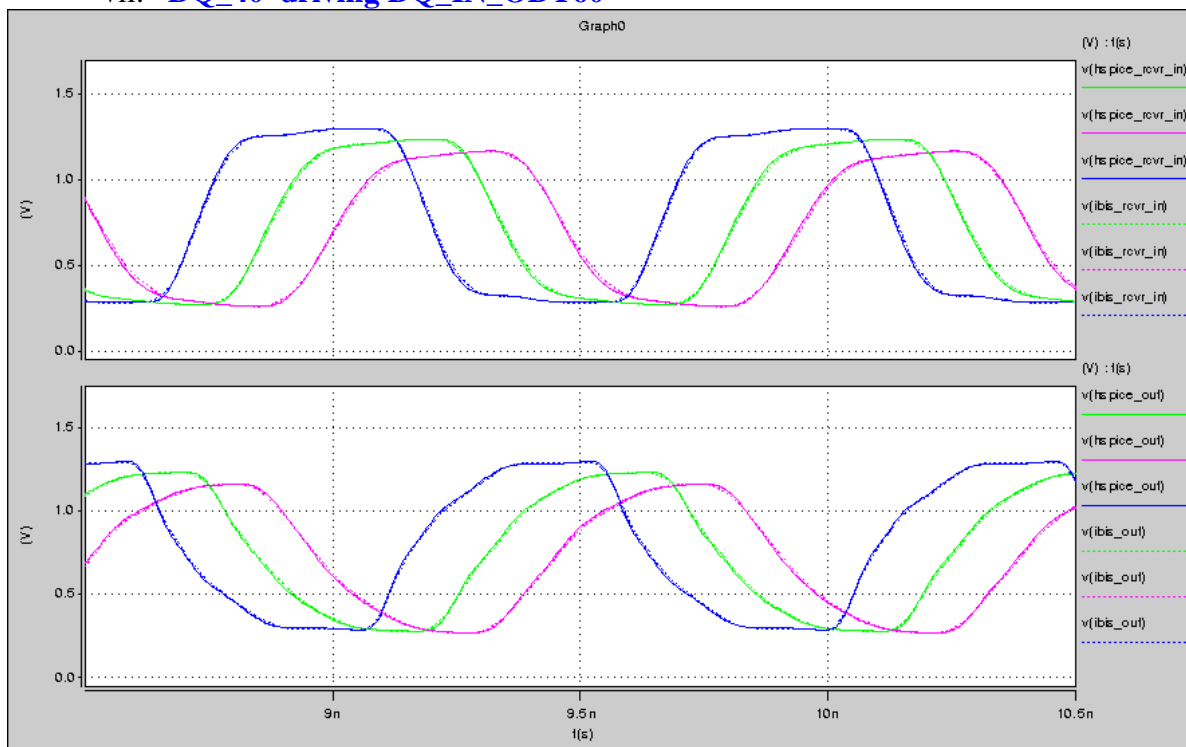
#### v. DQ\_34 driving DQ\_IN\_ODT60



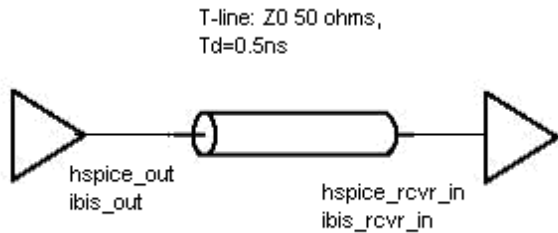
vi. DQ\_34 driving DQ\_IN\_ODT120



vii. DQ\_40 driving DQ\_IN\_ODT60



## Setup



## Comments:

1. IBIS model may not reflect speed grade availability.
2. Simulated I-V curves are the same for all speed grades.
3. C\_comp is compared with the DDR3-1600 specification only.
4. Slew rate is based on HSPICE simulation with a 25ohm load to Vtt. This includes simple package parasitics.

## Document Revision History

Rev **1.0** - Date **05/22/2013**

- a. IBIS revision **1.0**
- b. HSpice revision **1.0**

Rev **2.0** - Date **08/15/2014**

- a. IBIS revision **2.0**
- b. HSpice revision **2.0**