IBIS/HSpice Model Quality Report

Design ID: various (see the IBIS file header)
Description: eMMC with Phison PS8222 eMMC 5.0 microcontroller
Marketing device name(s): various (see the IBIS file header)
Valid speed grades: 200 MHZ DDR @1.8V / 52 MHz DDR @3.3V
Zip filename: ibis_emmc_ps8222_embedded_it.zip
IBIS filename: emmc_ps8222_embedded_it.ibs **File rev:** 1.10 and later
Die rev (controller): BB or CC
Date: from February 17, 2017
Datasheet link:
E-mail modelsupport@micron.com for questions regarding Quality Report.

Device Parameters

VDDQ – Slow: 1.7 **Typical:** 1.8 **Fast:** 1.95
VDDQ – Slow: 2.7 **Typical:** 3.3 **Fast:** 3.6
Junction Temperature (Automotive) - Slow: 100 **Typical:** 50 **Fast:** -40
VDDQ/VSSQ Decoupling Capacitance: 220 pF
Included in HSPICE DQ/DQS models? Amount per DQ/DQS model:
VDDQ/VSSQ Decoupling Capacitance Series Resistance: 2 ohm

The device contains some power decoupling capacitors mounted on the package substrate: see the Notes within the IBIS file header for additional information.
Note that at the package level the power supply to the eMMC I/O buffers (DAT, DC, CMD, CLK, RST_n) is provided through the VCCQ2 package net. Additional package power nets (VCCQ1, VDDI, etc) are used for eMMC internal core or NAND dies.

IBIS Quality Summary

1. ☒ Include the IBIS Quality Specification 2.0 Overall IBIS Quality level. For details on IBIS Quality, reference the quality specification and quality checklist on IBIS quality webpage http://www.eda.org/pub/ibis/quality_wip/.

   Overall IBIS Quality Level: 3S
   Exceptions:

2. ☒ Include the filename of the IBIS Quality Checklist that accompanies this report.

   Filename: emmc_ps8222_ibis_quality_checklist.xlsx

IBIS MODEL Correlation

Datasheet Correlation

1. ☒ Compare C_comp with datasheet Input C. Provide C_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16).

   Component name: **bare-die**

		IBIS C_comp (die only)		Datasheet	
		min	max	min	max
DQ	C_total	2.97p	3.80pF		6pF
IN	C_total	2.97p	3.80pF		6pF
CLK	C_total	2.97p	3.80pF		6pF

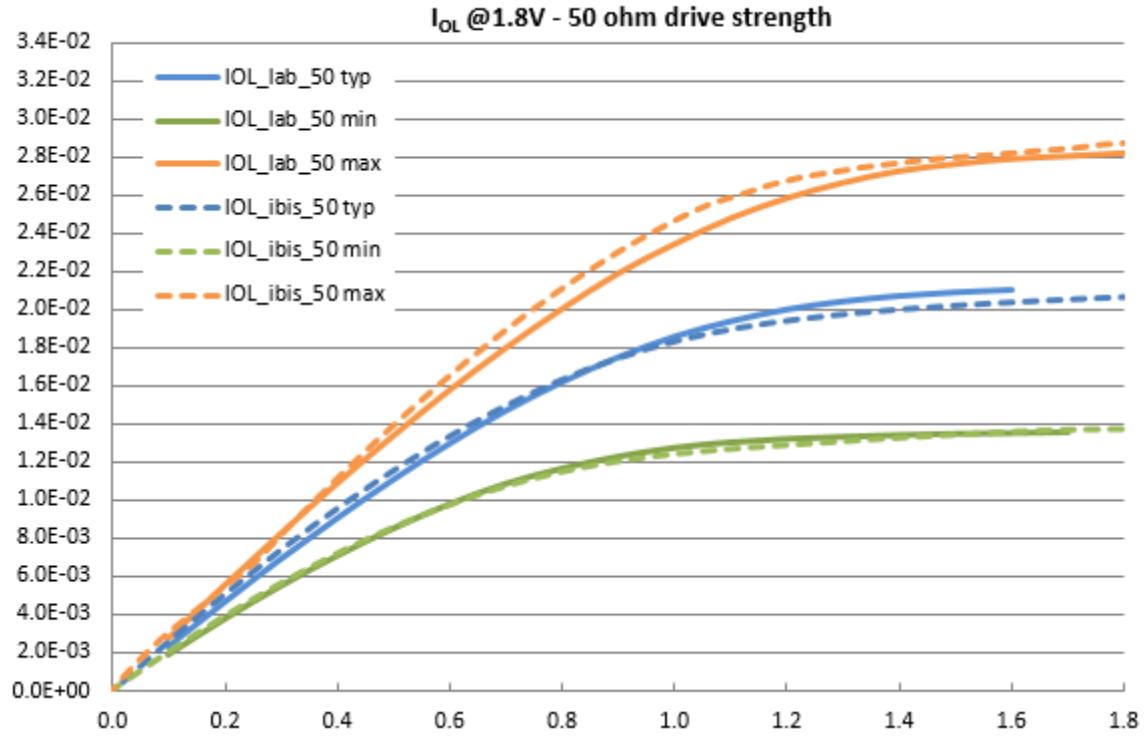
Measurement Correlation

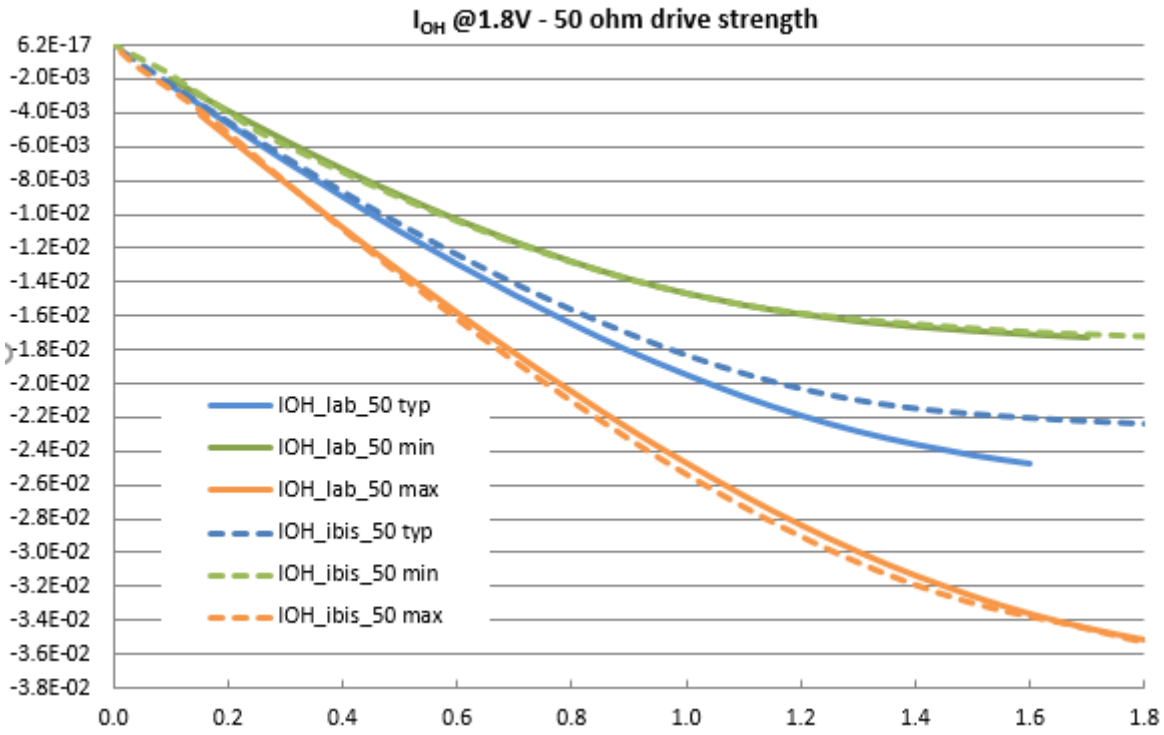
1. ☒ For Output or I/O models compare measured IOH/IOL data with IBIS pullup/pulldown data. Include measurement conditions in the image labels.

    a. Model name: **DAT_1p8_50_ohm**

        i. Pullup comparison. Measurement conditions:
        VCCQ(min,typ,max) = 1.7 , 1.85 , 1.95
        Temp(min,typ,max) = 105 , 25 , -40
        silicon corner lots: slow,typ,fast

        ii. Pulldown comparison. Measurement conditions:
        VCCQ(min,typ,max) = 1.7 , 1.85 , 1.95
        Temp(min,typ,max) = 105 , 25 , -40
        silicon corner lots: slow,typ,fast





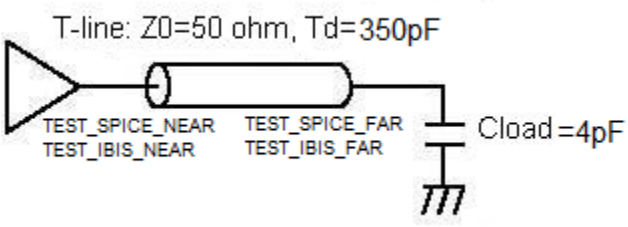
IBIS vs Spice Correlation

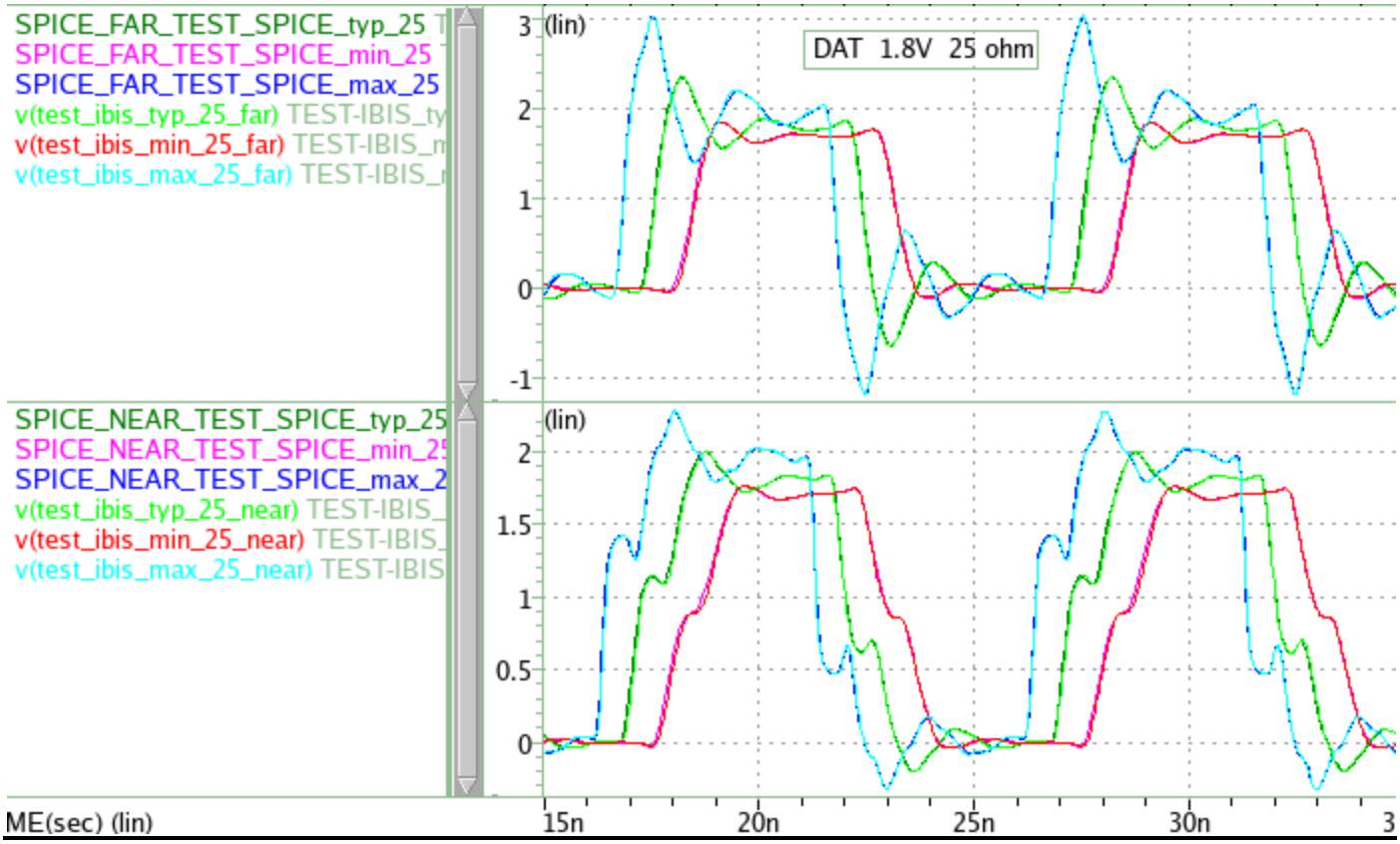
1. ☒ For all Output or I/O models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element).

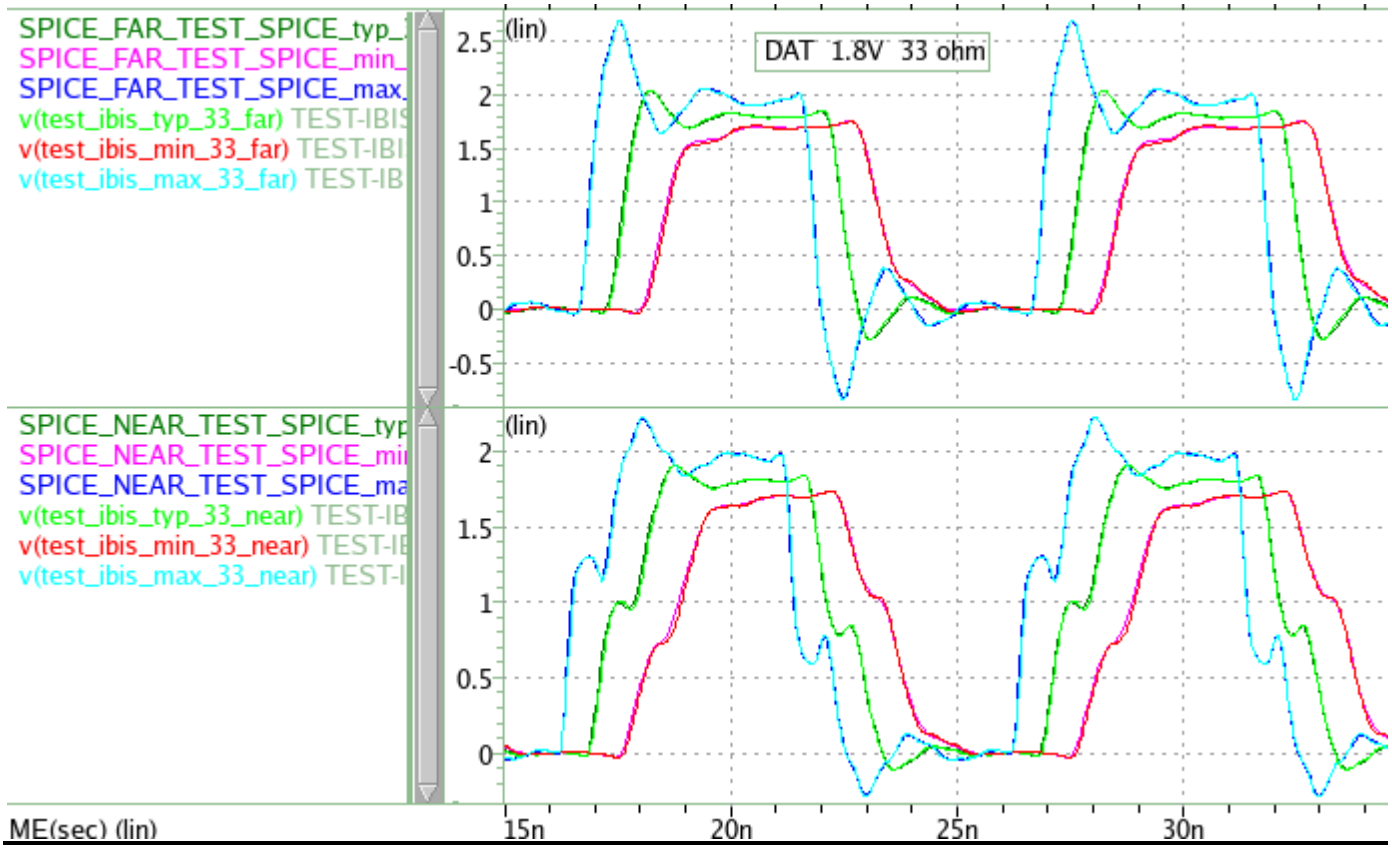
   a. ☒ Use the setup and node naming conventions shown below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations:
   SPICE: Cadence Spectre - Version 13.1.0.169 64bit
   IBIS: HSPICE H-2013.03-SP1 32-BIT

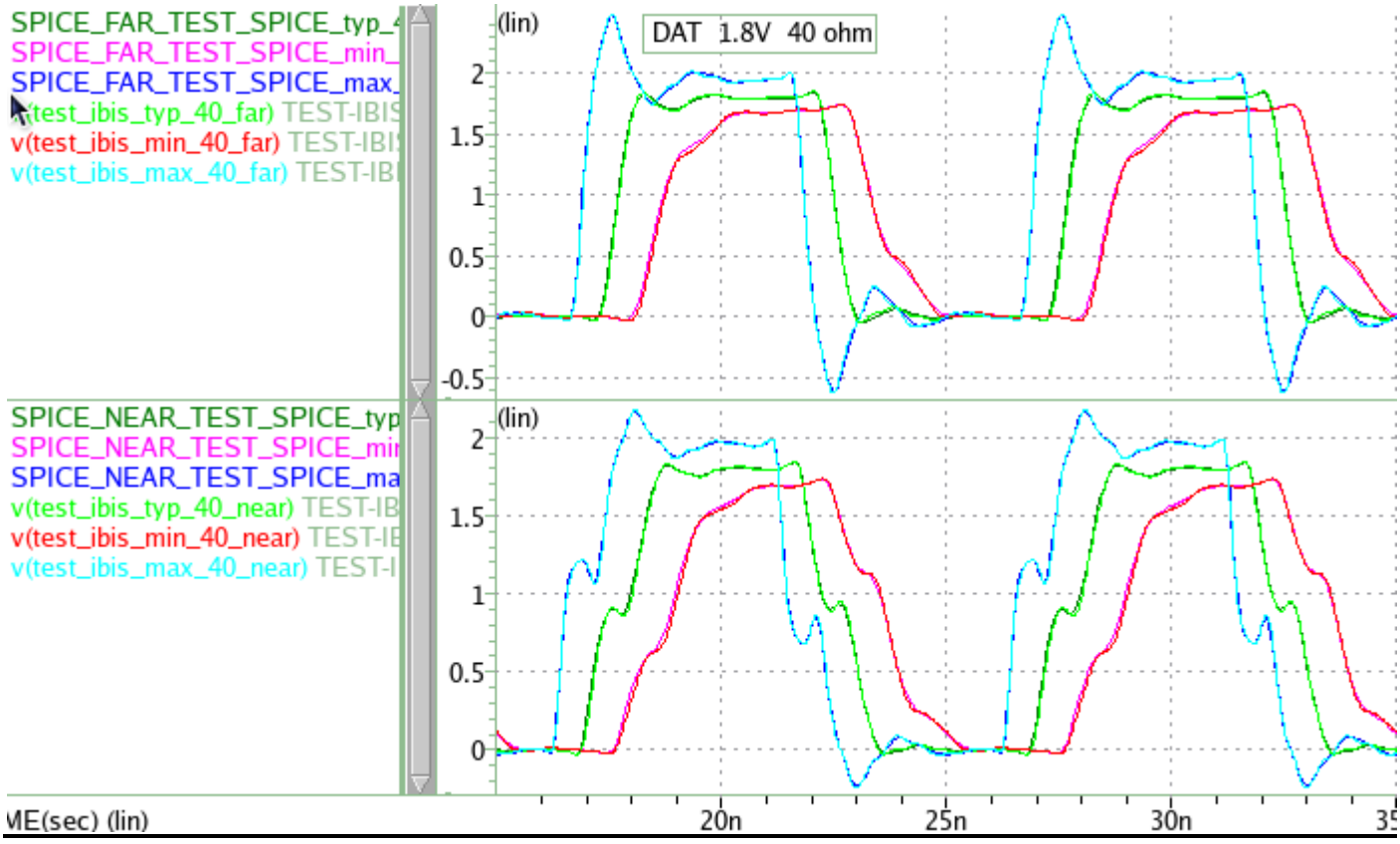
   b. ☒ Run simulations for all corners cases and at fastest speed grades, testing ODT models as loads when applicable.

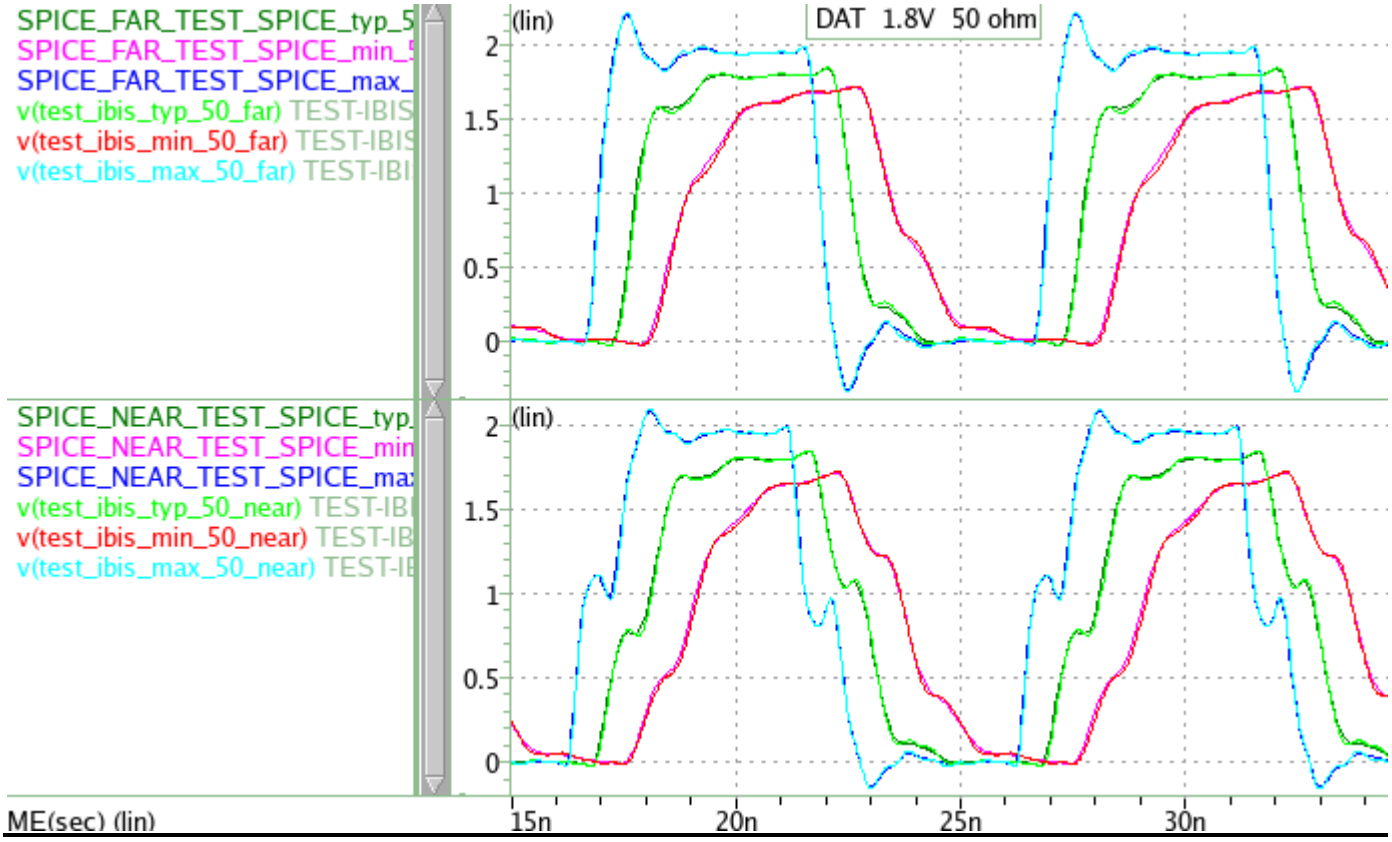
Setup

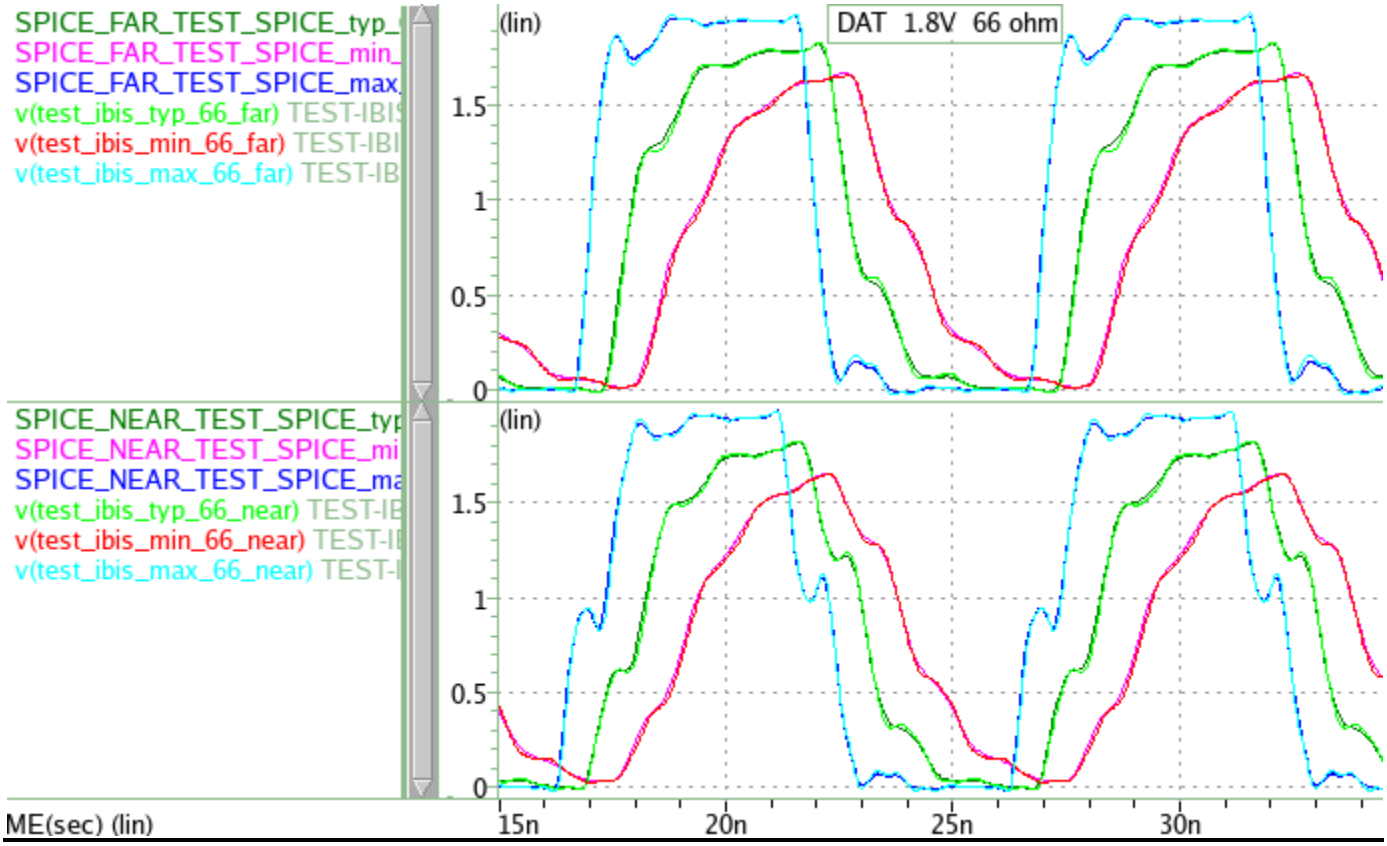


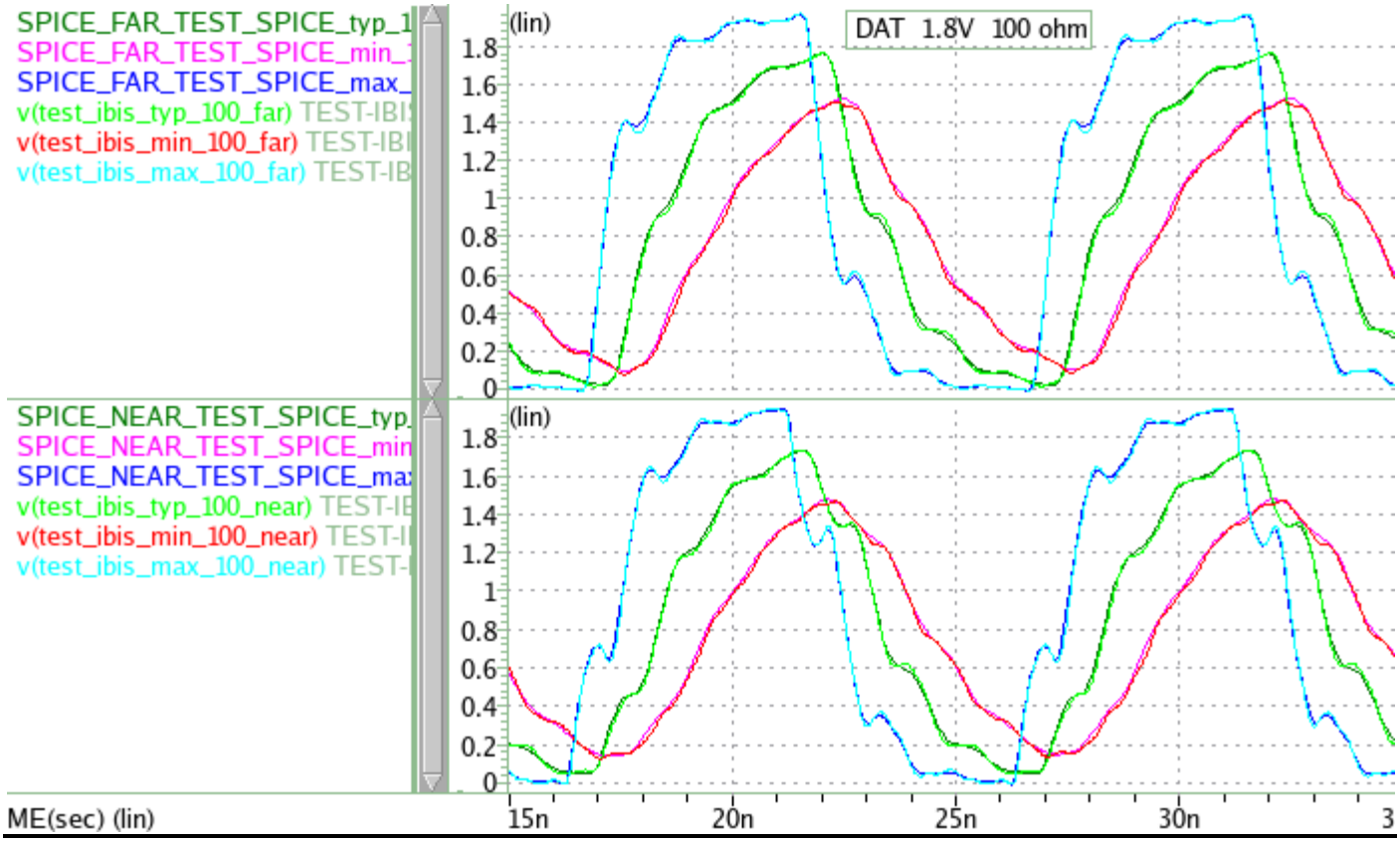


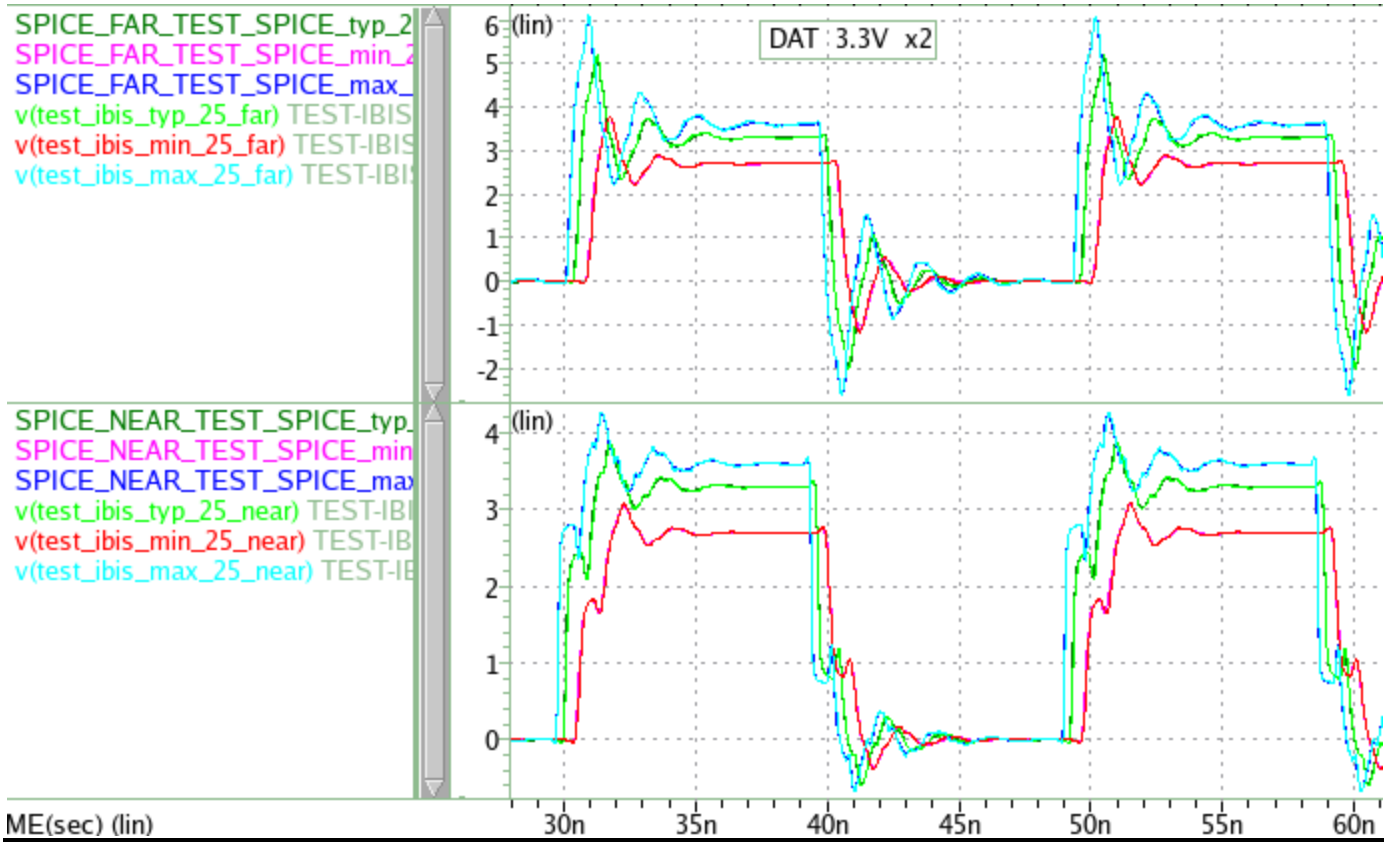


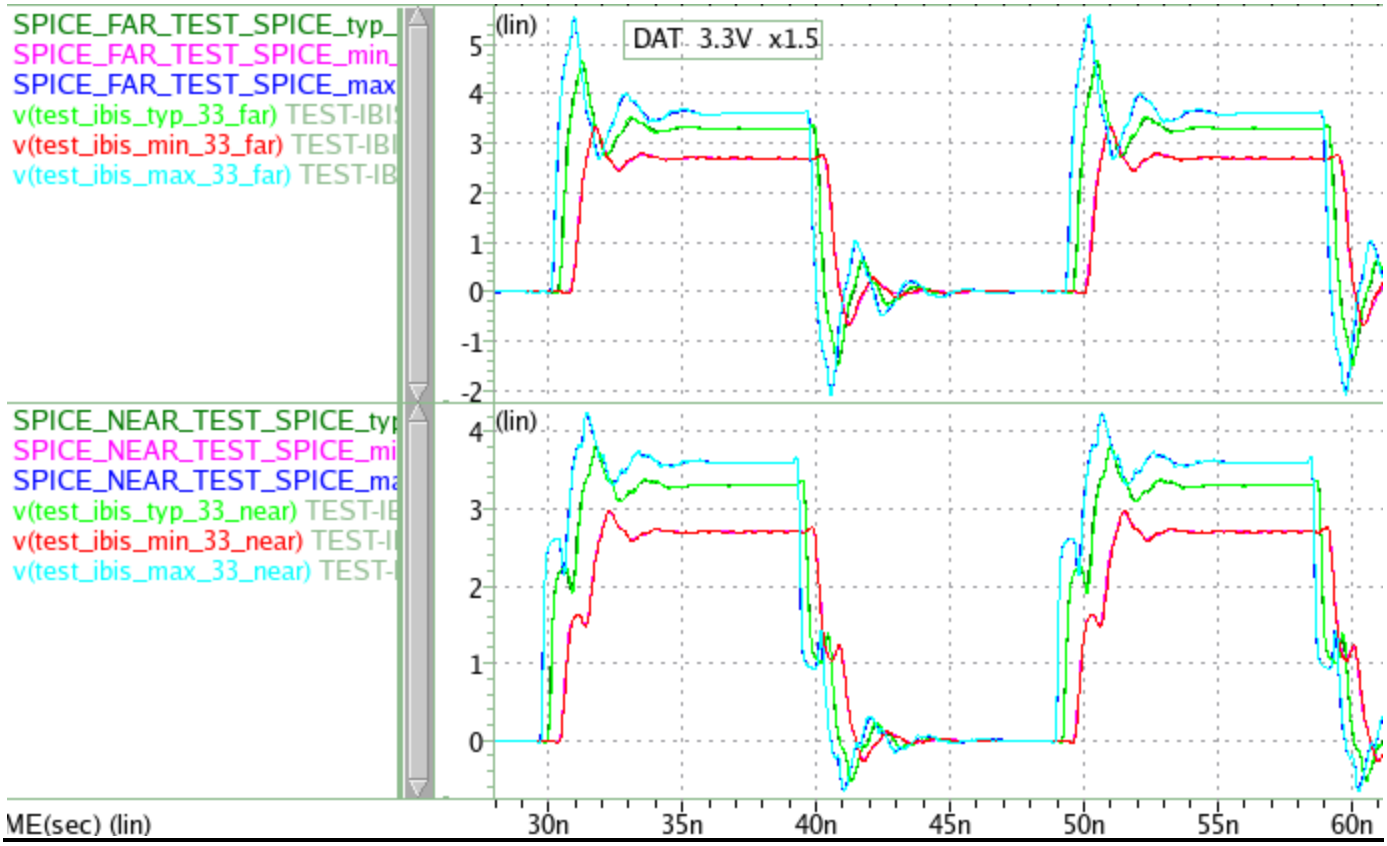


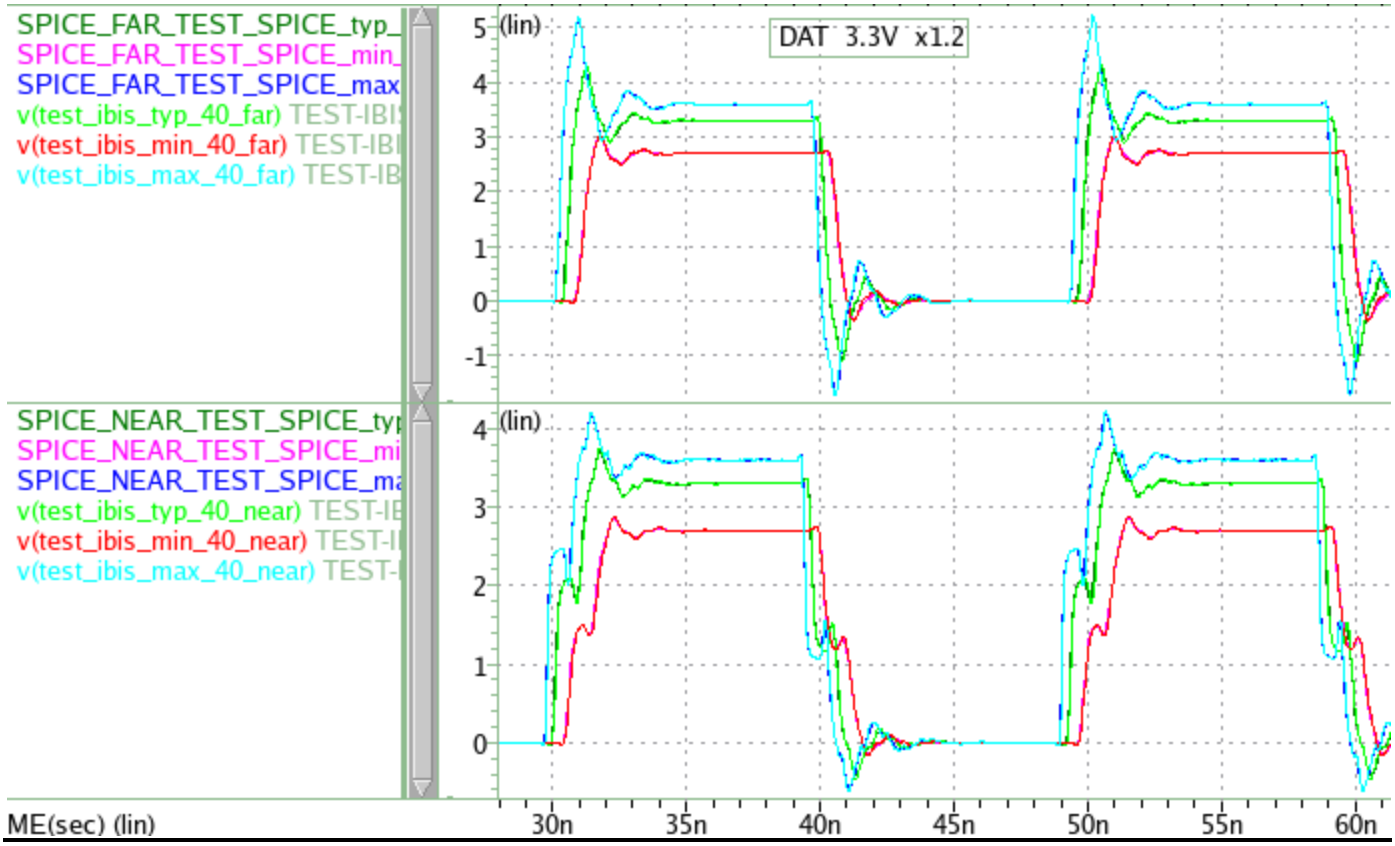


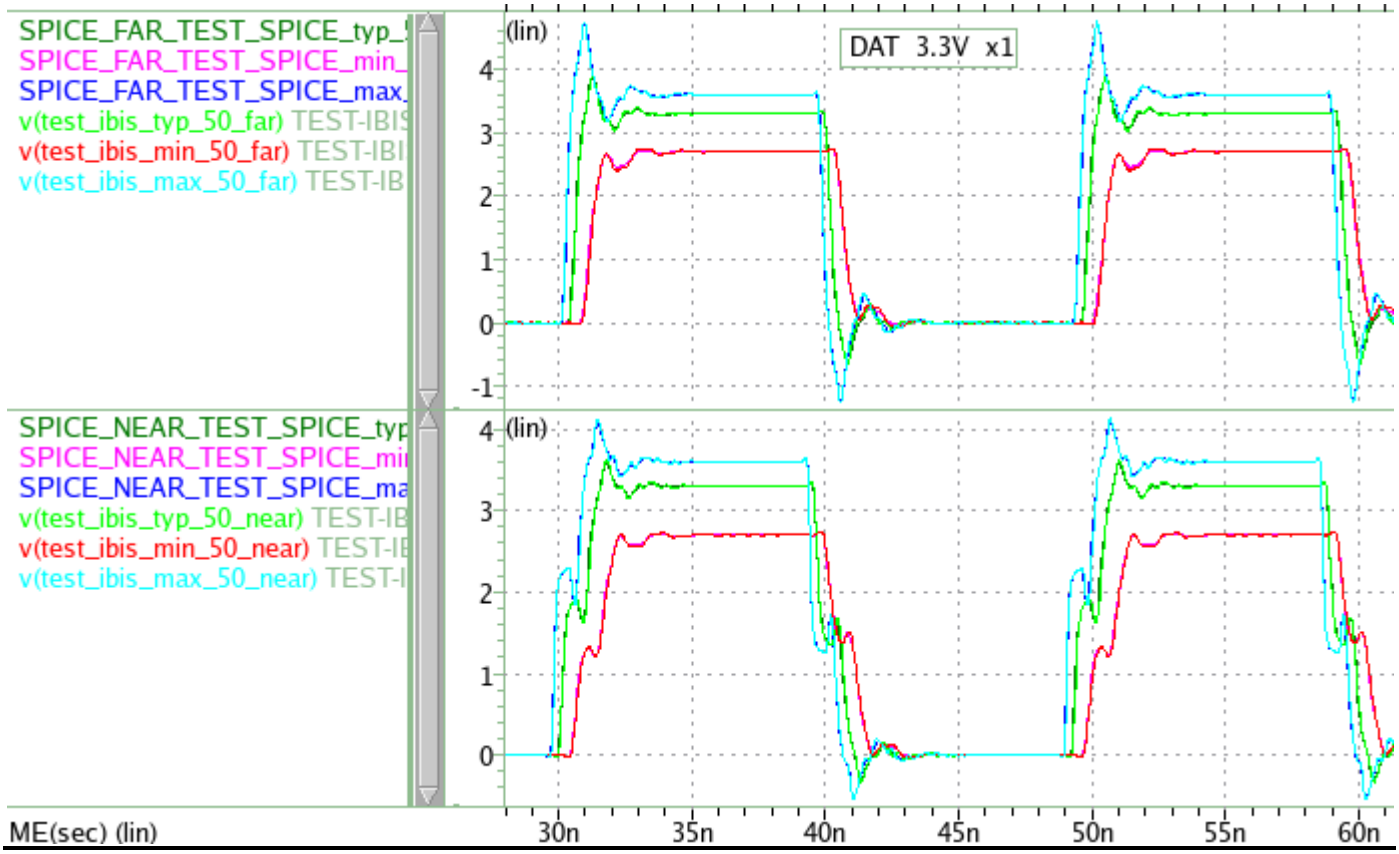


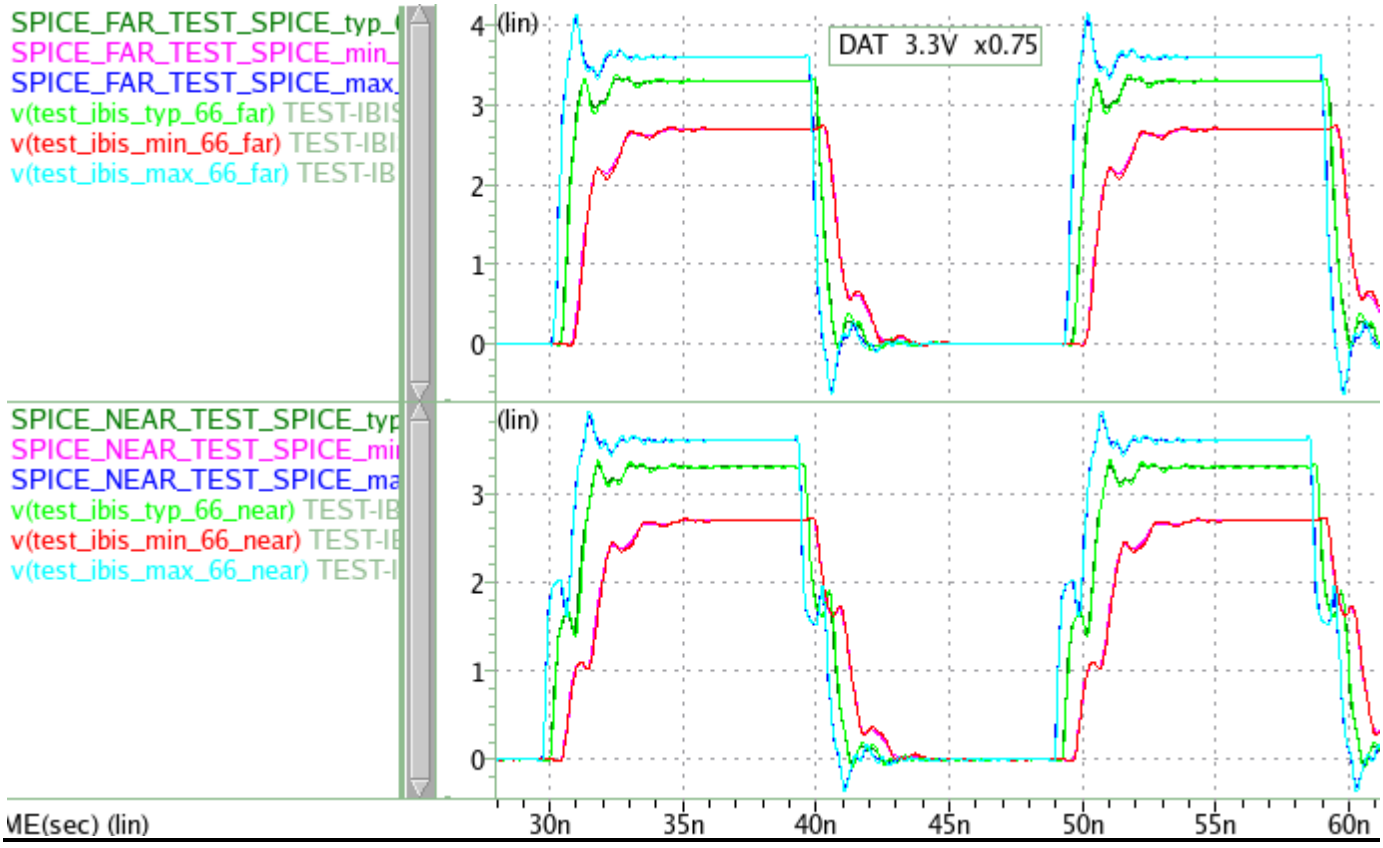


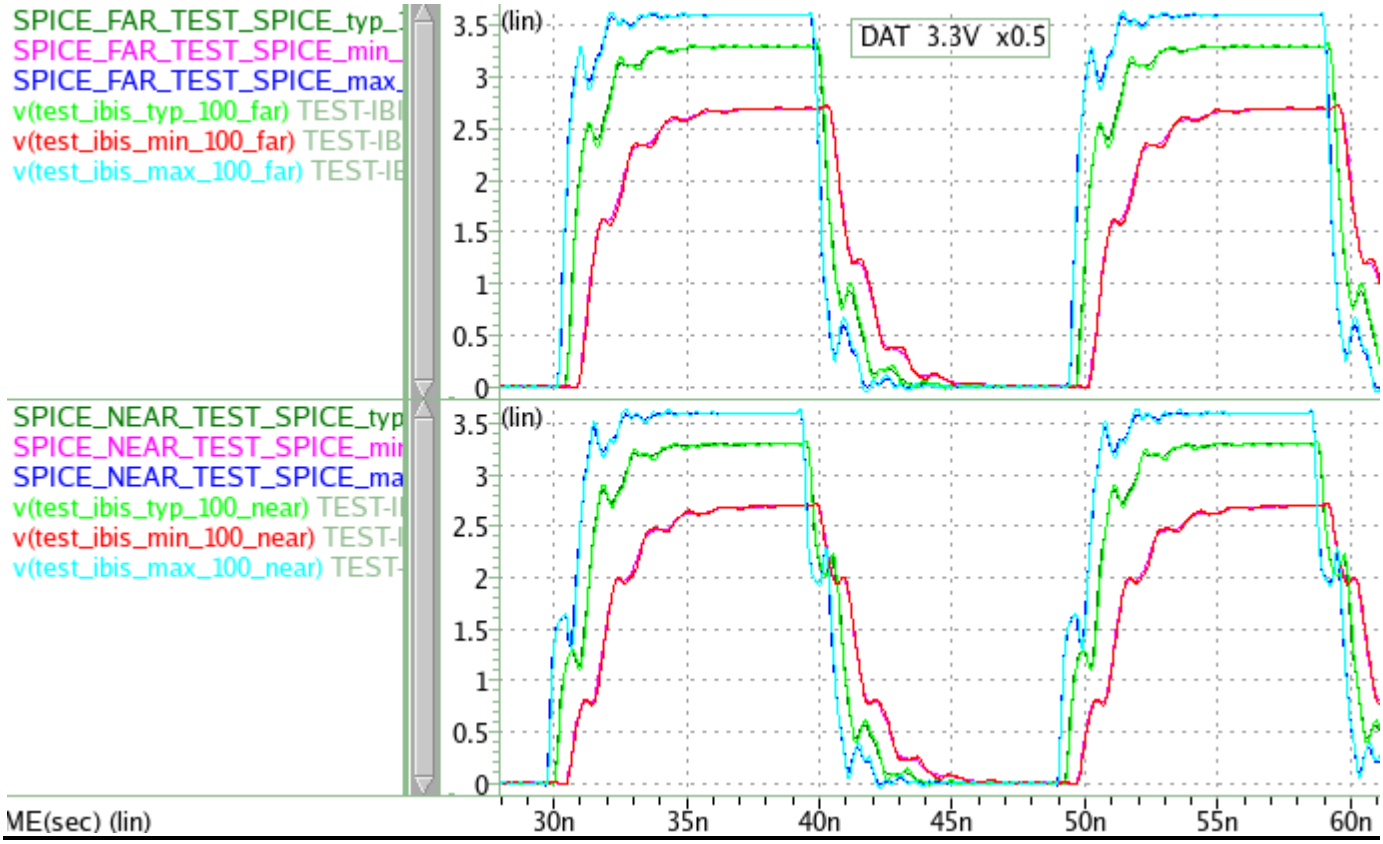












Comments:

Document Revision History

Rev **1.0** - Date **May 10, 2014**

a. IBIS revision **1.0 and later**
b. HSpice revision **N/A**

Rev **1.1** - Date **February 17, 2017**

a. IBIS revision **1.10 and later**
b. HSpice revision **N/A**