Design ID: F88R

Description: 1.125Gb RLDRAM3

Marketing device name(s): MT44K64M18RB, MT44K32M36RB

Valid speed grades: RL3-1866, RL3-2133, RL3-2400

Zip filename: f88r_ibis.zip

IBIS filename (Version 5.0): f88r.ibs, f88r_it.ibs **File rev:** 2.0

HSPICE filename: f88r_hspice.zip **File rev:** 2.0

Die revision: A

Date: September 12, 2016

Datasheet Link (from micron.com):
https://www.micron.com/~/media/documents/products/data-sheet/dram/1,-d-,125gb_x18_x36_rldram3.pdf

E-mail modelsupport@micron.com for questions regarding Quality Report.

Device Parameters

VDDQ **Slow:** 1.14V **Typical:** 1.20V **Fast:** 1.26V

VDD **Slow:** 1.28V **Typical:** 1.35V **Fast:** 1.42V

Junction Temperature (Commercial) **Slow:** 110C **Typical:** 50C **Fast:** 0C

Junction Temperature (Industrial) **Slow:** 110C **Typical:** 50C **Fast:** -40C

VDDQ/VSSQ Decoupling Capacitance (Approximate value at 10MHz) – Full Die: 17.4nF

Included in HSPICE DQ/DM/DK/QK models? Yes **Amount per DQ model:** 334pF

Included in IBIS DQ/DM/DK/QK models? No, must be included with separate Spice subcircuit (.ckt files) found in the zip file.

VDDQ/VSSQ Decoupling Capacitance ESR – Full Die: 0.038ohms

VDDQ/VSSQ Decoupling Capacitance ESR – per DQ model: ~2ohms

IBIS Quality Summary

1. ☒ Include the IBIS Quality Specification 2.0 Overall IBIS Quality level. For details on IBIS Quality, reference the quality specification and quality checklist on IBIS quality webpage http://www.ibis.org/quality_wip/checklist.html.

   Overall IBIS Quality Level: **IQ3MSX**

   Exceptions: **V-t length in Version 5.0 model is excessive due to inclusion of [Composite Current] I-t data.**

2. ☒ Include the filename of the IBIS Quality Checklist that accompanies this report.

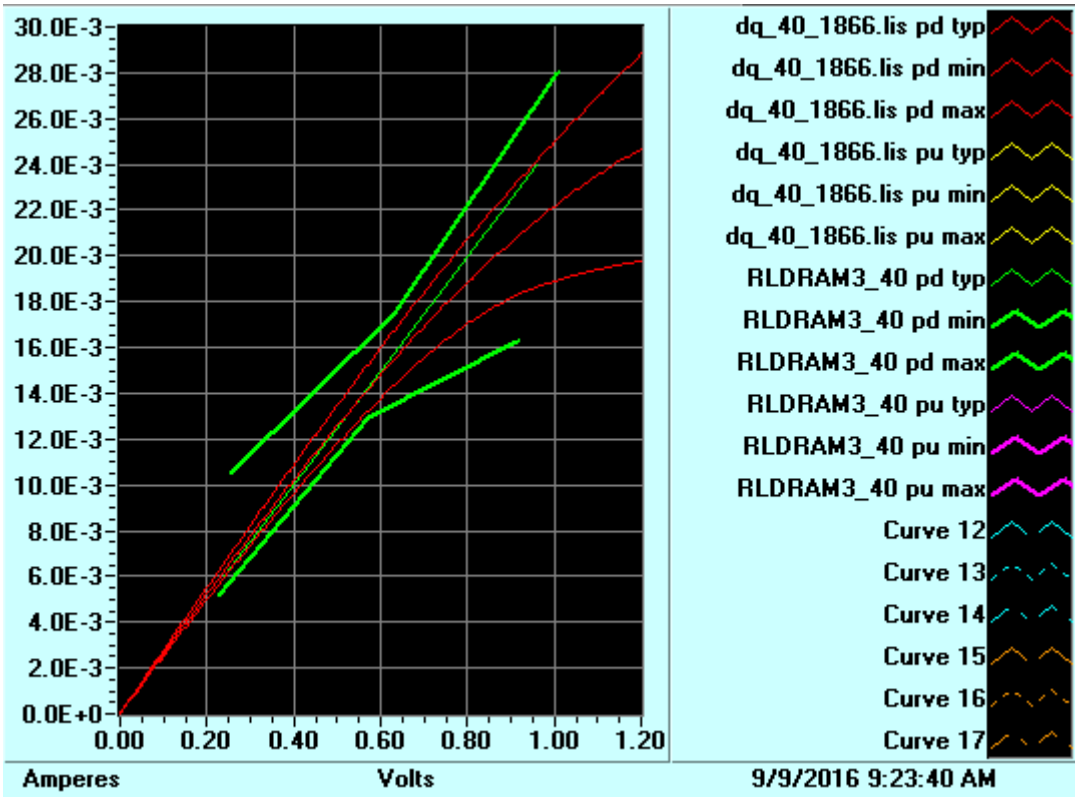
   Filename: **f88r_ibis_quality_checklist.xls**

IBIS Model Correlation: datasheet

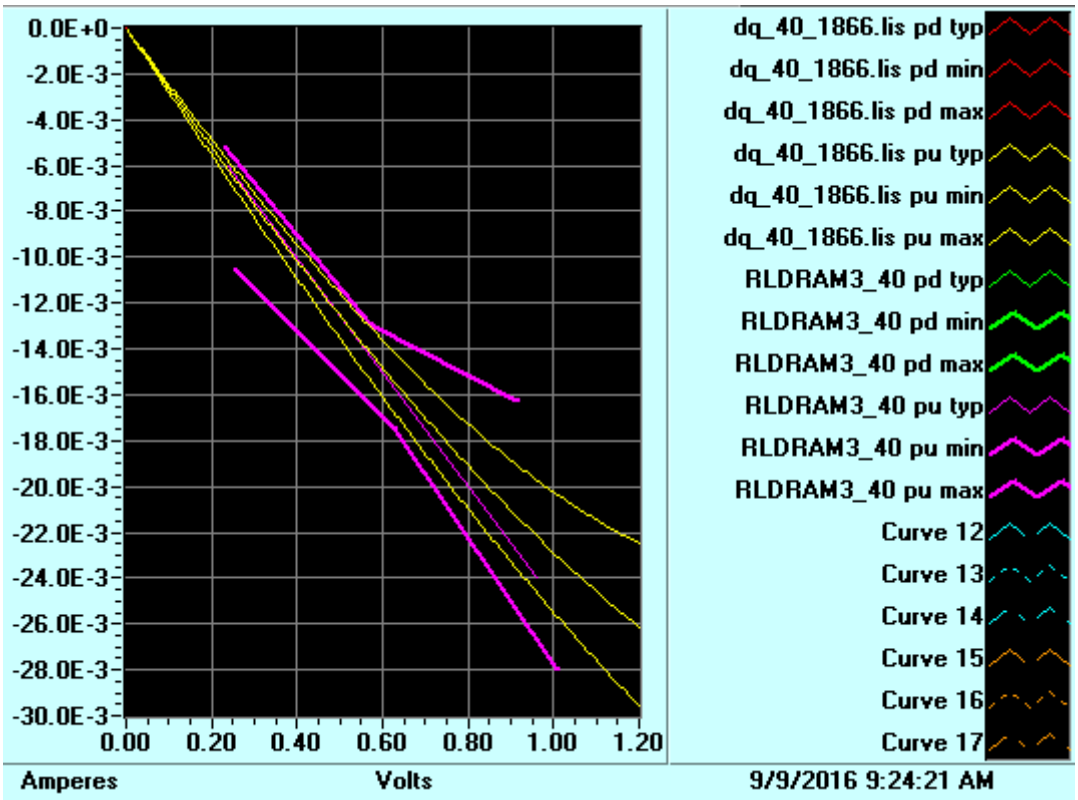
1. ☒ For Output or I/O model compare datasheet IOH/IOL data with IBIS pullup/pulldown data.

a. Model name: **DQ_40**

i. Pulldown I-V versus **RLDRAM3** specification

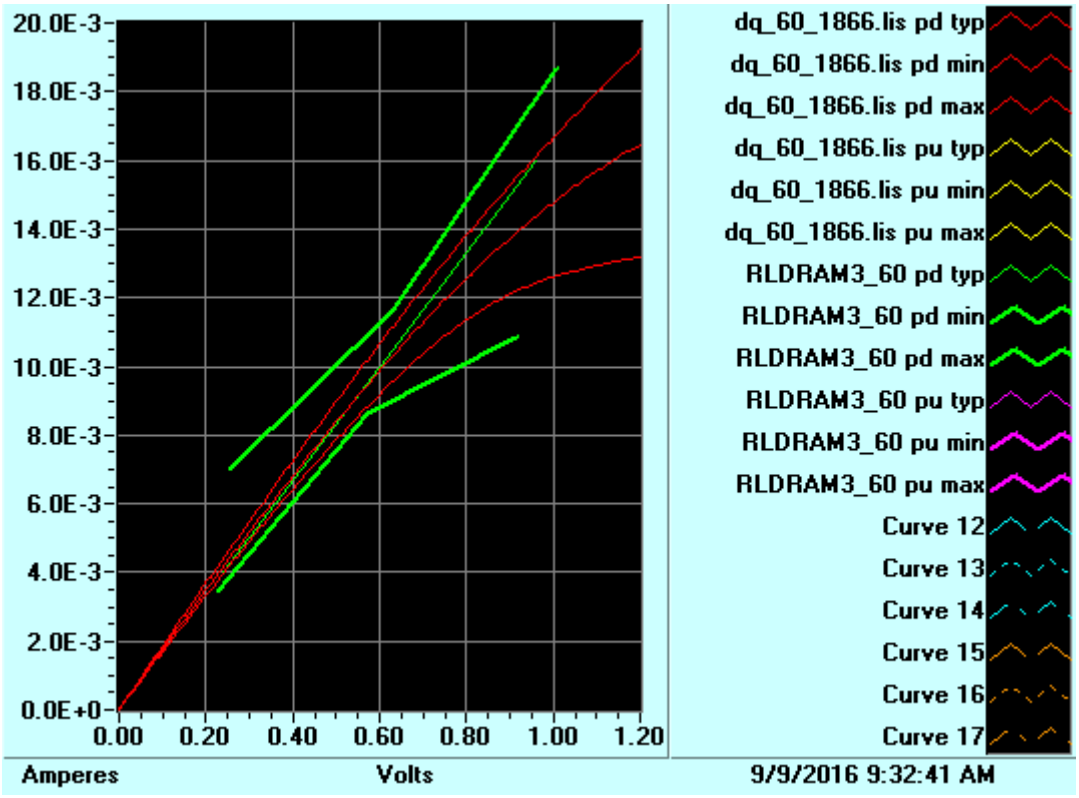


ii. Pullup I-V versus **RLDRAM3** specification

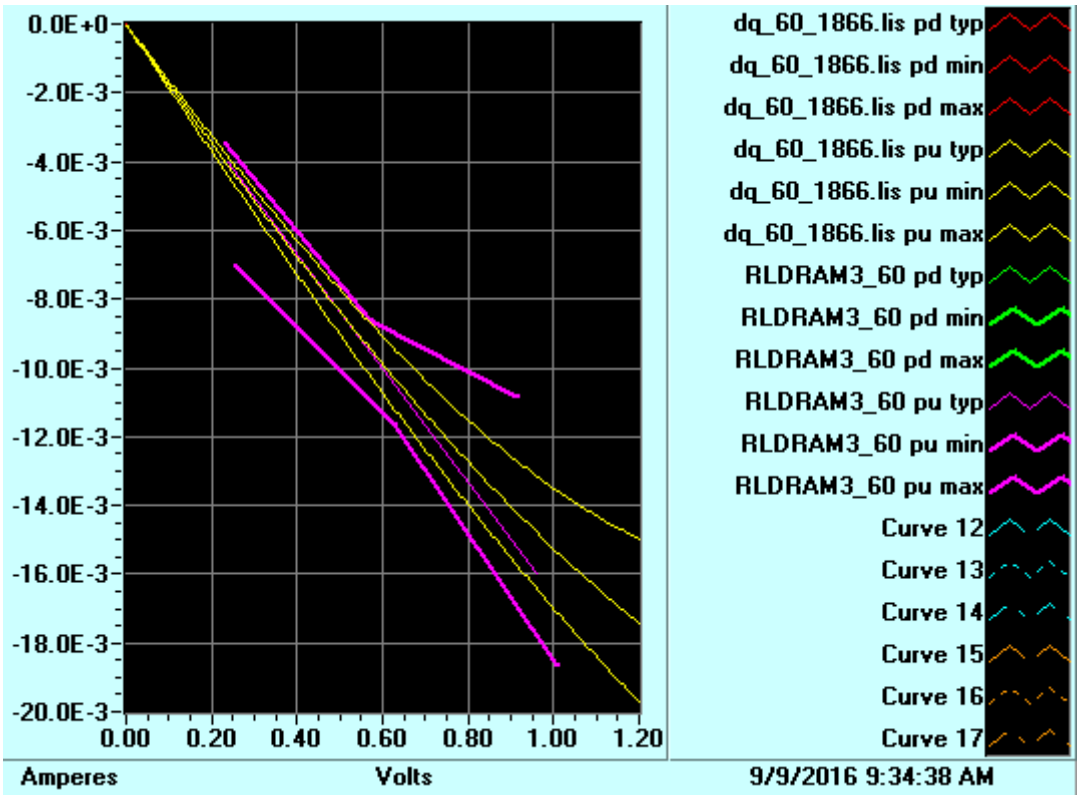


b. Model name: **DQ_60**

i. Pulldown I-V versus **RLDRAM3** specification



ii. Pullup I-V versus **RLDRAM3** specification



2. ☒ Compare C_comp with datasheet Input Capacitance. Provide C_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16).

Component name: **MT44K64M18RB, MT44K32M36RB**

Signal	IBIS pkg min [pF]	IBIS pkg max [pF]	IBIS die min [pF]	IBIS die max [pF]	IBIS tot min [pF]	IBIS tot max [pF]	Spec min [pF]	Spec max [pF]
DQ/DM/DK/QK	0.92	1.14	1.13	1.33	**2.06**	**2.47**	**1.90**	**3.10**
INPUT	1.00	1.18	0.28	0.48	**1.28**	**1.66**	**1.25**	**2.25**
CLK	0.81	0.82	0.45	0.65	**1.26**	**1.47**	**1.30**	**2.10**
JTAG IN	0.75	0.97	0.38	0.58	**1.13**	**1.55**	**1.50**	**4.50**
JTAG OUT	0.93	0.93	0.78	0.98	**1.71**	**1.91**	**1.50**	**4.50**

3. ☒ If slew rate specifications (rise/fall slew) are available from the datasheet, complete Spice simulations to generate slew rate data and provide a comparison table.

Model	IBIS slew rate RISE [V/ns] typ	IBIS slew rate RISE [V/ns] min	IBIS slew rate RISE [V/ns] max	SPEC slew rate RISE [V/ns] min	SPEC slew rate RISE [V/ns] max
DQ_40	3.64	2.75	4.10	**2.50**	**6.00**

Model	IBIS slew rate FALL [V/ns] typ	IBIS slew rate FALL [V/ns] min	IBIS slew rate FALL [V/ns] max	SPEC slew rate FALL [V/ns] min	SPEC slew rate FALL [V/ns] max
DQ_40	3.66	2.76	4.01	**2.50**	**6.00**

4. ☒ Compare ODT data with datasheet.

ODT calculated using the formula: $RTT = (V_{IH(ac)} - V_{IL(ac)}) / |(I(V_{IH(ac)}) - I(V_{IL(ac)})|$

ODT40	TYP	MIN	MAX
Vil (V)	0.450	0.420	0.480
Vih (V)	0.750	0.720	0.780
Ivil (A)	-0.003	-0.003	-0.004
Ivih (A)	0.003	0.003	0.004
	TYP	MIN	MAX
Rtt (Model)	45.39	50.79	40.54
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	40	64	36

ODT60	TYP	MIN	MAX
Vil (V)	0.450	0.420	0.480
Vih (V)	0.750	0.720	0.780
Ivil (A)	-0.002	-0.002	-0.003
Ivih (A)	0.002	0.002	0.002
	TYP	MIN	MAX
Rtt (Model)	68.08	76.05	60.80
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	60	96	54

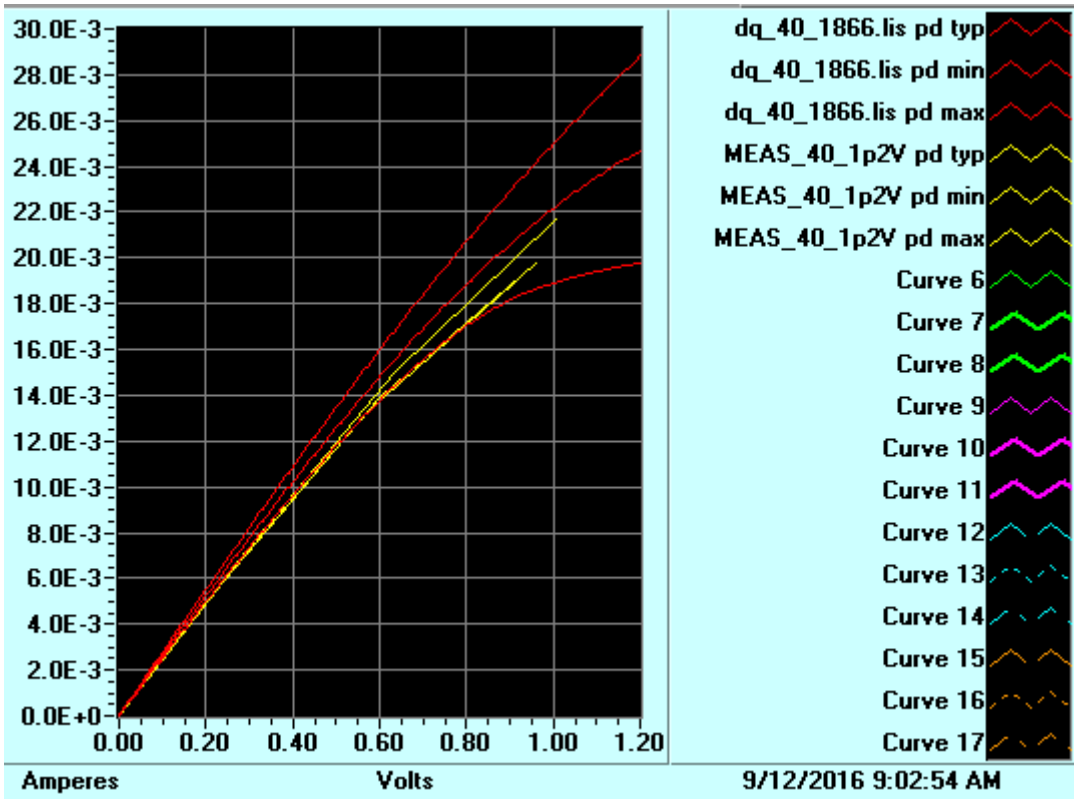
ODT120	TYP	MIN	MAX
Vil (V)	0.450	0.420	0.480
Vih (V)	0.750	0.720	0.780
Ivil (A)	-0.001	-0.001	-0.001
Ivih (A)	0.001	0.001	0.001
	TYP	MIN	MAX
Rtt (Model)	136.10	152.26	121.55
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	120	192	108

IBIS Model Correlation: measurements

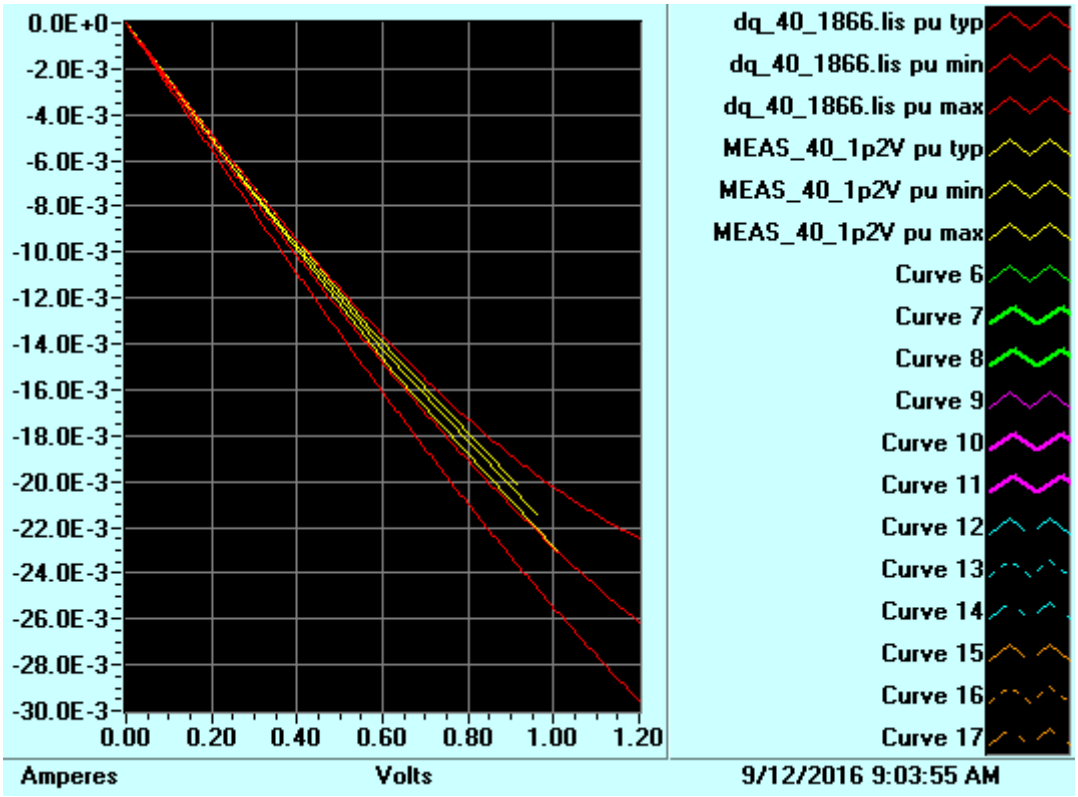
1. ☒ For Output or I/O models compare measured IOH/IOL data with IBIS pullup/pulldown data. If the measurement conditions are different from the IBIS conditions, run Spice simulations using the same measurement conditions such as VCC, temperature, and process. Include measurement conditions in the image labels.

a. Model name: **DQ_40**

i. Pullup comparison. Measurement conditions: **1.2V/25C, 1.14V/95C, and 1.26V/0C**

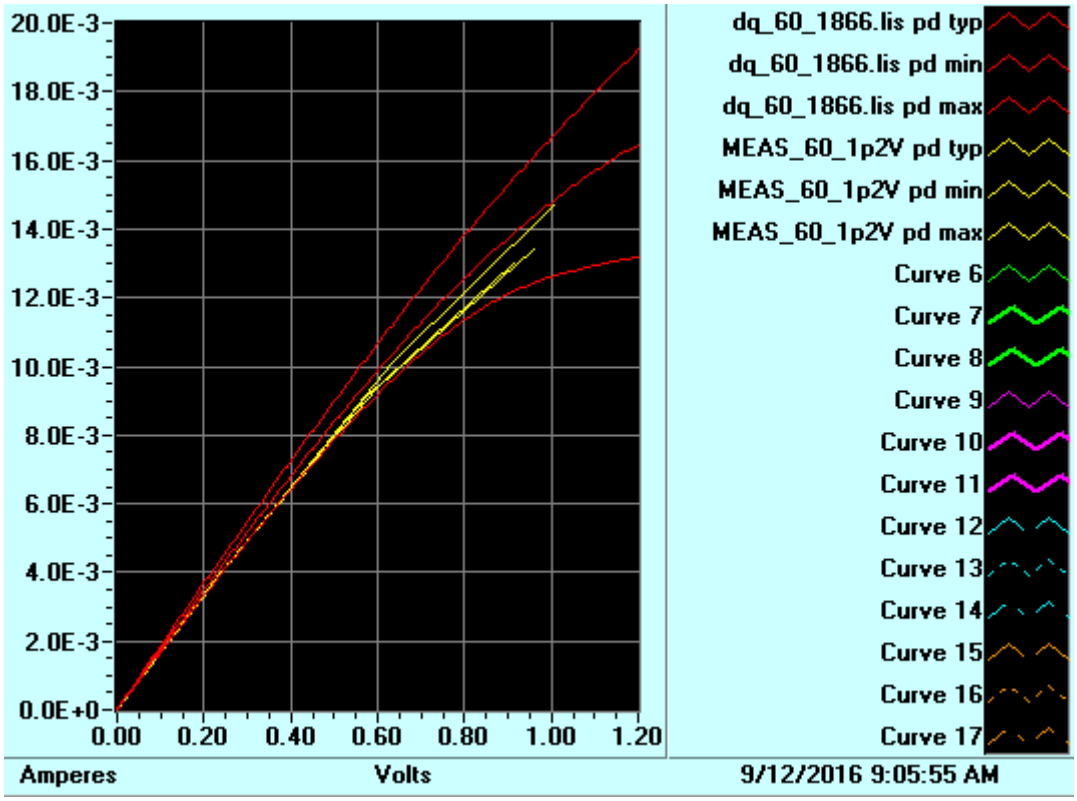


ii. Pulldown comparison. Measurement conditions: **1.2V/25C, 1.14V/95C, and 1.26V/0C**

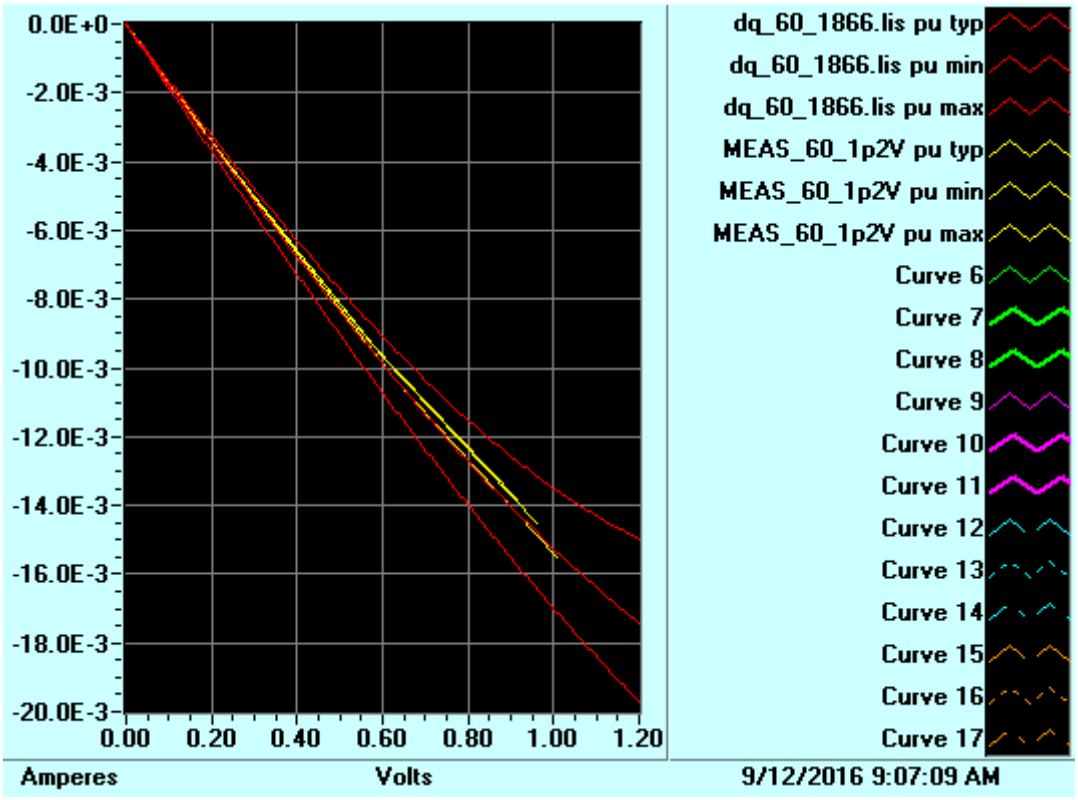


b. Model name: **DQ_60**

i. Pullup comparison. Measurement conditions: **1.2V/25C, 1.14V/95C, and 1.26V/0C**



ii. Pulldown comparison. Measurement conditions: **1.2V/25C, 1.14V/95C, and 1.26V/0C**



2. ☒ Compare C_comp with measured C_comp. Provide C_comp comparison table for all models and for all package combinations (i.e x4, x8 and x16).

Component name: **MT44K64M18RB, MT44K32M36RB**

Signal	IBIS pkg min [pF]	IBIS pkg max [pF]	IBIS die min [pF]	IBIS die max [pF]	IBIS tot min [pF]	IBIS tot max [pF]	Measured min [pF]	Measured max [pF]
DQ/DM/DK/QK	0.92	1.14	1.13	1.33	**2.06**	**2.47**	**2.19**	**2.54**
INPUT	1.00	1.18	0.28	0.48	**1.28**	**1.66**	**1.37**	**1.56**
CLK	0.81	0.82	0.45	0.65	**1.26**	**1.47**	**1.33**	**1.40**
JTAG IN	0.75	0.97	0.38	0.58	**1.13**	**1.55**	**1.23**	**1.40**
JTAG OUT	0.93	0.93	0.78	0.98	**1.71**	**1.91**	**1.80**	**1.82**

3. ☐ If measured clamp current data is available, provide an IBIS versus measurement comparison for all models. Include measurement conditions in the image labels.

Not Available

4. ☒ If slew rate data (rise/fall slew) is available from measurements, complete Spice simulations to generate slew rate data and provide a comparison table.

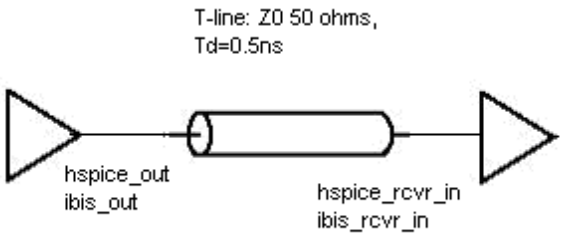
Model	IBIS slew rate RISE [V/ns] typ	IBIS slew rate RISE [V/ns] min	IBIS slew rate RISE [V/ns] max	MEAS slew rate RISE [V/ns] min	MEAS slew rate RISE [V/ns] max
DQ_40	3.31	2.57	3.72	**2.73**	**3.79**

Model	IBIS slew rate FALL [V/ns] typ	IBIS slew rate FALL [V/ns] min	IBIS slew rate FALL [V/ns] max	MEAS slew rate FALL [V/ns] min	MEAS slew rate FALL [V/ns] max
DQ_40	3.35	2.57	3.68	**2.83**	**3.74**

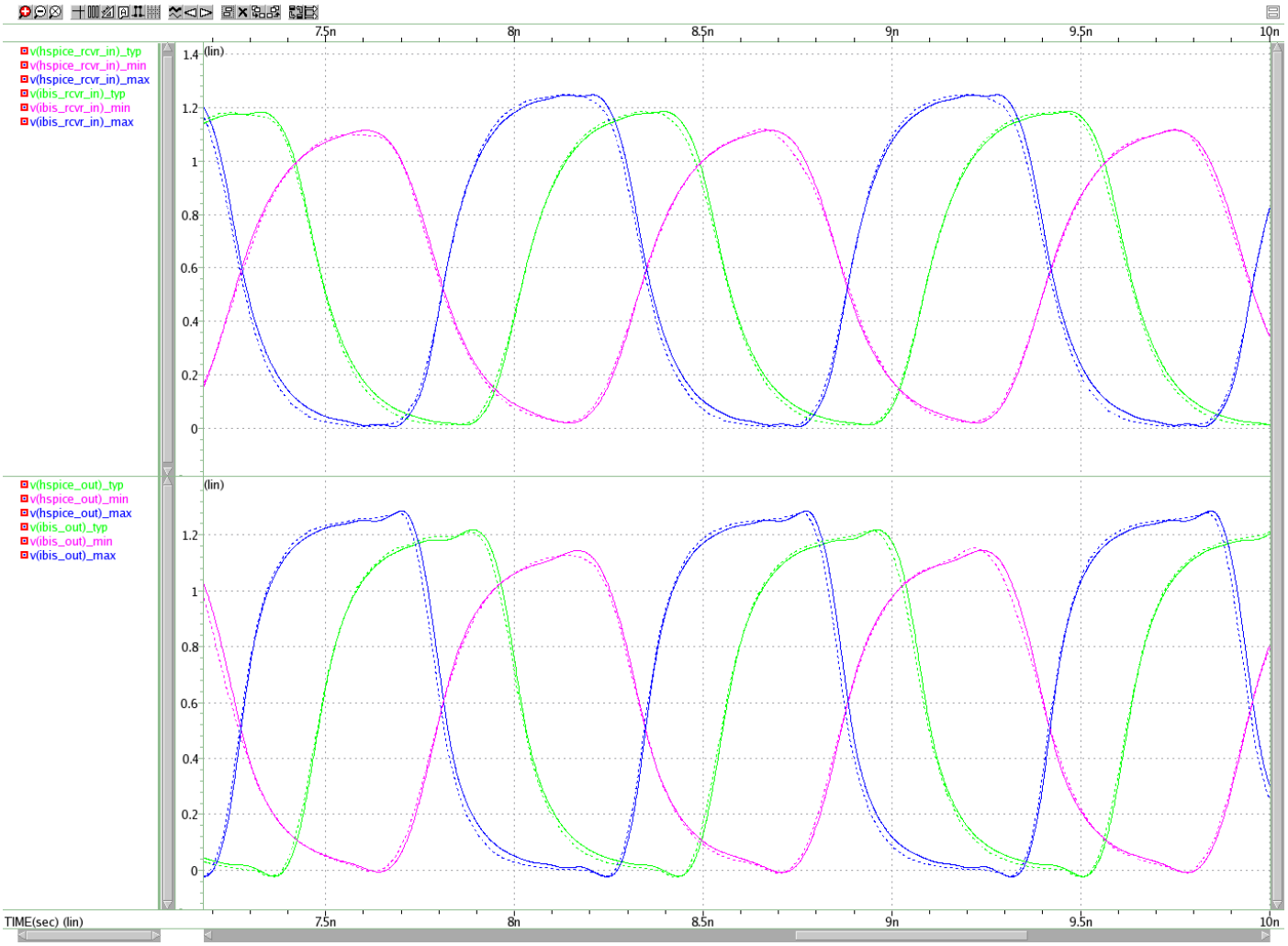
IBIS Model Correlation: IBIS vs Spice (IBIS 4.2)

1. ☒ For all Output or I/O models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element).
   a. ☒ Use the setup and node naming conventions shown below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations: **HPSICE 2016.06**
   b. ☒ Run simulations for all corners cases and at fastest speed grades, testing ODT models as loads when applicable

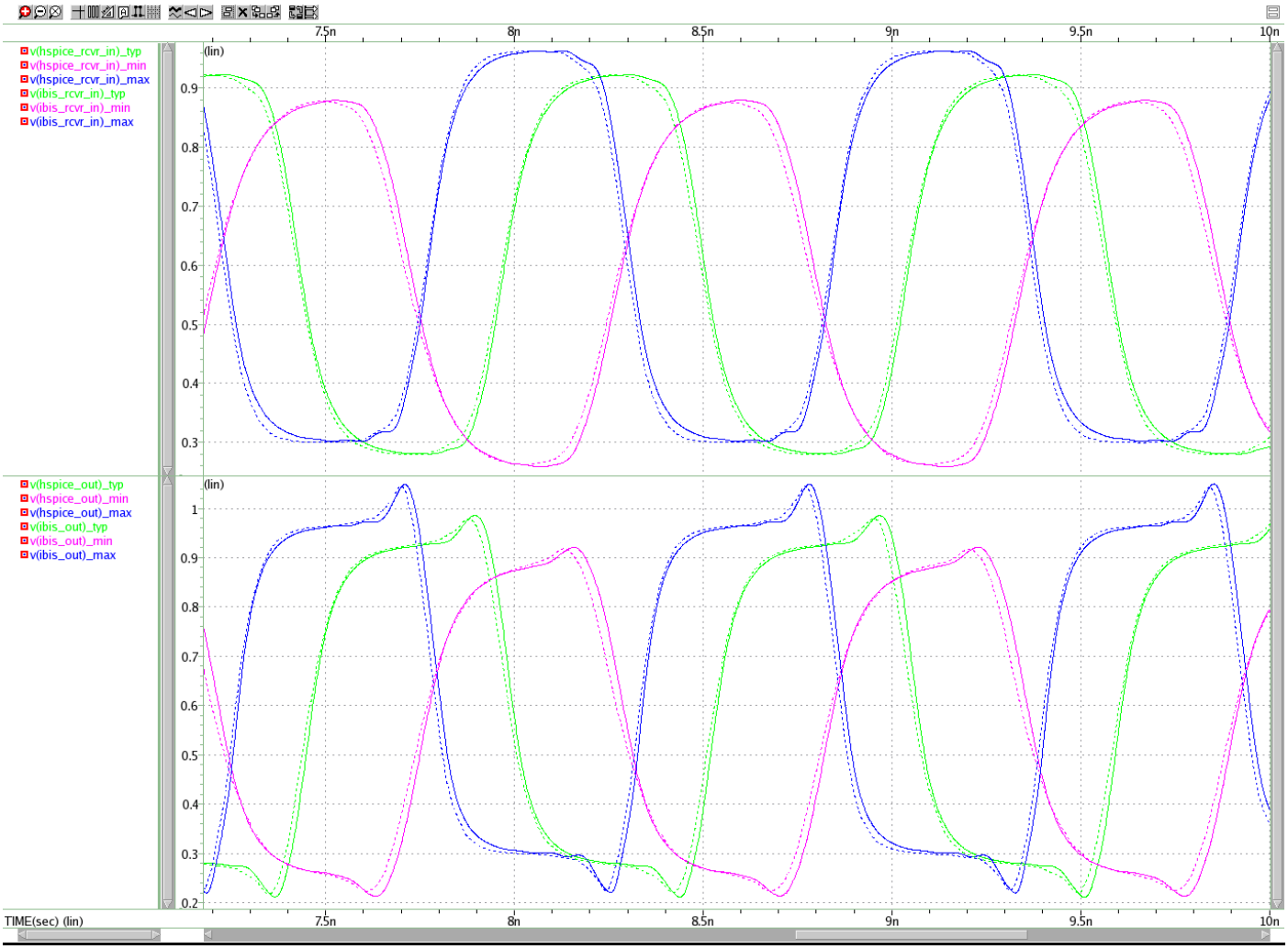
SETUP:



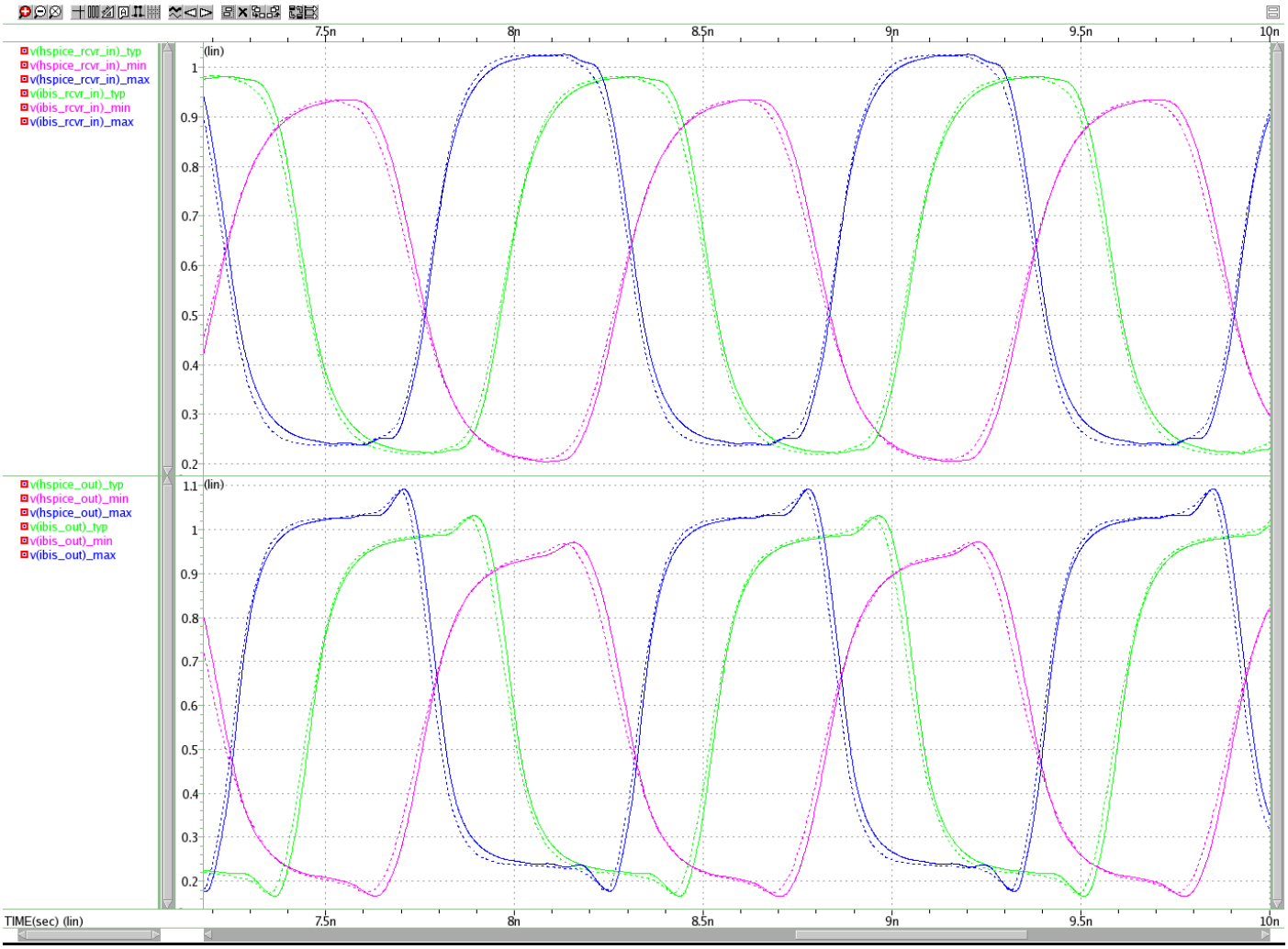
i. **DQ_40_1866** driving **DQ_40_1866**



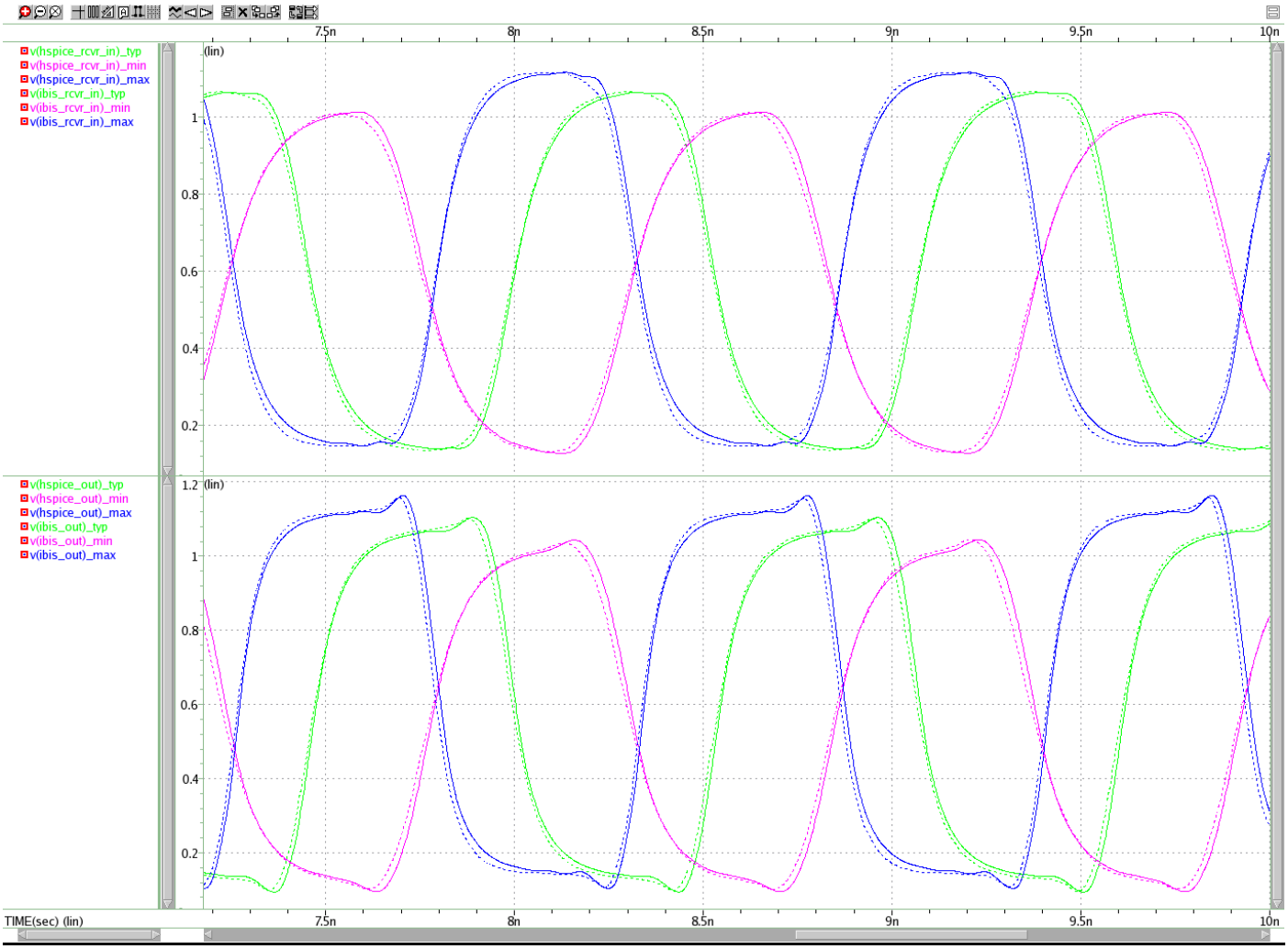
ii. **DQ_40_1866** driving **DQ_40_ODT40_1866**



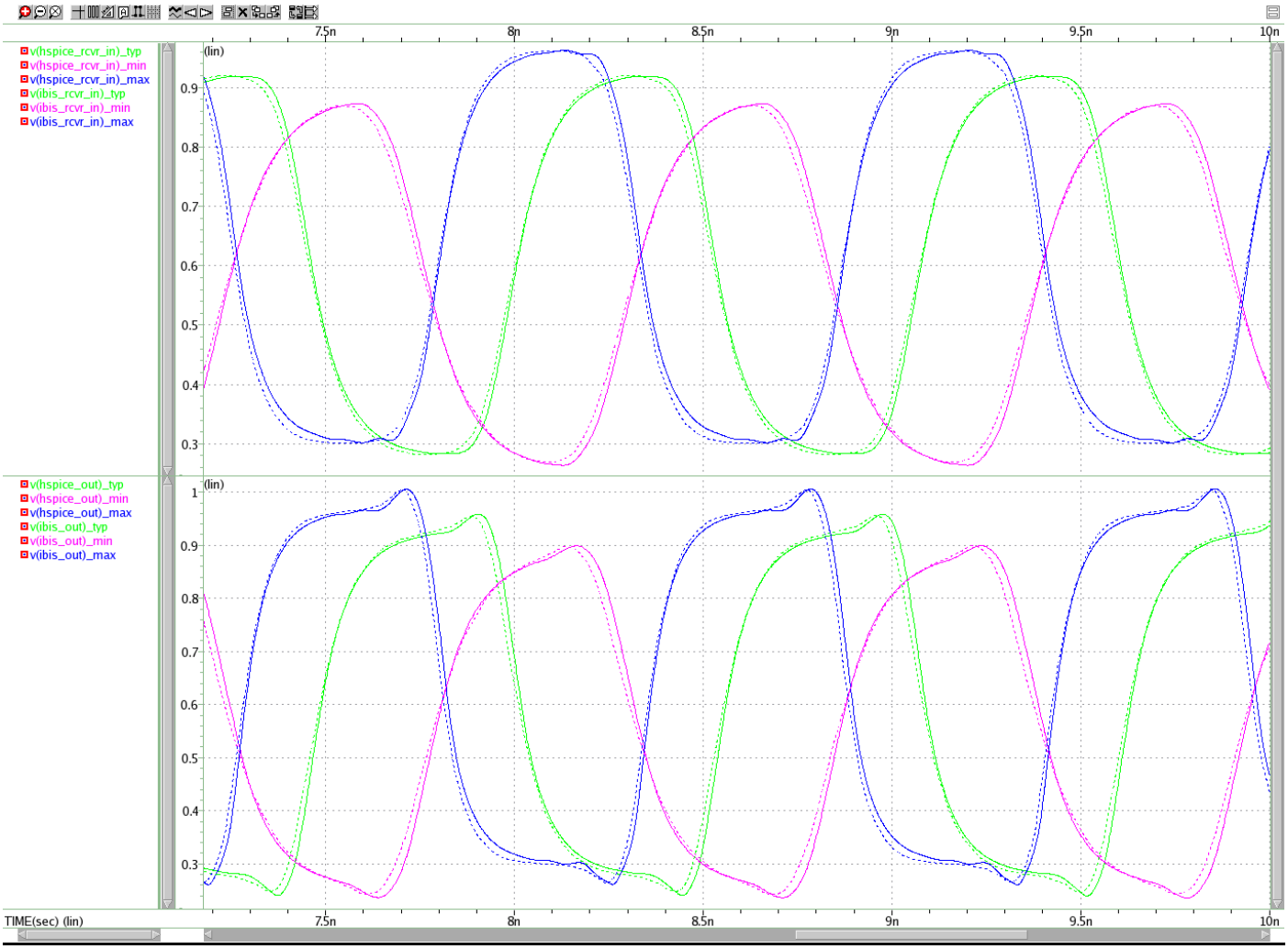
iii. **DQ_40_1866** driving **DQ_40_ODT60_1866**



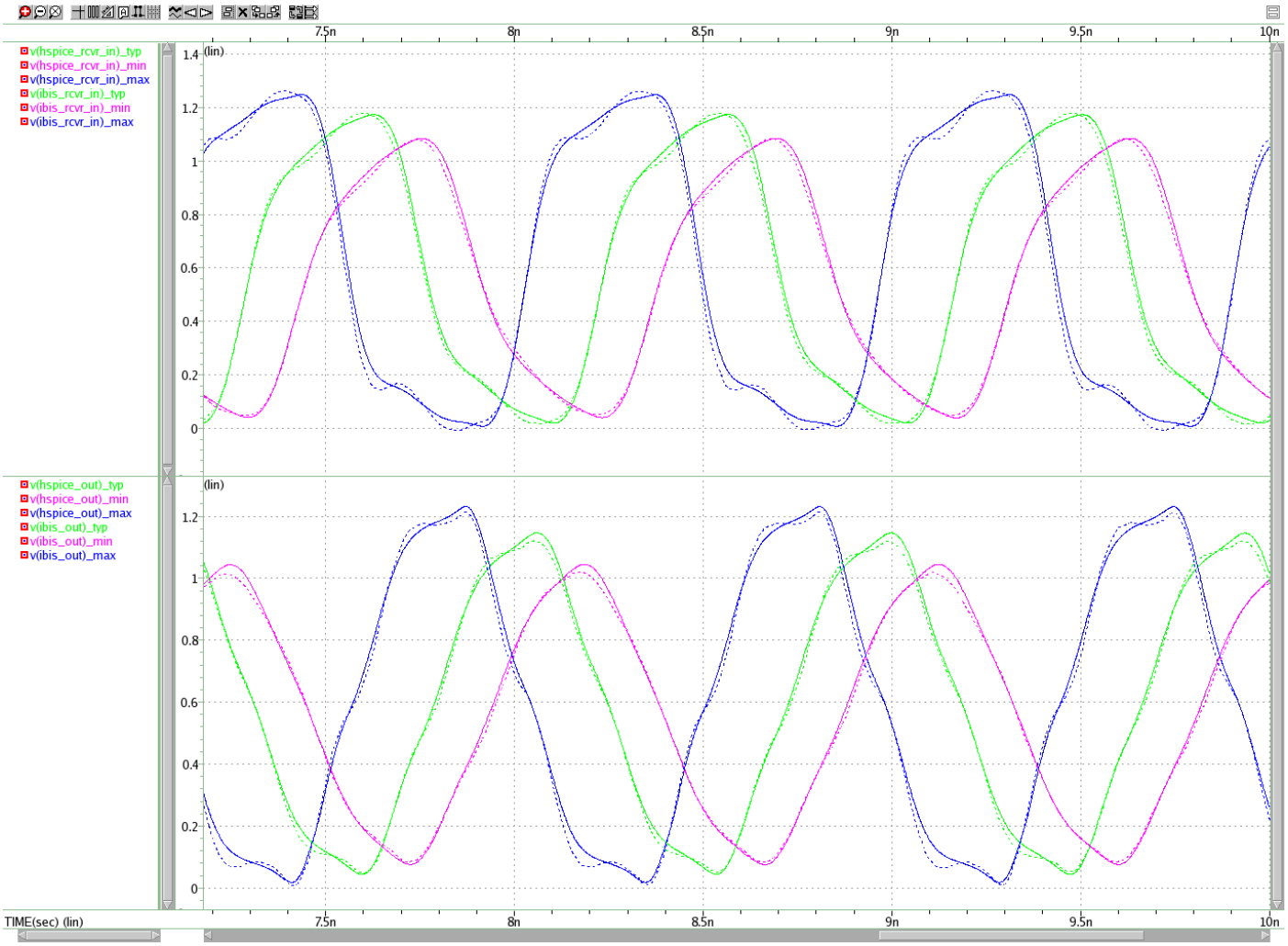
iv. **DQ_40_1866** driving **DQ_40_ODT120_1866**



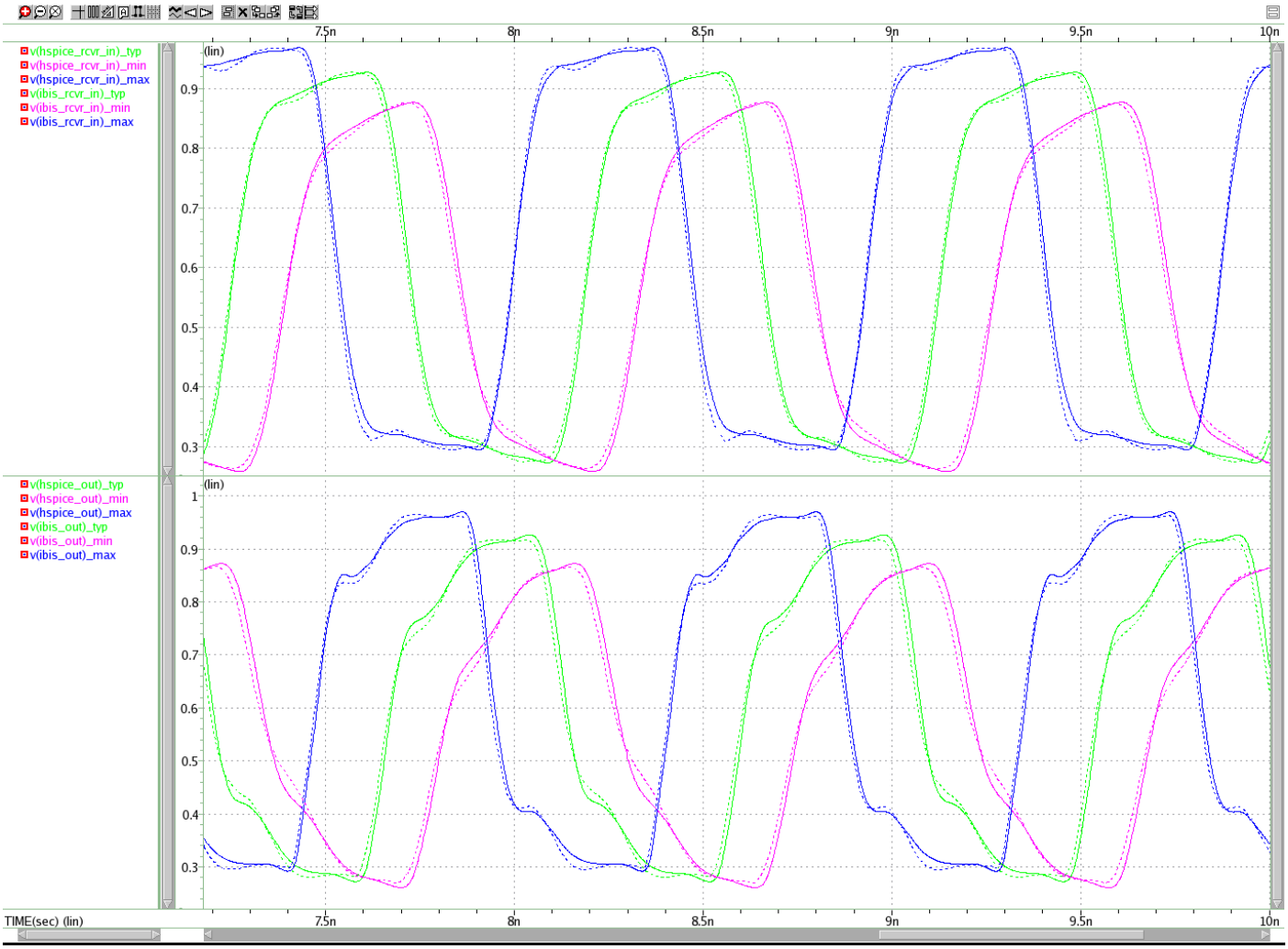
v. **DQ_60_1866** driving **DQ_60_ODT60_1866**



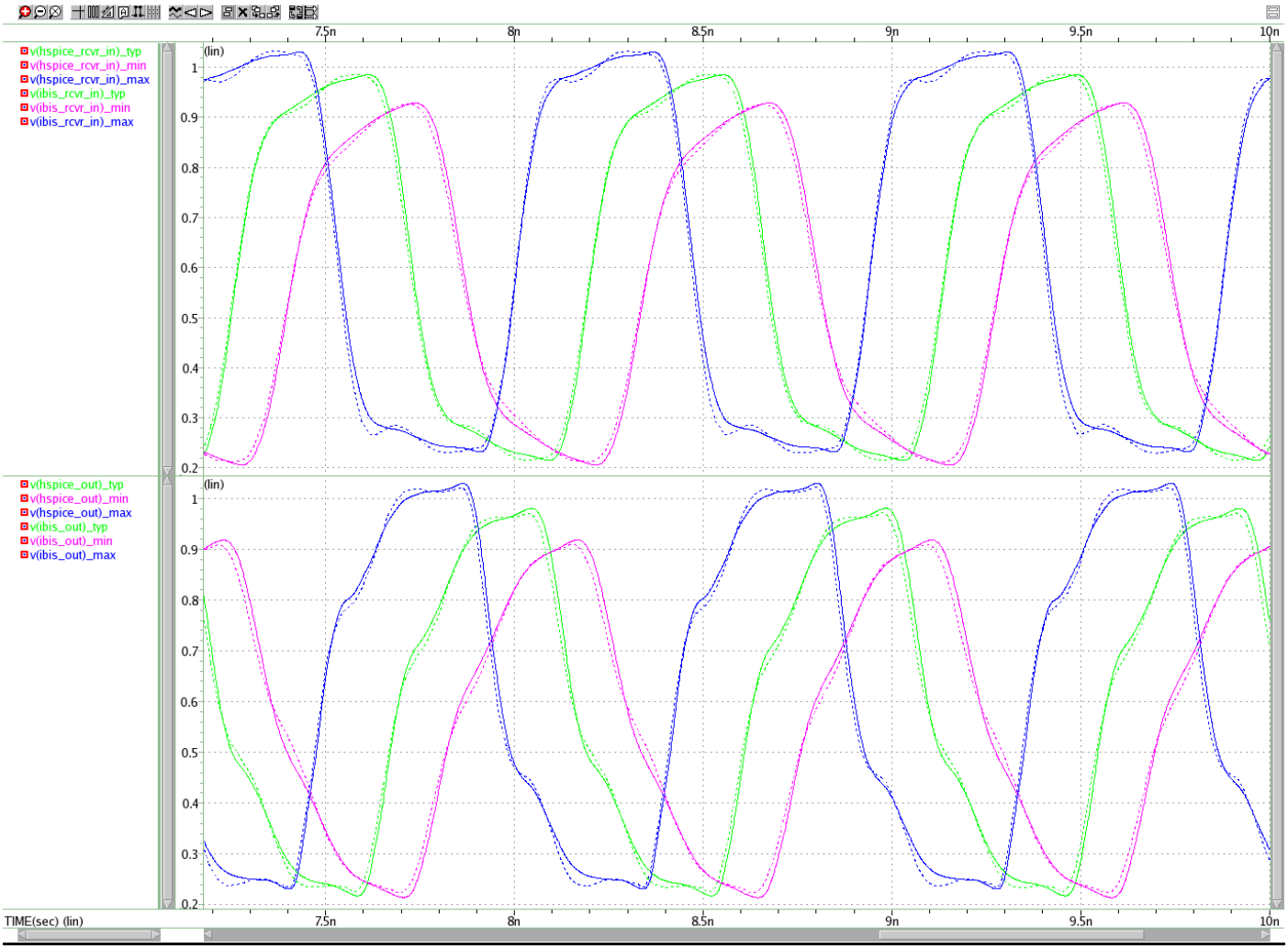
vi. **DQ_40_2133** driving **DQ_40_2133**



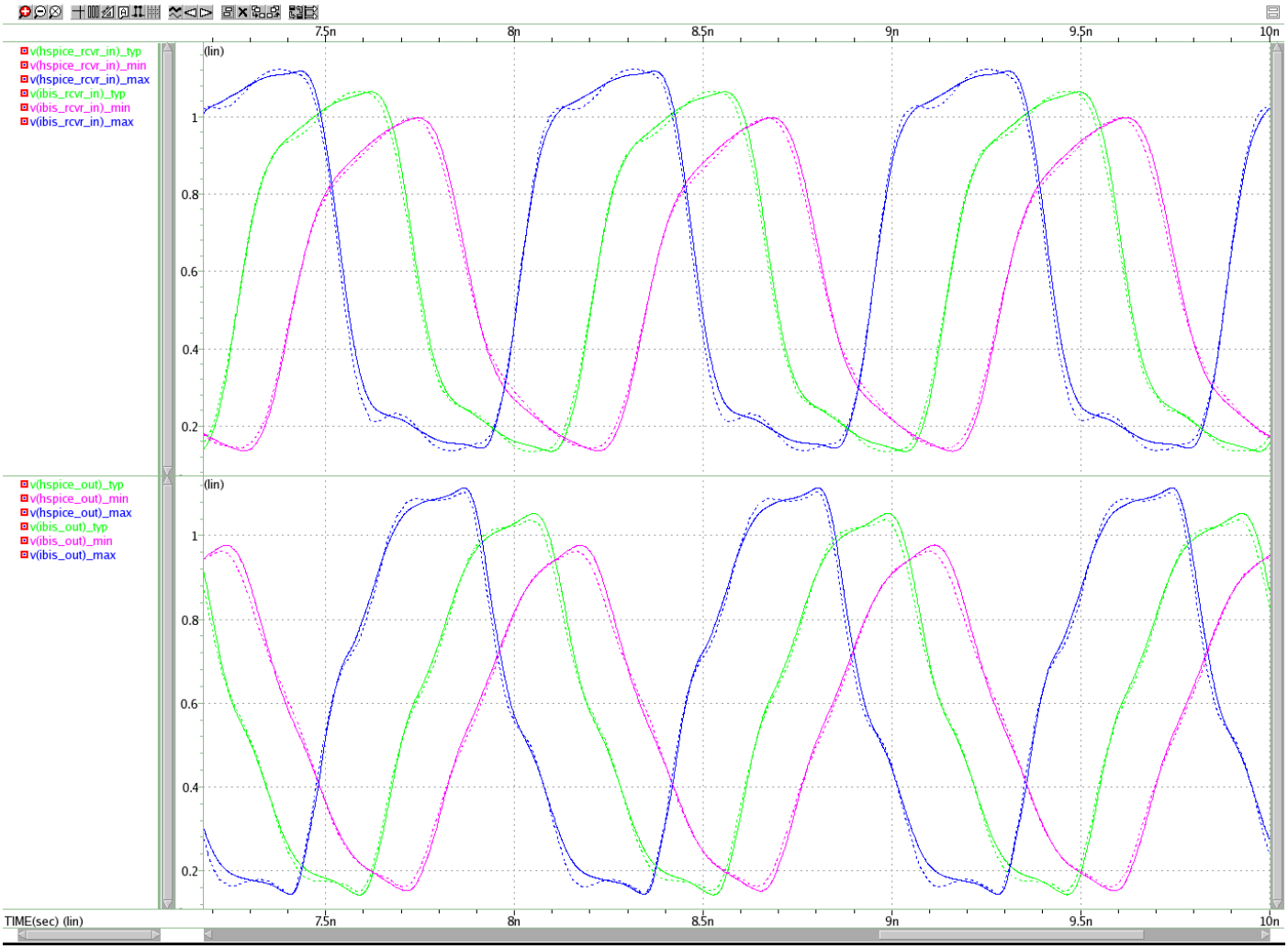
vii. **DQ_40_2133** driving **DQ_40_ODT40_2133**



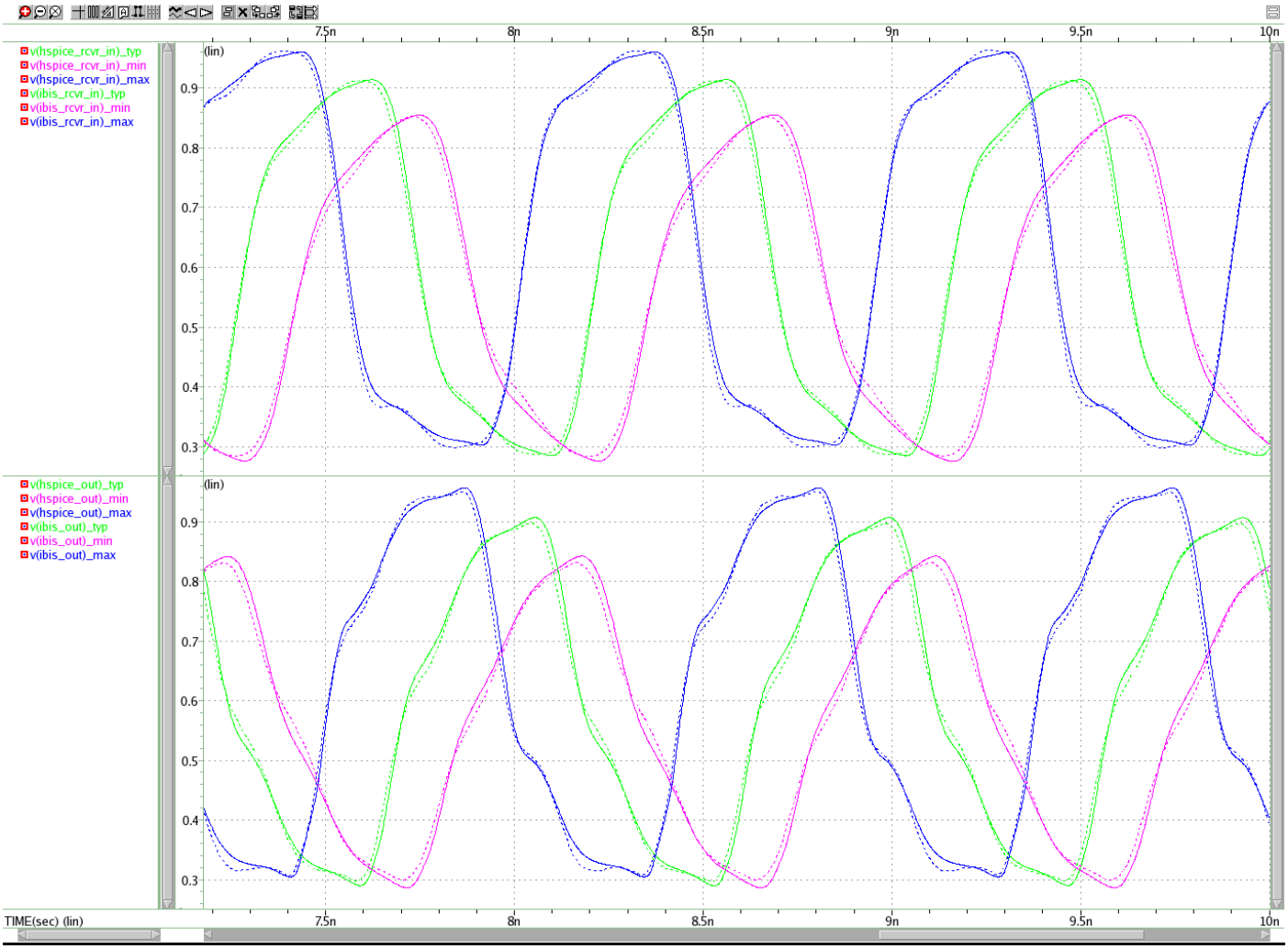
viii. **DQ_40_2133** driving **DQ_40_ODT60_2133**



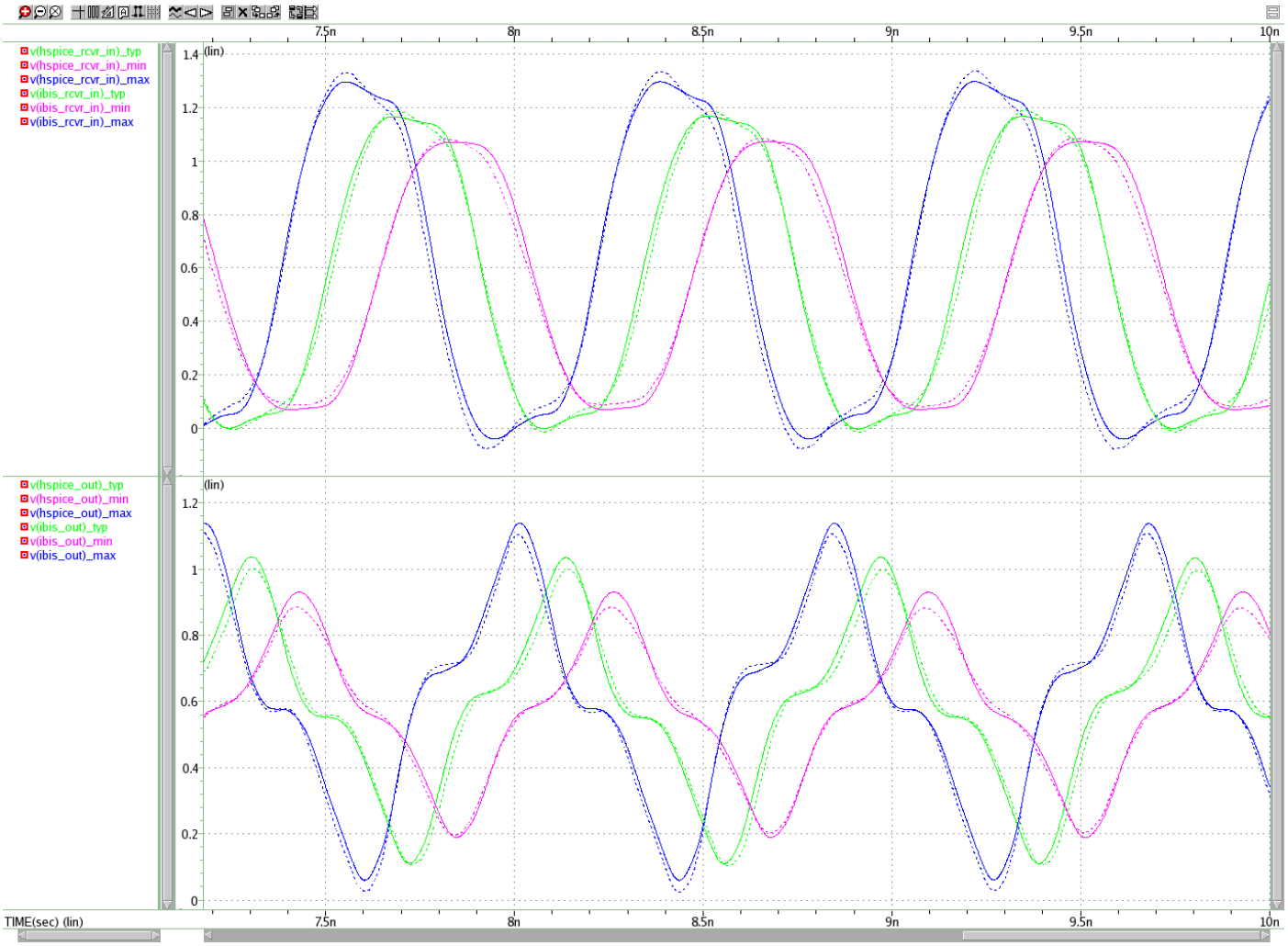
ix. **DQ_40_2133** driving **DQ_40_ODT120_2133**



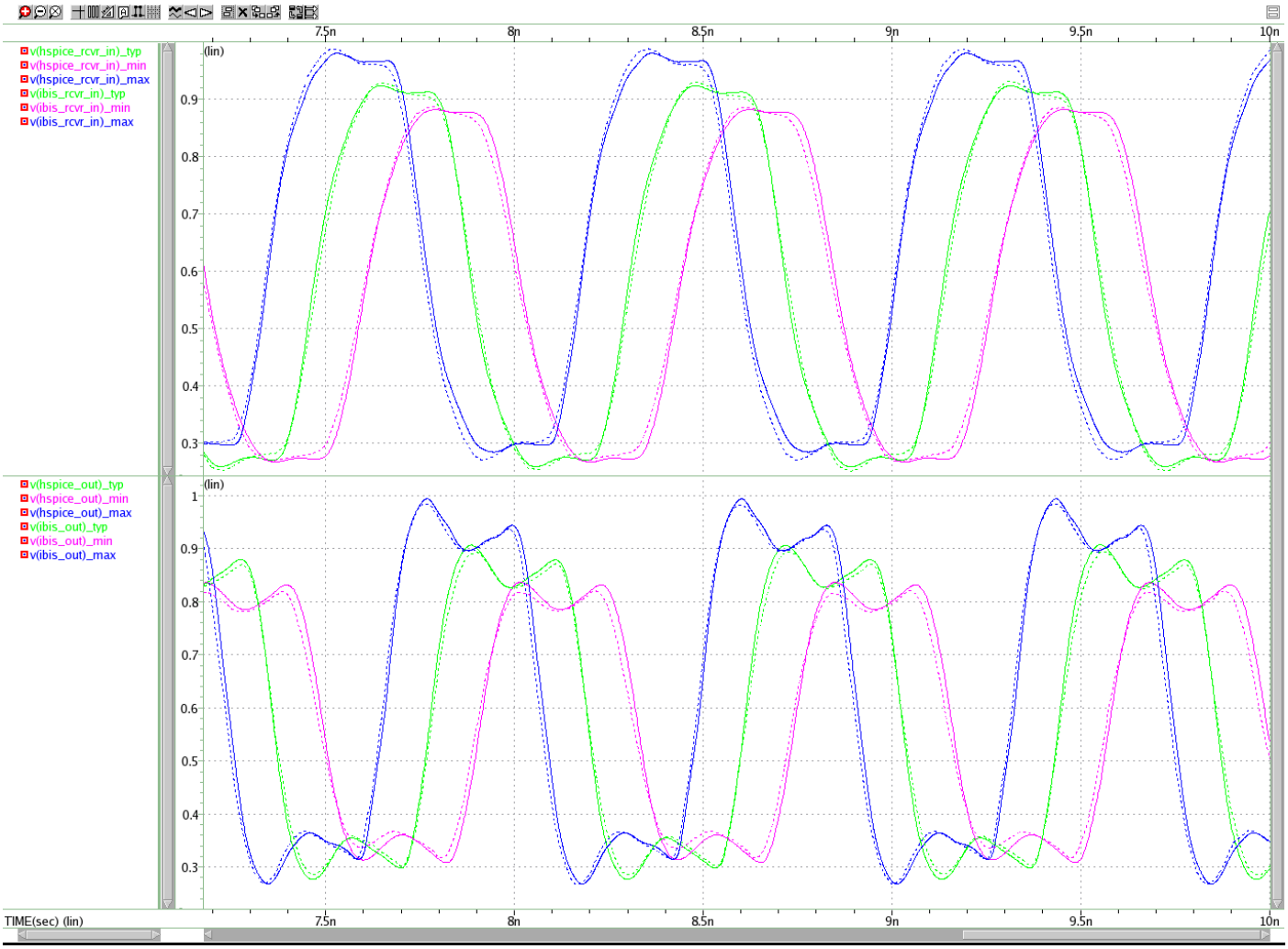
x. **DQ_60_2133** driving **DQ_60_ODT60_2133**



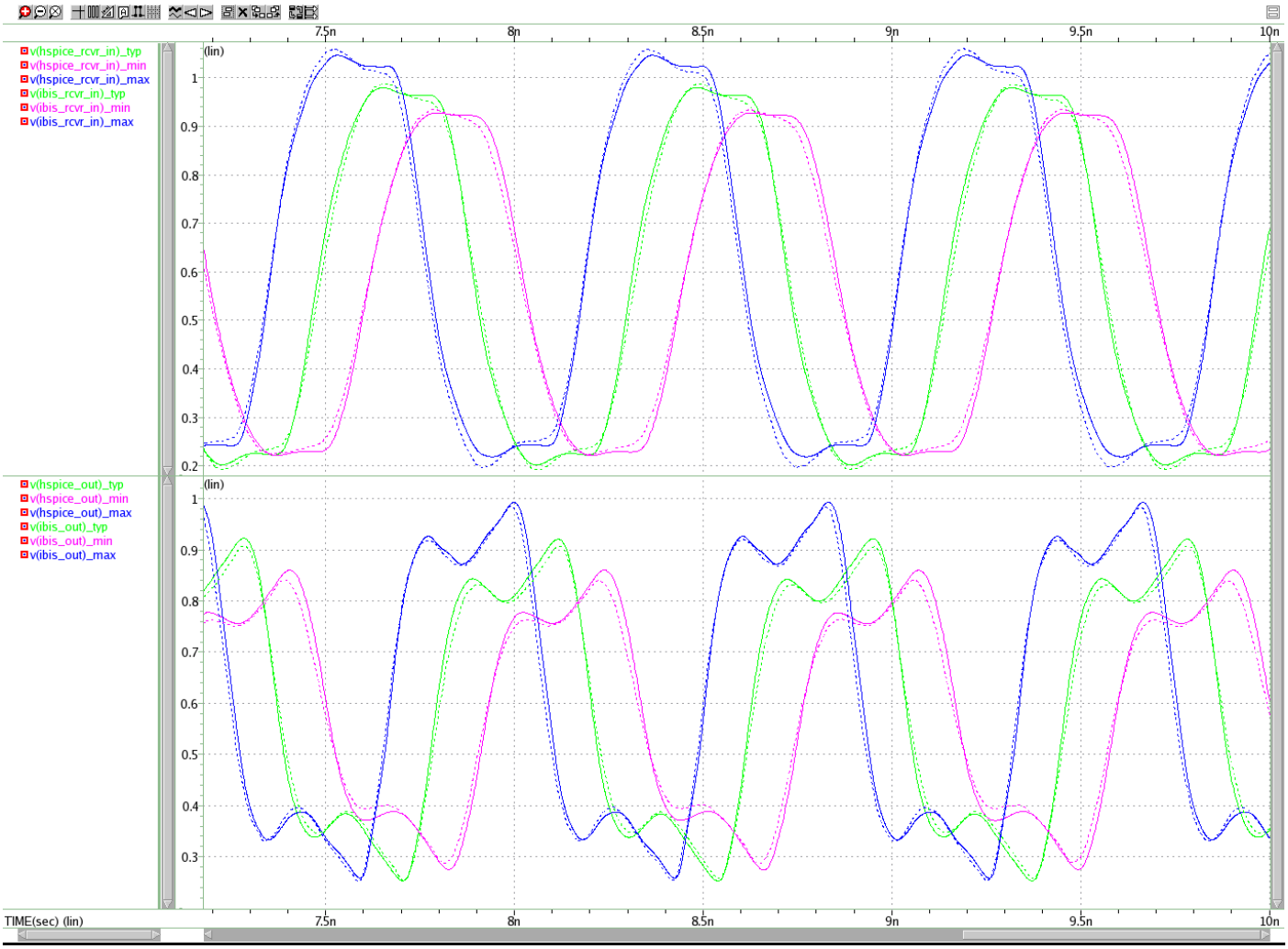
xi. **DQ_40_2400** driving **DQ_40_2400**



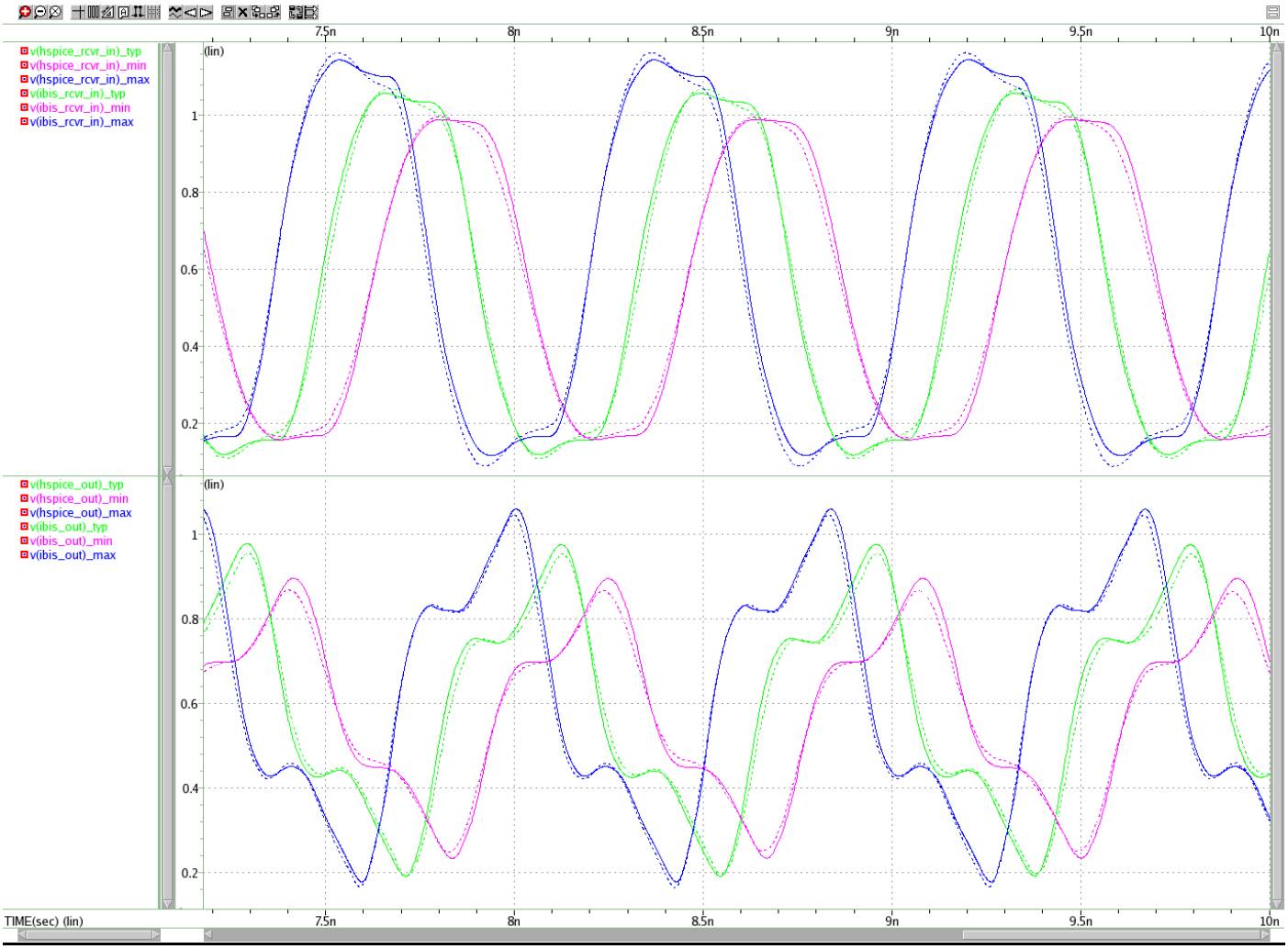
xii. **DQ_40_2400** driving **DQ_40_ODT40_2400**



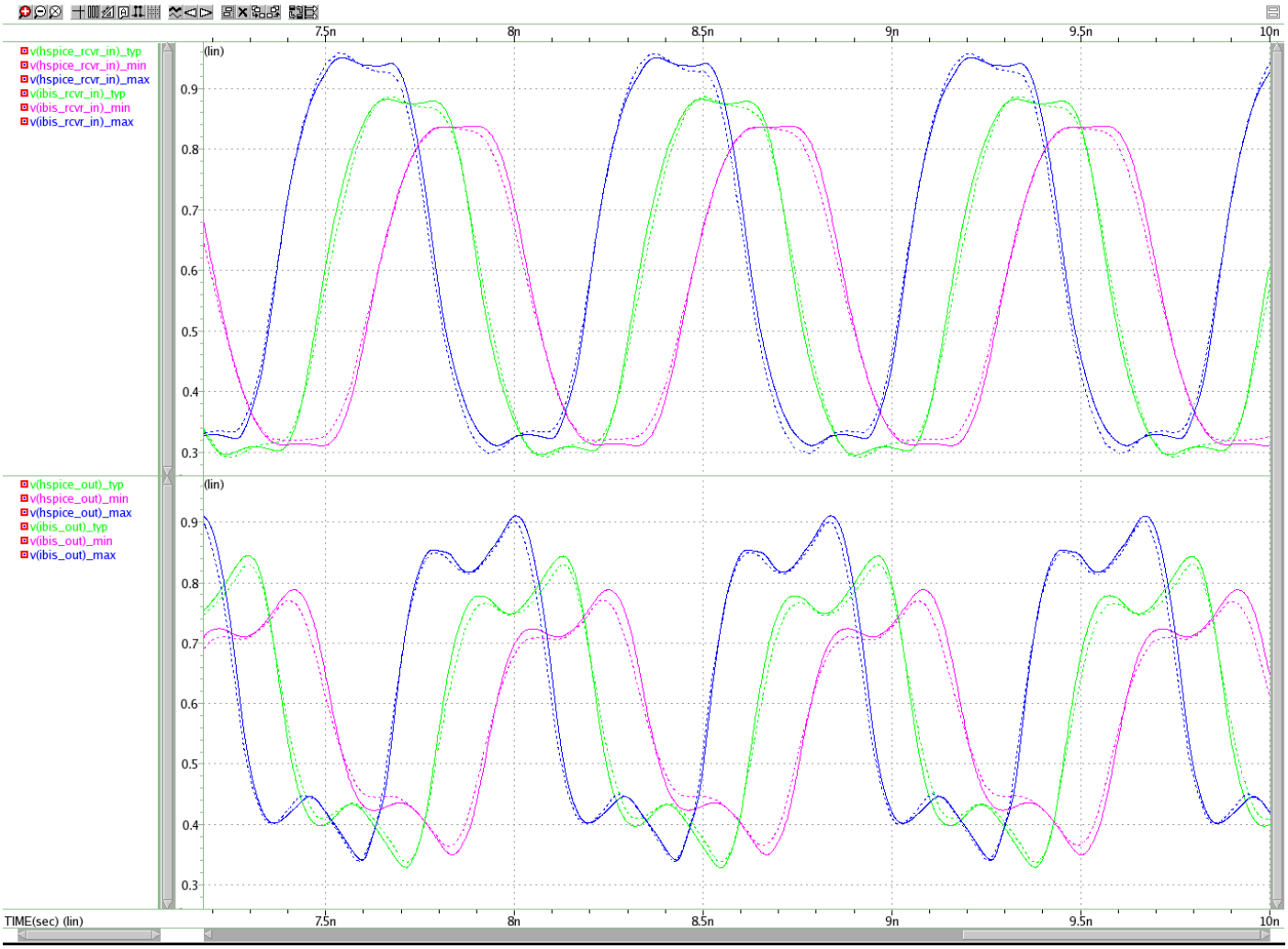
xiii. **DQ_40_2400** driving **DQ_40_ODT60_2400**



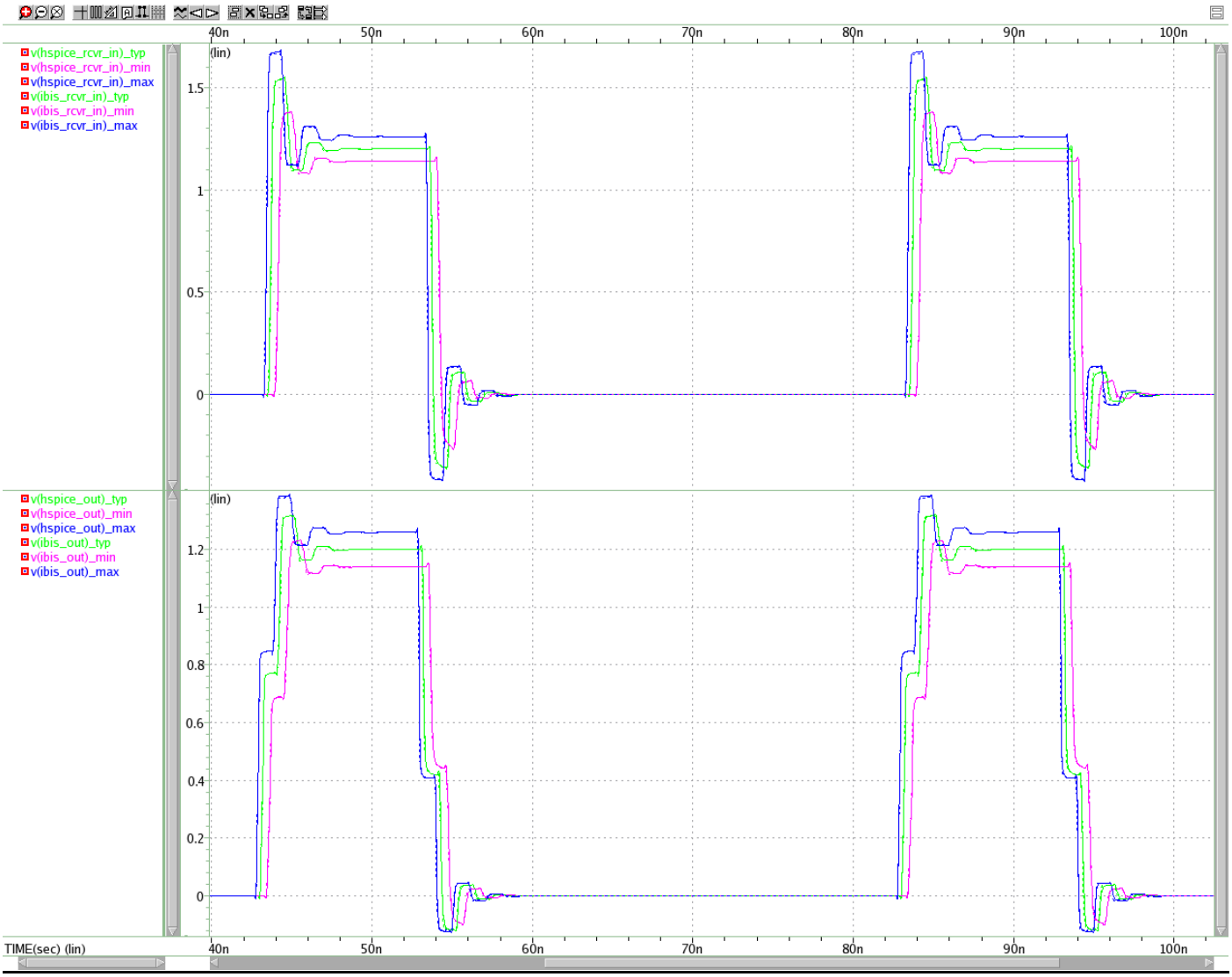
xiv. **DQ_40_2400** driving **DQ_40_ODT120_2400**



xv. **DQ_60_2400** driving **DQ_60_ODT60_2400**



xvi. **TDO_1866** driving **TDO_1866**



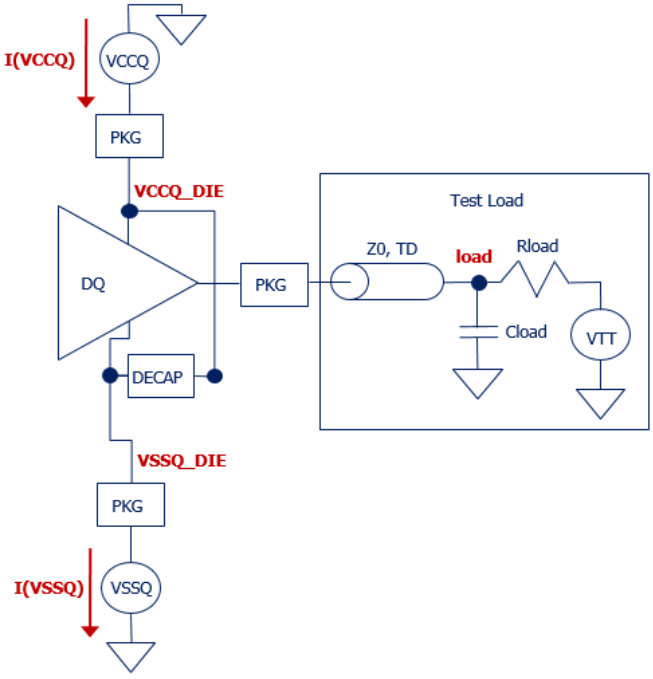
IBIS Model Correlation: IBIS vs Spice (IBIS 5.0)

1. ☒ For all Output or I/O IBIS Version 5.0 power-aware models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element) with a non-ideal power supply connection.

   a. ☒ Use the setup and node naming conventions shown in Setup B below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations: **HSPICE 2016.06**

   b. ☒ Run simulations for all corner cases and at fastest speed grades

SETUP B:



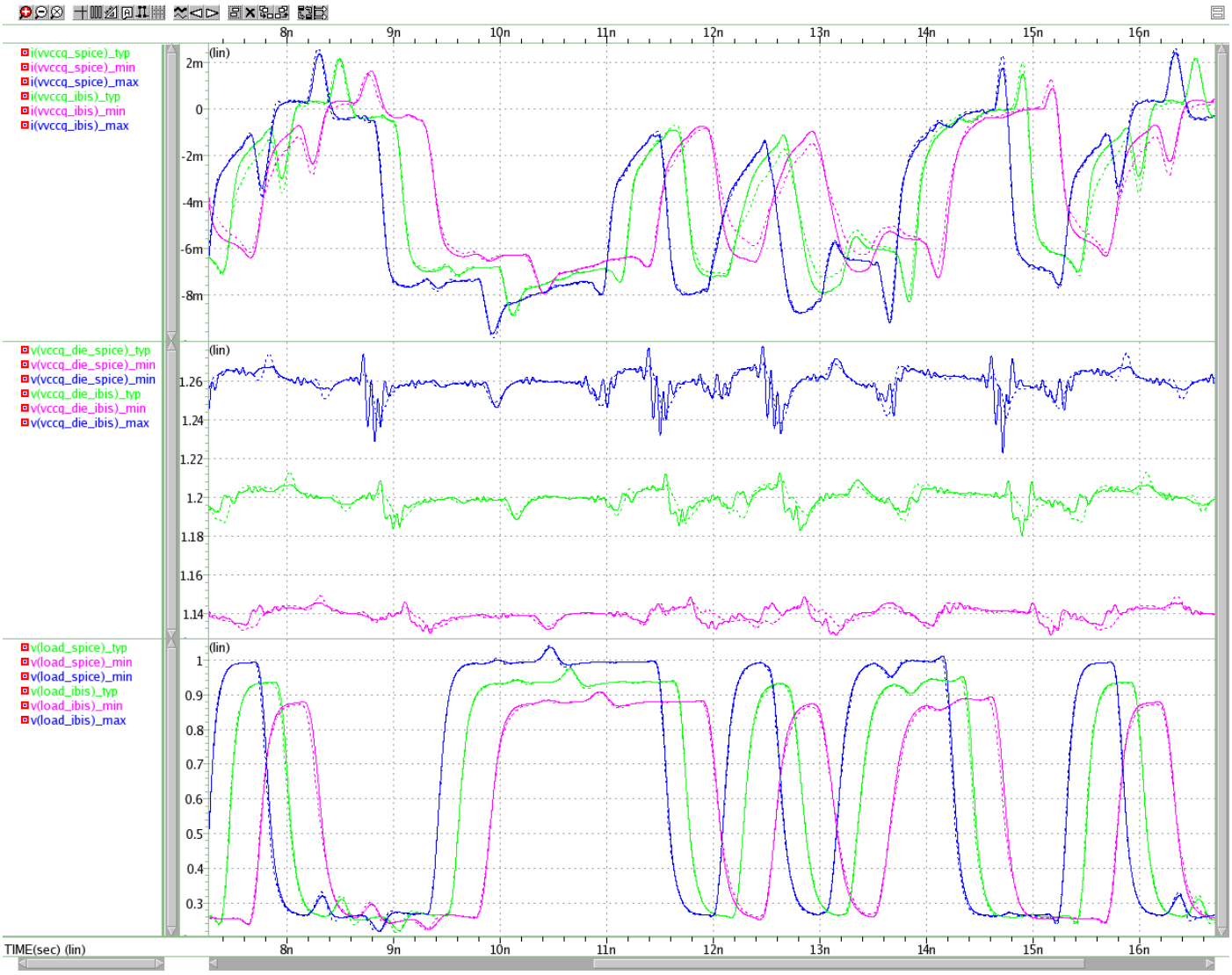
Test Load Values

Z0	=	50 Ω
Td	=	200 ps
Cload	=	5 pF
Rload	=	50 Ω
VTT	=	VDDQ/2

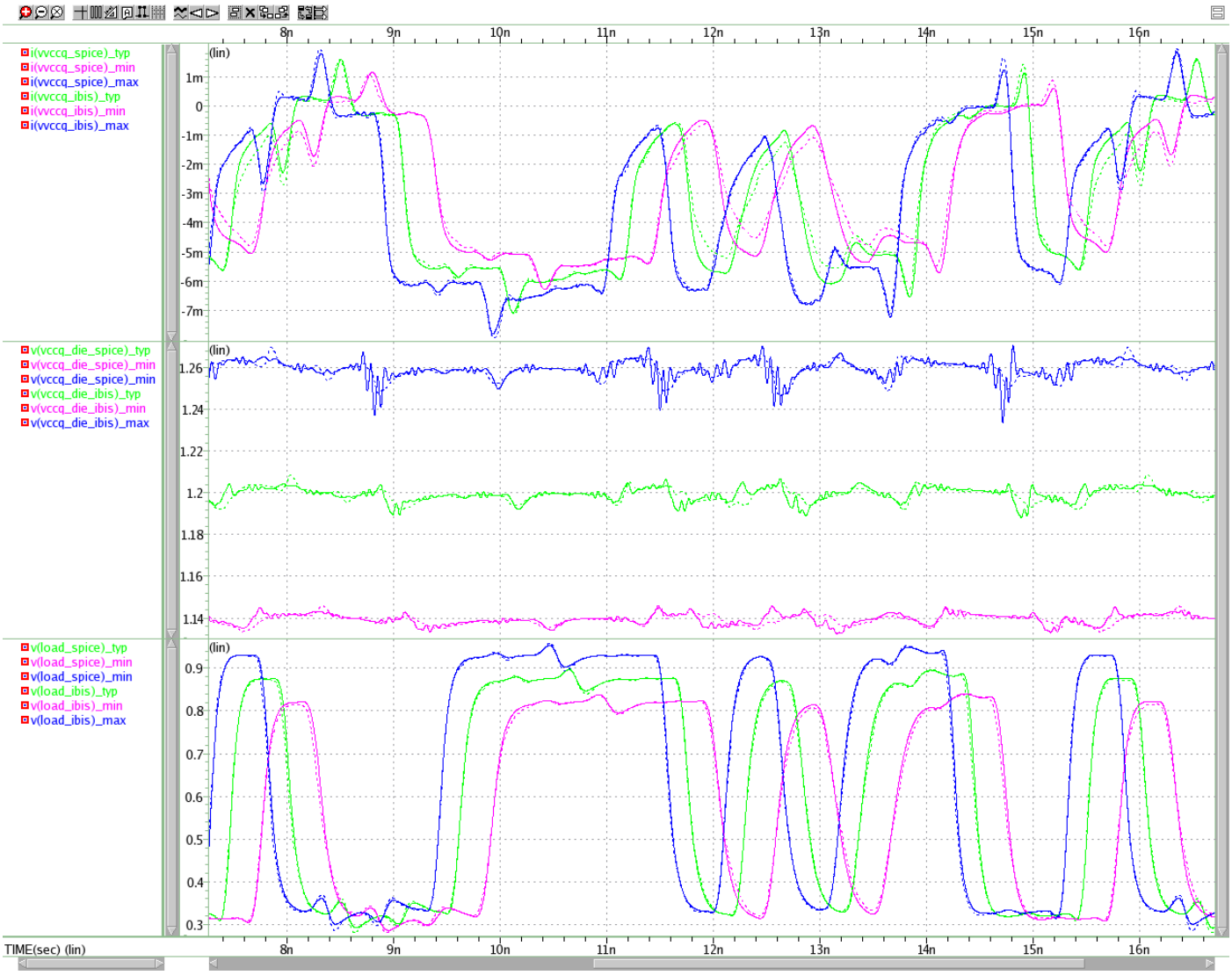
Package Model used for correlation

Lpkg	PAD	BALL	1.25n	0.25
Lpkg_vccq	vccq_die	vccq_ball	1.25n	0.25
Lpkg_vssq	vssq_die	vssq_ball	0.10n	0.05
K1	Lpkg_vccq	Lpkg_vssq	0.20	
K2	Lpkg	Lpkg_vccq	0.20	
K3	Lpkg	Lpkg_vssq	0.20	
Cpkg_vccq	BALL	vccq_ball	0.20p	
Cpkg_vssq	BALL	vssq_ball	0.20p	
Cpkg_vccq_vssq	vccq_ball	vssq_ball	0.40p	

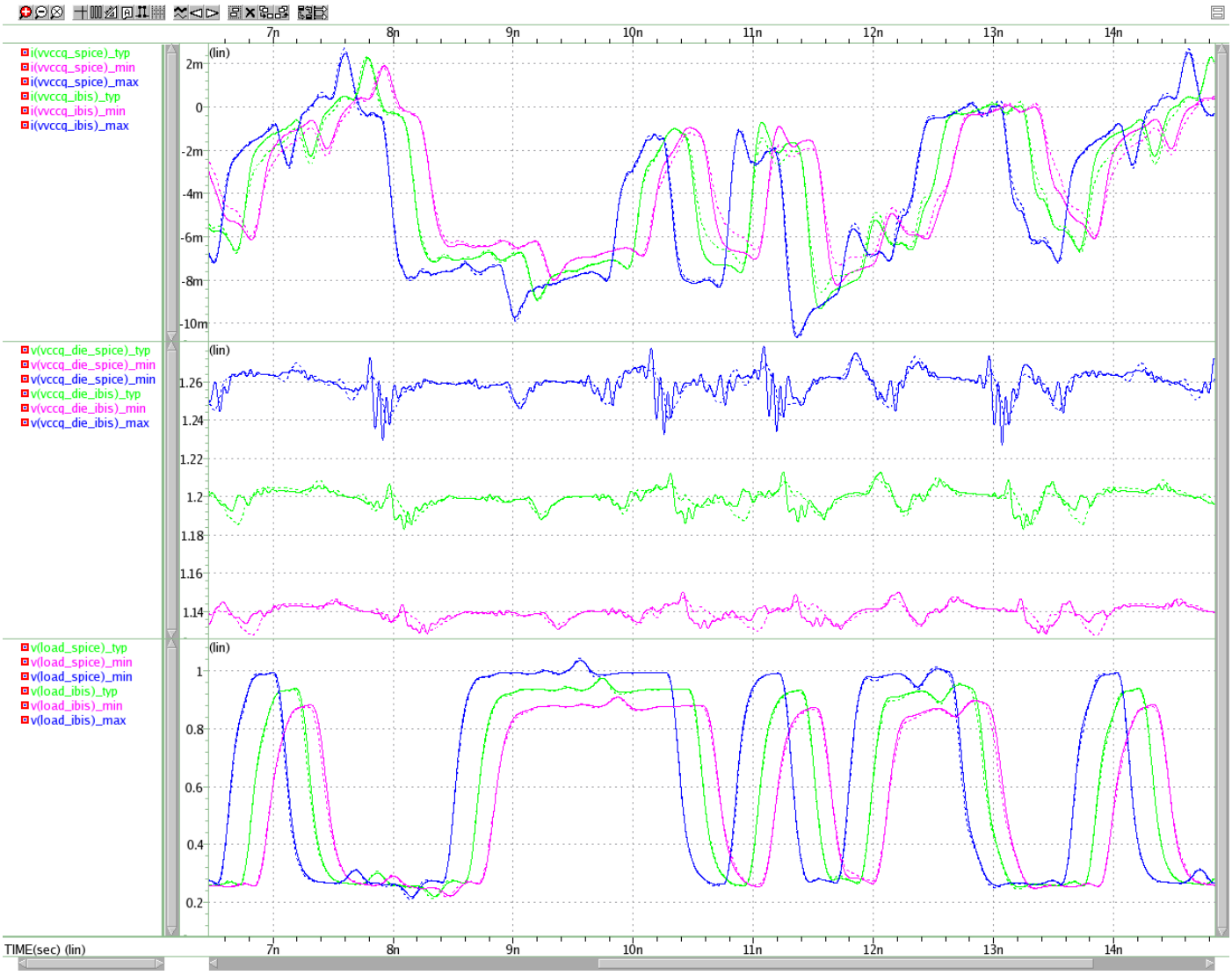
i. DQ_40_1866



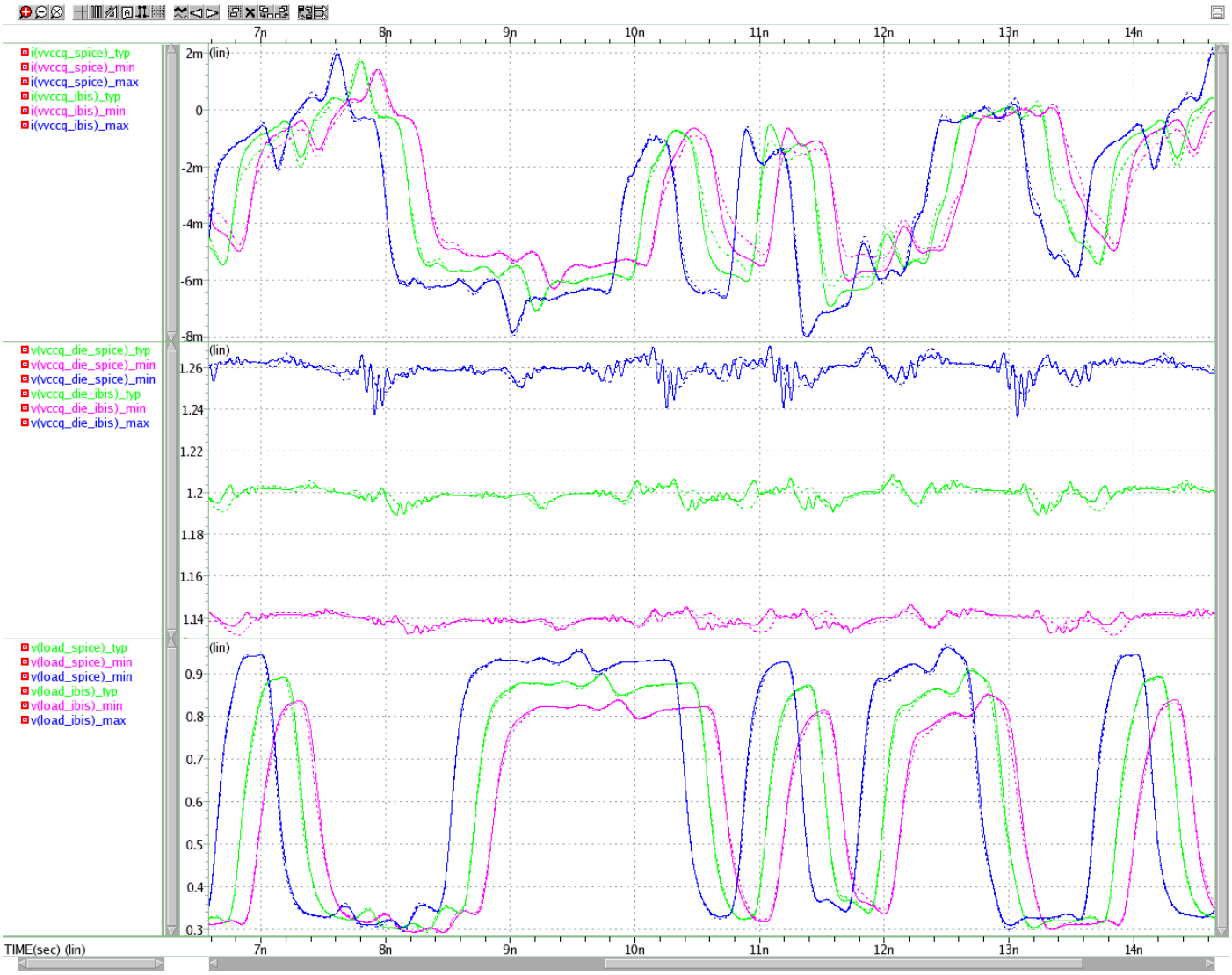
ii. **DQ_60_1866**



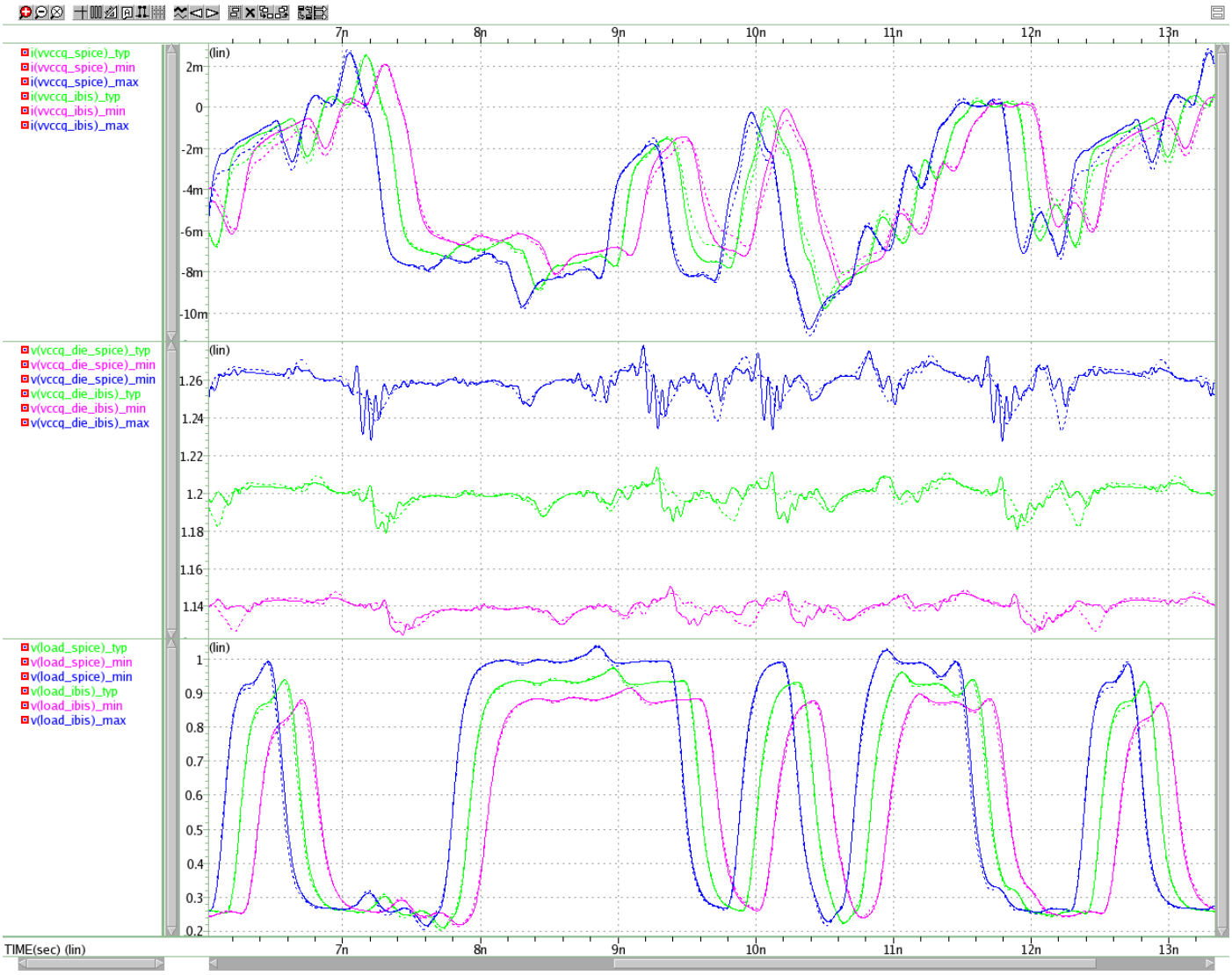
iii. **DQ_40_2133**



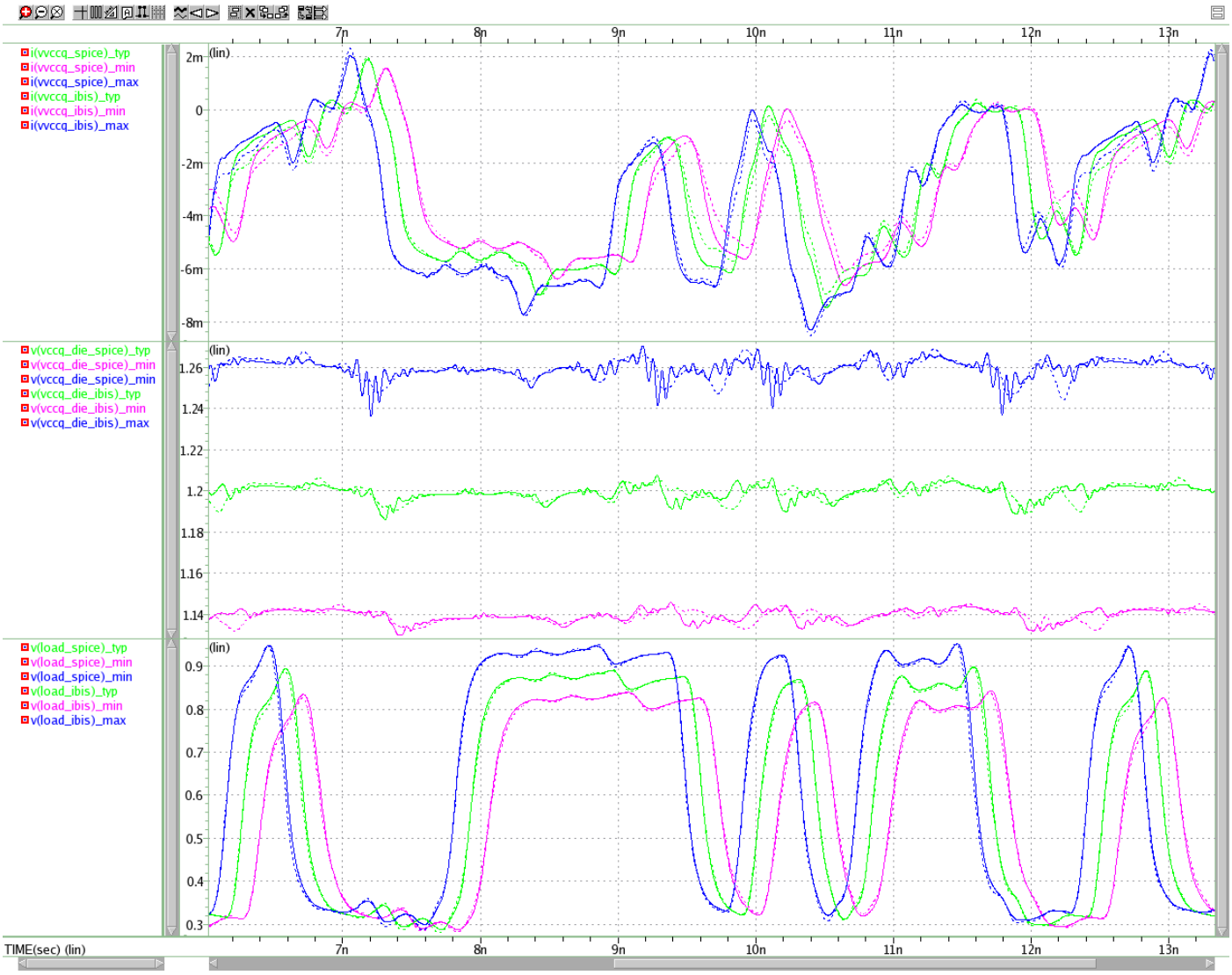
iv. **DQ_60_2133**



v. DQ_40_2400



vi. **DQ_60_2400**



Comments

1. **Model may not reflect speed grade availability.**
2. **C_comp is compared with the 2400 speed grade specification only.**
3. **Slew rate is based on HSPICE simulation with a 25ohm load to Vtt. This includes simple package parasitics for pin and power/gnd nets. The measurement comparison also includes probe and measurement fixture loading parasitics.**

Document Revision History

Rev **1.0** - Date **November 14, 2014**

a. IBIS revision **1.0**

b. HSPICE revision **1.0**

Rev **2.0** - Date **September 12, 2016**

a. IBIS revision **2.0**

b. HSPICE revision **2.0**

