IBIS/HSPICE Model Quality Report

Design ID: Y66A
Description: 256Mb - x8, x16 SDRAM
Marketing device name(s): MT48LC32M8A2P, MT48LC16M16A2P, MT48LC32M8A2BB, MT48LC16M16A2B4, MT48LC32M8A2Y66A, MT48LC16M16A2Y66A
Valid speed grades: SDRAM-100, 133, 143, 167 MHz
Zip filename: y66a_ibis.zip
IBIS filename: y66a.ibs, y66a_at.ibs, y66a_it.ibs **File rev:** 2.1
HSpice filename: y66a_hspice.zip **File rev:** 2.0
EBD filename (if applicable): N/A **File rev:** N/A
Die rev: G
Date: September 3, 2019
Datasheet Link (from micron.com): go to https://www.micron.com and search for y66a

For support contact your local Micron FAE/Sales contacts
(more information at https://www.micron.com/support/sales-network).

Device Parameters

VDDQ – Slow: 3.0 **Typical:** 3.3 **Fast:** 3.6
VDD – Slow: 3.0 **Typical:** 3.3 **Fast:** 3.6
Junction Temperature (Commercial) - Slow: 85C **Typical:** 50C **Fast:** 0C
Junction Temperature (Industrial) - Slow: 95C **Typical:** 50C **Fast:** -40C
Junction Temperature (Automotive) - Slow: 110C **Typical:** 50C **Fast:** -40C
VDDQ/VSSQ Decoupling Capacitance: 3.571nF
Included in HSPICE DQ/DQS models? YES **Amount per DQ/DQS model:** 111.59pF
VDDQ/VSSQ Decoupling Capacitance Series Resistance: 11.77 Ohms

IBIS Quality Summary

1. ☒ Include the IBIS Quality Specification 2.0 Overall IBIS Quality level. For details on IBIS Quality, reference the quality specification and quality checklist on IBIS quality webpage http://www.eda.org/pub/ibis/quality_wip/.

   Overall IBIS Quality Level: 3MS
   Exceptions: 0

2. ☒ Include the filename of the IBIS Quality Checklist that accompanies this report.

   Filename: y66a_ibis_quality_2.1_checklist.xls

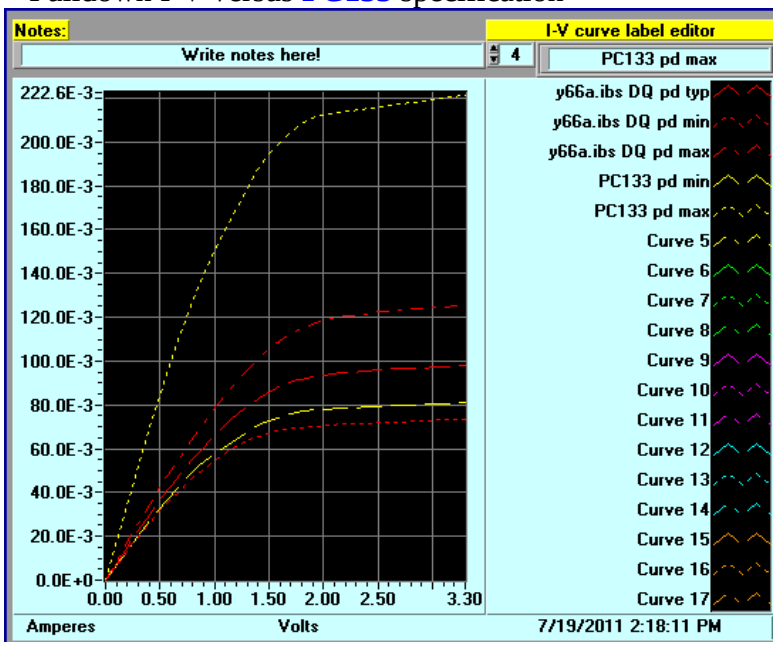
IBIS MODEL Correlation

Datasheet Correlation

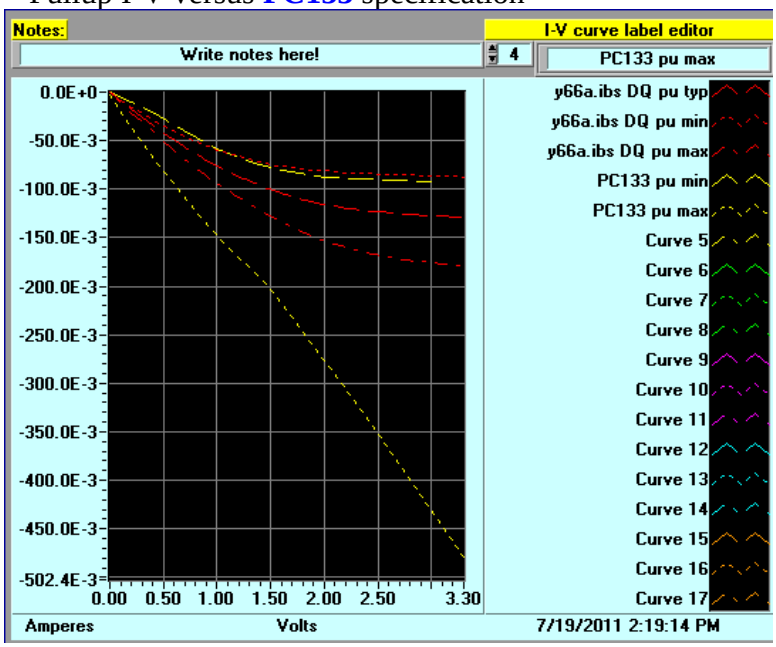
1. ☒ For Output or I/O model compare datasheet IOH/IOL data with IBIS pullup/pulldown data. [1]

   a. Model name: **DQ**

      i. Pulldown I-V versus **PC133** specification



      ii. Pullup I-V versus **PC133** specification



2. ☒ Compare C_comp with datasheet Input C. Provide C_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16).

Component name: **MT48LC32M8A2BB (60-ball FBGA)**

		IBIS		Datasheet	
		min	max	min	max
DQ	C_comp	3.72	4.02	NA	NA
	C package	0.72	1.26	NA	NA
	C_total	4.44	5.28	3.00	6.00
INPUT	C_comp	2.15	2.35	NA	NA
	C package	0.67	1.08	NA	NA
	C_total	2.82	3.43	1.50	3.80
CLK	C_comp	2.23	2.43	NA	NA
	C package	0.83	0.83	NA	NA
	C_total	3.06	3.26	1.50	3.50
DM	C_comp	2.58	2.78	NA	NA
	C package	0.72	0.72	NA	NA
	C_total	3.29	3.49	1.50	3.80

Component name: **MT48LC16M16A2B4 (54-ball VFBGA)**

		IBIS		Datasheet	
		min	max	min	max
DQ	C_comp	3.72	4.02	NA	NA
	C package	0.63	1.09	NA	NA
	C_total	4.35	5.12	3.00	6.00
INPUT	C_comp	2.15	2.35	NA	NA
	C package	0.65	1.01	NA	NA
	C_total	2.80	3.35	1.50	3.80
CLK	C_comp	2.23	2.43	NA	NA
	C package	0.74	0.74	NA	NA
	C_total	2.97	3.17	1.50	3.50
DM	C_comp	2.58	2.78	NA	NA
	C package	0.68	0.91	NA	NA
	C_total	3.25	3.69	1.50	3.80

Component name: **MT48LC32M8A2P (54-pin TSOP)**

		IBIS		Datasheet	
		min	max	min	max
DQ	C_comp	3.72	4.02	NA	NA
	C package	0.41	0.78	NA	NA
	C_total	4.13	4.80	4.00	6.00
INPUT	C_comp	2.15	2.35	NA	NA
	C package	0.63	0.94	NA	NA
	C_total	2.78	3.29	2.50	3.80
CLK	C_comp	2.23	2.43	NA	NA
	C package	0.68	0.68	NA	NA
	C_total	2.91	3.11	2.50	3.50
DM	C_comp	2.58	2.78	NA	NA
	C package	0.63	0.63	NA	NA
	C_total	3.21	3.41	2.50	3.80

Component name: **MT48LC16M16A2P (54-pin TSOP)**

		IBIS		Datasheet	
		min	max	min	max
DQ	C_comp	3.72	4.02	NA	NA
	C package	0.41	0.78	NA	NA
	C_total	4.13	4.80	4.00	6.00
INPUT	C_comp	2.15	2.35	NA	NA
	C package	0.63	0.94	NA	NA
	C_total	2.78	3.29	2.50	3.80
CLK	C_comp	2.23	2.43	NA	NA
	C package	0.68	0.68	NA	NA
	C_total	2.91	3.11	2.50	3.50
DM	C_comp	2.58	2.78	NA	NA
	C package	0.58	0.63	NA	NA
	C_total	3.15	3.41	2.50	3.80

3. ☐ If slew rate specifications (rise/fall slew) are available from the datasheet, complete HSpice simulations to generate slew rate data and provide a comparison table.

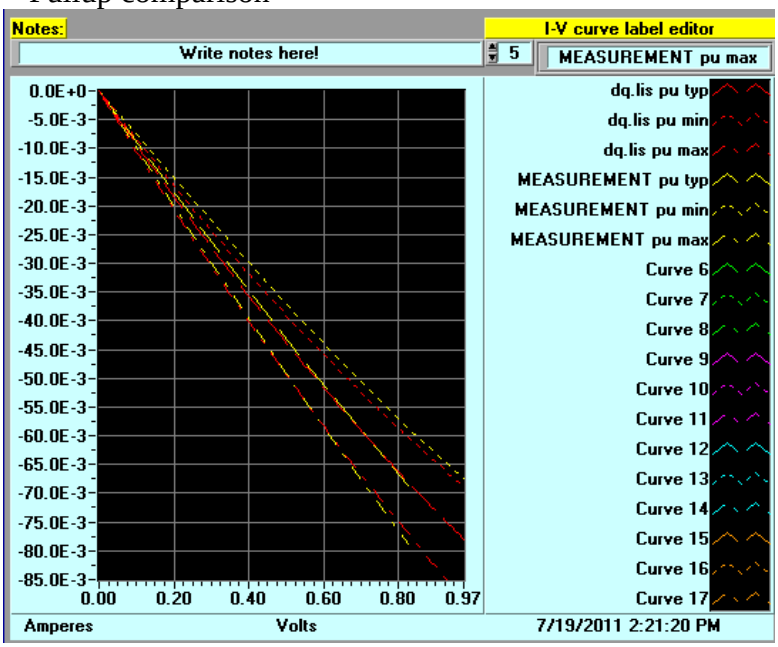
Not Available

4. ☐ Compare ODT data with datasheet.

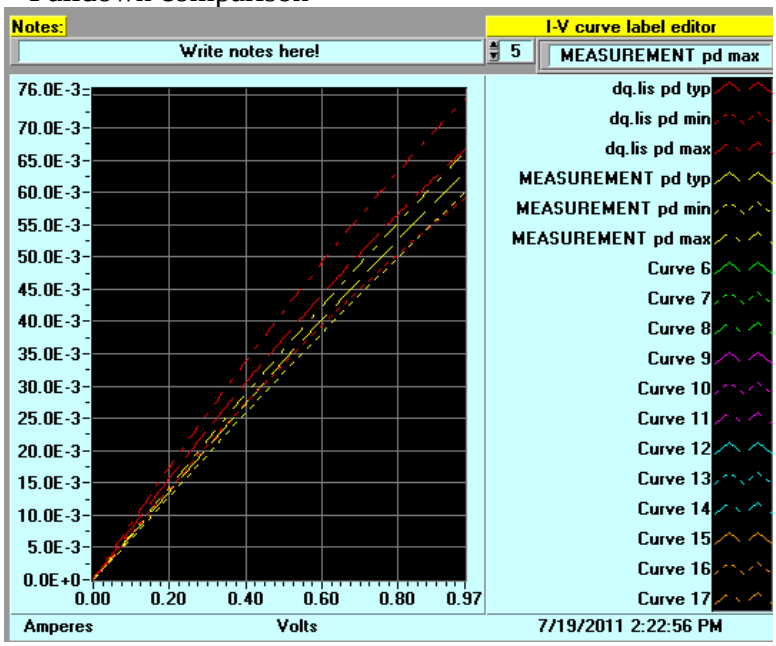
Not Applicable

Measurement Correlation

1. ☒ For Output or I/O models compare measured IOH/IOL data with IBIS pullup/pulldown data. If the measurement conditions are different than the IBIS conditions, run HSpice simulations using the same measurement conditions such as VCC, temperature, and process. Include measurement conditions in the pullup/pulldown images.[2]
    a. Model name: **DQ (measurement range 0-0.975V)**
        i. Pullup comparison



        ii. Pulldown comparison



2. ☒ Compare C_comp with measured C_comp. Provide C_comp comparison table for all models and for all package combinations (i.e x4, x8 and x16).

Component name: **MT48LC32M8A2BB (60-ball FBGA)**

		IBIS			Measured		
		min	typ	max	min	typ	max
DQ	C_comp	3.72	3.87	4.02	NA	NA	NA
	C package	0.72	1.06	1.26	NA	NA	NA
	C_total	4.44	4.93	5.28	4.55	4.93	5.40
INPUT	C_comp	2.15	2.25	2.35	NA	NA	NA
	C package	0.67	0.93	1.08	NA	NA	NA
	C_total	2.82	3.17	3.43	2.75	3.17	3.43
CLK	C_comp	2.23	2.33	2.43	NA	NA	NA
	C package	0.83	0.83	0.83	NA	NA	NA
	C_total	3.06	3.16	3.26	3.09	3.16	3.20
DM	C_comp	2.58	2.68	2.78	NA	NA	NA
	C package	0.72	0.72	0.72	NA	NA	NA
	C_total	3.29	3.39	3.49	3.34	3.39	3.43

Component name: **MT48LC16M16A2B4 (54-ball VFBGA)**

		IBIS			Measured		
		min	typ	max	min	typ	max
DQ	C_comp	3.72	3.87	4.02	NA	NA	NA
	C package	0.63	0.87	1.09	NA	NA	NA
	C_total	4.35	4.74	5.12	4.30	4.76	5.14
INPUT	C_comp	2.15	2.25	2.35	NA	NA	NA
	C package	0.65	0.80	1.01	NA	NA	NA
	C_total	2.80	3.04	3.35	2.82	3.02	3.31
CLK	C_comp	2.23	2.33	2.43	NA	NA	NA
	C package	0.74	0.74	0.74	NA	NA	NA
	C_total	2.97	3.07	3.17	2.93	2.98	3.01
DM	C_comp	2.58	2.68	2.78	NA	NA	NA
	C package	0.68	0.80	0.91	NA	NA	NA
	C_total	3.25	3.47	3.69	3.29	3.47	3.62

Component name: **MT48LC16M16A2P (54-pin TSOP)**

		IBIS			Measured		
		min	typ	max	min	typ	max
DQ	C_comp	3.72	3.87	4.02	NA	NA	NA
	C package	0.41	0.59	0.78	NA	NA	NA
	C_total	4.13	4.46	4.80	4.15	4.47	4.99
INPUT	C_comp	2.15	2.25	2.35	NA	NA	NA
	C package	0.63	0.79	0.94	NA	NA	NA
	C_total	2.78	3.03	3.29	2.60	3.11	3.43
CLK	C_comp	2.23	2.33	2.43	NA	NA	NA
	C package	0.68	0.68	0.68	NA	NA	NA
	C_total	2.91	3.01	3.11	2.78	2.90	3.01
DM	C_comp	2.58	2.68	2.78	NA	NA	NA
	C package	0.58	0.61	0.63	NA	NA	NA
	C_total	3.15	3.28	3.41	3.04	3.20	3.33

3. ☐ If measured clamp current data is available provide an IBIS and measurement comparison for all models.

Not Available

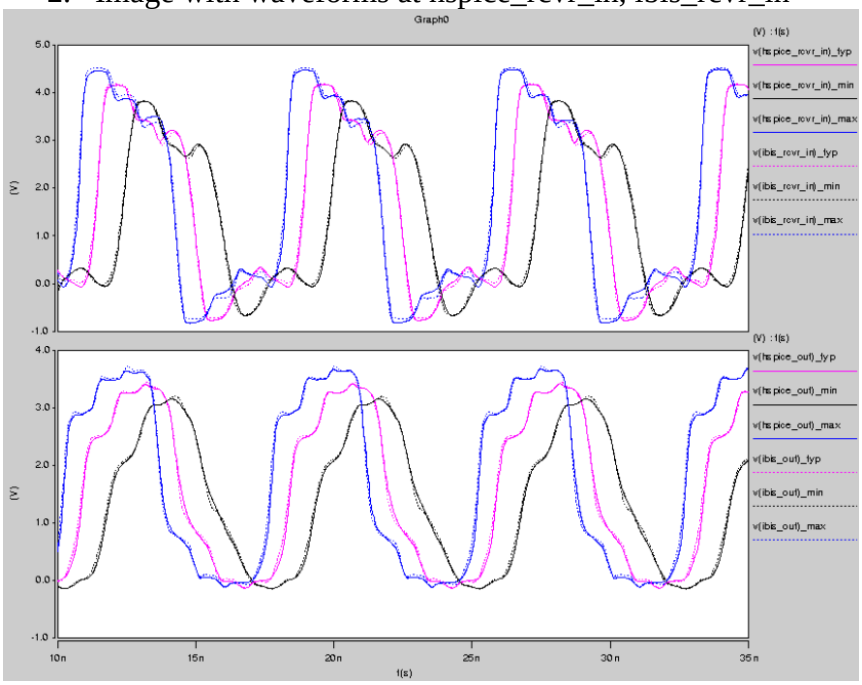
4. ☐ If slew rate data (rise/fall slew) is available from measurements, complete HSpice simulations to generate slew rate data and provide a comparison table.

Not Available

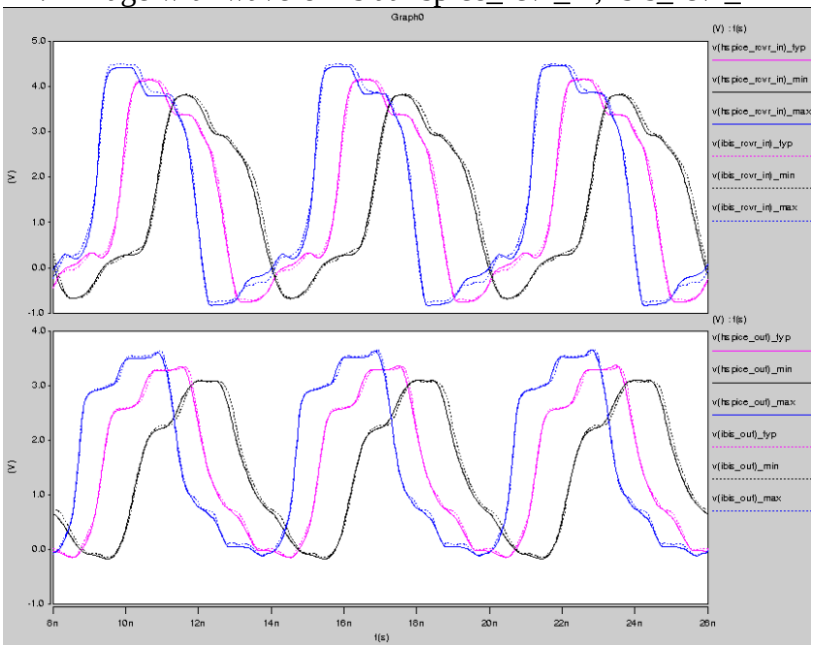
IBIS vs HSPICE Correlation

1. ☒ For all Output or I/O models, run HSpice transient simulations using encrypted netlists and the IBIS model (b-element).
   a. ☒ Use the setup and node naming conventions shown below for the IBIS and HSpice deck file (.sp file). Update the setup diagram if it is different. Indicate the version of HSPICE simulator used for simulations: **2008.09**
   b. ☒ Run simulations for all corners cases and at maximum allowable speed grade

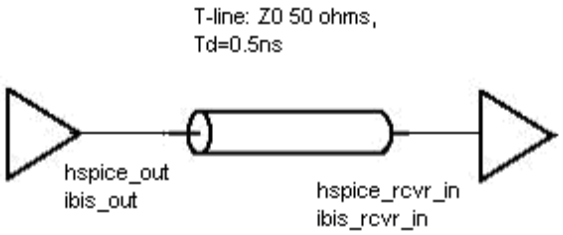
i. DQ driving DQ at 133MHz
   1. Image with waveforms at hspice_out, ibis_out
   2. Image with waveforms at hspice_rcvr_in, ibis_rcvr_in



ii. DQ driving DQ at 167MHz
   1. Image with waveforms at hspice_out, ibis_out
   2. Image with waveforms at hspice_rcvr_in, ibis_rcvr_in



Setup



Comments:

Document Revision History

Rev **1.0** - Date **12/13/2010**
- a. IBIS revision **1.0**
- b. HSpice revision **1.0**

Rev **2.0** - Date **07/19/2011**
- a. IBIS revision **2.0**
- b. HSpice revision **2.0**

Rev **2.1** - Date **09/03/2019**
- a. IBIS revision **2.1**
- b. HSpice revision **2.0**