

## IBIS/HSPICE Model Quality Report

**Design ID- Y14W**

**Description-64Mb x4, x8, x16, x32 SDRAM**

**Marketing device name(s): MT48LC16M4A2TG, MT48LC8M8A2TG, MT48LC4M16A2TG, MT48LC4M16A2F4, MT48LC2M32B2TG, MT48LC2M32B2B5**

**Zip File Name: y14w\_ibis.zip, y14w\_x32\_ibis.zip, y14w\_spice.zip, y14w\_x32\_spice.zip**

**IBIS File name: y14w.ibs, y14w\_x32.ibs File rev: 2.2, 2.3**

**HSPICE File name: y14w\_spice.zip, y14w\_x32\_spice.zip File rev: 2.1**

**EBD file name (if applicable): File rev:**

**Die Rev: G**

**Date: June 18, 2008**

**Datasheet Link**<http://download.micron.com/pdf/datasheets/dram/sdram/64MSDRAM.pdf>,  
<http://download.micron.com/pdf/datasheets/dram/sdram/64MSDRAMx32.pdf>

E-mail at [modelsupport@micron.com](mailto:modelsupport@micron.com) for questions regarding Quality Report

- ☒ Include the IBIS Quality Summary information in the Quality report. For details on IBIS Quality check the quality specification and quality checklist on IBIS quality webpage  
[http://www.vhdl.org/pub/ibis/quality\\_wip/](http://www.vhdl.org/pub/ibis/quality_wip/)

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#####
|                               IBIS Quality Notes                               |
|#####|
|IQ SUMMARY Overall Quality of component and models Level 2b|
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|IQ Level 0 - 0 errors 0 warnings|
|IQ Level 1 - All checks done for completeness and correctness|
|IQ Level 2 – HSPICE/Measurement Correlation|
|IQ Buffer dqbuff: Quality level 2b|
|IQ Buffer inbuff: Quality level 2b|
|IQ Buffer inbuff2: Quality level 2b|
|IQ Buffer clkbuff: Quality level 2b|
|
|IQ Level 0|
|All Level 1 checks performed and are either OK or NA|
|
|IQ Level 1|
|All Level 1 checks performed and are either OK or NA|
|
```

# IQ Level 2b

- | Using V-t IBIS Data compared to source HSPICE models
- | Using I-V Data compared to measurement data
- | Using C\_comp compared to measurement data

## IQ BEGIN IBIS Quality Checklist

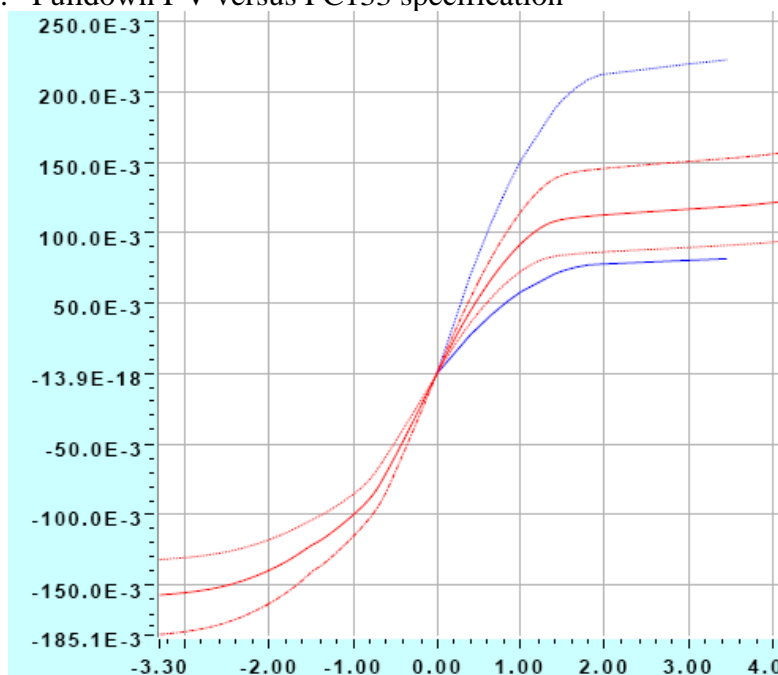
IQ FILE: y14w.ibs/y14w_x32.ibs	IQ Level: 1
IQ COMPONENT: MT48LC16M4A2TG	IQ Level: 1
IQ COMPONENT: MT48LC8M8A2TG	IQ Level: 1
IQ COMPONENT: MT48LC4M16A2TG	IQ Level: 1
IQ COMPONENT: MT48LC4M16A2F4	IQ Level: 1
IQ COMPONENT: MT48LC2M32B2TG	IQ Level: 1
IQ COMPONENT: MT48LC2M32B2B5	IQ Level: 1
IQ MODEL: dqbuff	IQ Level: 2b
IQ MODEL: inbuff	IQ Level: 2b
IQ MODEL: inbuff2	IQ Level: 2b
IQ MODEL: clkbuff	IQ Level: 2b

IQ END IBIS Quality Checklist

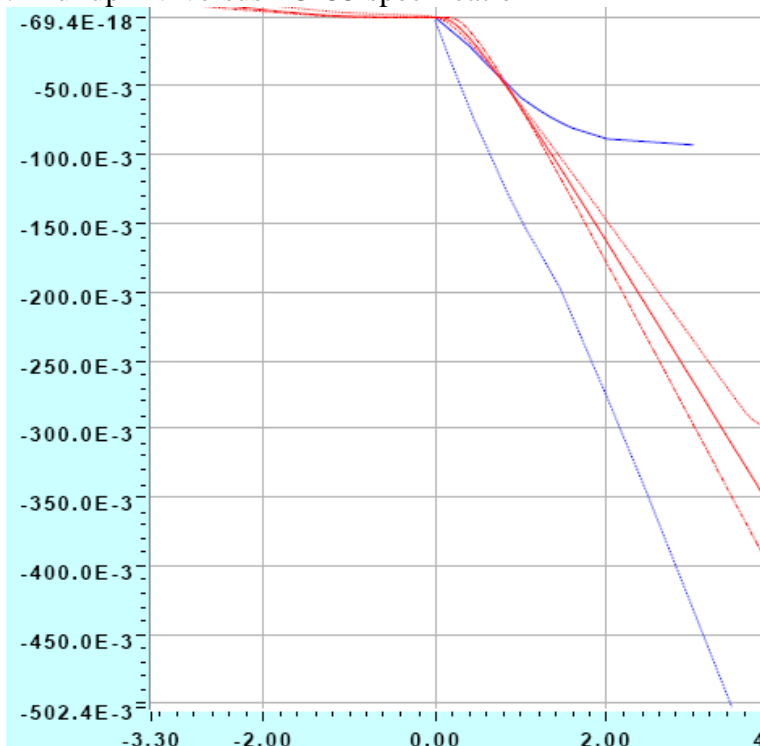
## IBIS MODEL Correlation

### Datasheet Correlation

1. ☒ For Output model or I/O model compare datasheet IOH/IOL data with Ibis pullup/pulldown data.
  - a. Model Name **dqbuff**
    - i. Pulldown I-V versus PC133 specification



ii. Pullup I-V versus PC133 specification



2. ☒ Compare C\_comp with datasheet Input C. Provide C\_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16)

Insert component name here **MT48LC4M16A2TG**

		IBIS		Datasheet	
		min	max	min	max
<b>DQ</b>	C_comp	3.80	4.50	NA	NA
	C package	0.52	1.12	NA	NA
	C_total	4.32	5.62	4.00	6.00
<b>INPUT</b>	C_comp	2.00	2.50	NA	NA
	C package	0.82	1.33	NA	NA
	C_total	2.82	3.83	2.50	3.80
<b>CLK</b>	C_comp	2.20	2.70	NA	NA
	C package	0.84	0.84	NA	NA
	C_total	3.04	3.54	2.50	3.50
<b>WE</b>	C_comp	2.40	2.90	NA	NA
	C package	0.77	0.77	NA	NA
	C_total	3.17	3.67	2.50	3.80
<b>DM</b>	C_comp	2.30	2.80	NA	NA
	C package	0.73	0.79	NA	NA
	C_total	3.03	3.59	2.50	3.80

Insert component name here **MT48LC4M16A2F4**

		IBIS		Datasheet	
		min	max	min	max
<b>DQ</b>	C_comp	3.80	4.50	NA	NA
	C package	0.67	1.72	NA	NA
	C_total	4.47	6.22	TBD	TBD
<b>INPUT</b>	C_comp	2.00	2.50	NA	NA
	C package	0.88	1.86	NA	NA
	C_total	2.88	4.36	TBD	TBD
<b>CLK</b>	C_comp	2.20	2.70	NA	NA
	C package	1.77	1.77	NA	NA
	C_total	3.97	4.47	TBD	TBD
<b>WE</b>	C_comp	2.40	2.90	NA	NA
	C package	2.21	2.21	NA	NA
	C_total	4.61	5.11	TBD	TBD
<b>DM</b>	C_comp	2.30	2.80	NA	NA
	C package	1.63	2.07	NA	NA
	C_total	3.93	4.87	TBD	TBD

Insert component name here **MT48LC2M32B2TG**

		IBIS		Datasheet	
		min	max	min	max
<b>DQ</b>	C_comp	3.80	4.50	NA	NA
	C package	0.58	0.97	NA	NA
	C_total	4.38	5.47	4.00	6.50
<b>INPUT</b>	C_comp	2.00	2.50	NA	NA
	C package	0.49	0.54	NA	NA
	C_total	2.49	3.04	2.50	4.00
<b>CLK</b>	C_comp	2.20	2.70	NA	NA
	C package	0.51	0.51	NA	NA
	C_total	2.71	3.21	2.50	4.00
<b>WE</b>	C_comp	2.40	2.90	NA	NA
	C package	0.54	0.54	NA	NA
	C_total	2.94	3.44	2.50	4.00
<b>DM</b>	C_comp	2.30	2.80	NA	NA
	C package	0.52	0.56	NA	NA
	C_total	2.82	3.36	2.50	4.00

Insert component name here **MT48LC2M32B2B5**

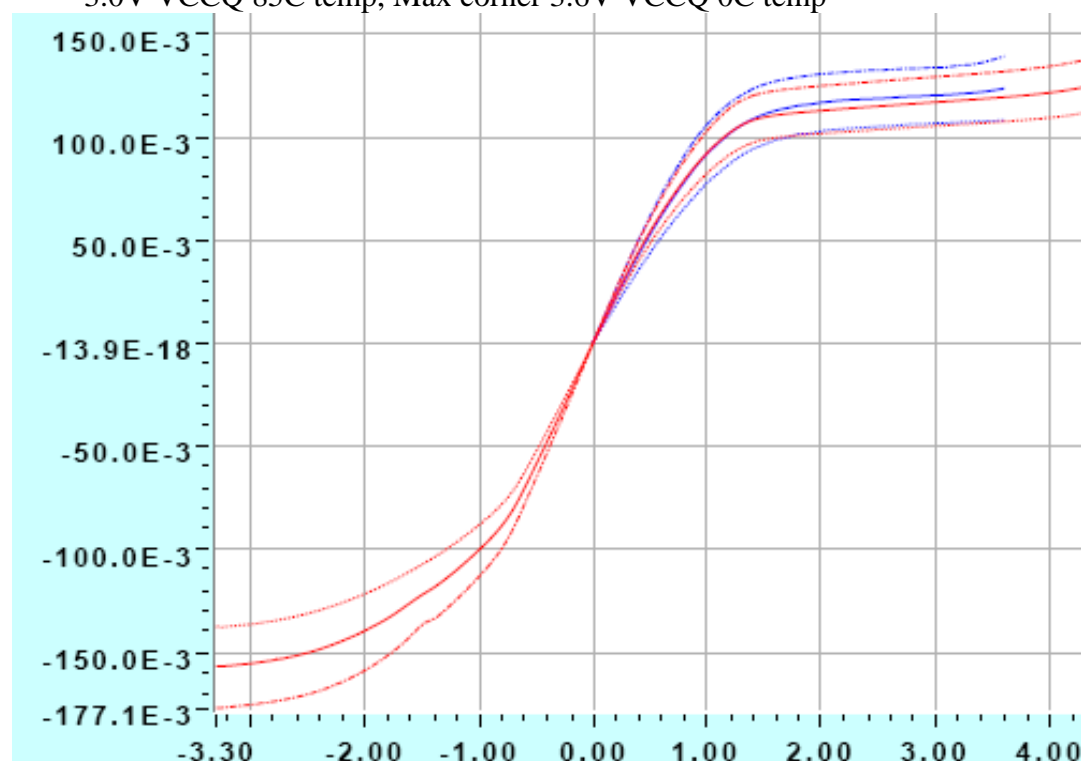
		IBIS		Datasheet	
		min	max	min	max
<b>DQ</b>	C_comp	3.80	4.50	NA	NA
	C package	0.54	1.05	NA	NA
	C_total	4.34	5.55	4.00	6.50
<b>INPUT</b>	C_comp	2.00	2.50	NA	NA
	C package	1.06	1.63	NA	NA
	C_total	3.06	4.13	2.50	4.00

CLK	C_comp	2.20	2.70	NA	NA
	C_package	1.22	1.22	NA	NA
	C_total	3.42	3.92	2.50	4.00
WE	C_comp	2.40	2.90	NA	NA
	C_package	1.33	1.33	NA	NA
	C_total	3.73	4.23	2.50	4.00
DM	C_comp	2.30	2.80	NA	NA
	C_package	0.52	0.96	NA	NA
	C_total	2.82	3.76	2.50	4.00

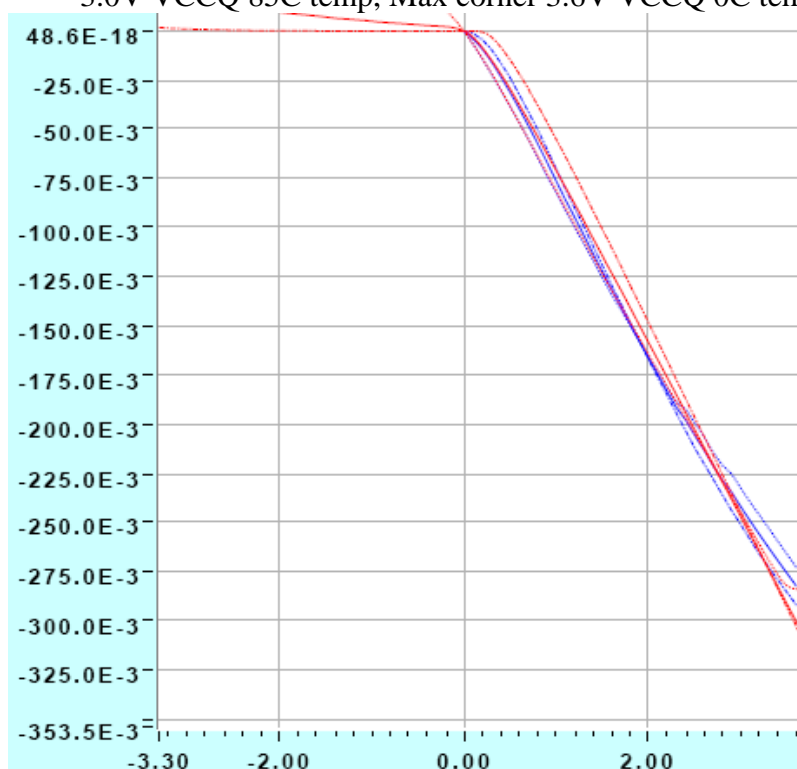
3. ☐ If slew rate specifications (Rise slew and Fall slew) are available from the datasheet, complete Hspice simulation to generate slew rate data and provide a comparison table.

### Measurement Correlation

1. ☒ For Output model or I/O model compare measured IOH/IOL data with IBIS pullup pulldown data. If the measurement condition is different than IBIS condition, run Hspice simulation using the same measurement condition, for example Vcc, temp and process. Include measurement conditions in the pullup/pulldown images.
- Model Name **dqbuff**
    - Pulldown comparison, Model (red), Measurements (blue), Min corner 3.0V VCCQ 85C temp, Max corner 3.6V VCCQ 0C temp



- ii. Pullup comparison, Model (red), Measurements (blue), Min corner 3.0V VCCQ 85C temp, Max corner 3.6V VCCQ 0C temp



2. ☒ Compare C\_comp with measured C\_comp. Provide C\_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16)

Insert component name here **MT48LC4M16A2TG**

		IBIS			Measured		
		min	typ	max	min	typ	max
<b>DQ</b>	C_comp	3.80	4.15	4.50	NA	NA	NA
	C package	0.52	0.71	1.12	NA	NA	NA
	C_total	4.32	4.86	5.62	4.32	4.74	5.36
<b>INPUT</b>	C_comp	2.00	2.25	2.50	NA	NA	NA
	C package	0.82	1.11	1.33	NA	NA	NA
	C_total	2.82	3.36	3.83	3.00	3.33	3.76
<b>CLK</b>	C_comp	2.20	2.45	2.70	NA	NA	NA
	C package	0.84	0.84	0.84	NA	NA	NA
	C_total	3.04	3.29	3.54	3.24	3.43	3.34
<b>WE</b>	C_comp	2.40	2.65	2.90	NA	NA	NA
	C package	0.77	0.77	0.77	NA	NA	NA
	C_total	3.17	3.42	3.67	3.53	3.60	3.67
<b>DM</b>	C_comp	2.30	2.55	2.80	NA	NA	NA
	C package	0.73	0.76	0.79	NA	NA	NA
	C_total	3.03	3.31	3.59	3.19	3.28	3.40

Insert component name here **MT48LC4M16A2F4**

		IBIS			Measured		
		min	typ	max	min	typ	max
<b>DQ</b>	C_comp	3.80	4.15	4.50	NA	NA	NA
	C_package	0.67	1.11	1.72	NA	NA	NA
	C_total	4.47	5.26	6.22	5.03	5.40	6.08
<b>INPUT</b>	C_comp	2.00	2.25	2.50	NA	NA	NA
	C_package	0.88	1.41	1.86	NA	NA	NA
	C_total	2.88	3.66	4.36	3.20	3.64	3.98
<b>CLK</b>	C_comp	2.20	2.45	2.70	NA	NA	NA
	C_package	1.77	1.77	1.77	NA	NA	NA
	C_total	3.97	4.22	4.47	4.13	4.16	4.19
<b>WE</b>	C_comp	2.40	2.65	2.90	NA	NA	NA
	C_package	2.21	2.21	2.21	NA	NA	NA
	C_total	4.61	4.86	5.11	4.85	4.87	4.89
<b>DM</b>	C_comp	2.30	2.55	2.80	NA	NA	NA
	C_package	1.63	1.85	2.07	NA	NA	NA
	C_total	3.93	4.40	4.87	4.08	4.27	4.48

Insert component name here **MT48LC2M32B2TG**

		IBIS			Measured		
		min	typ	max	min	typ	max
<b>DQ</b>	C_comp	3.80	4.15	4.50	NA	NA	NA
	C_package	0.58	0.72	0.97	NA	NA	NA
	C_total	4.38	4.87	5.47	4.43	4.87	5.48
<b>INPUT</b>	C_comp	2.00	2.25	2.50	NA	NA	NA
	C_package	0.49	0.52	0.54	NA	NA	NA
	C_total	2.49	2.77	3.04	2.54	2.79	3.02
<b>CLK</b>	C_comp	2.20	2.45	2.70	NA	NA	NA
	C_package	0.51	0.51	0.51	NA	NA	NA
	C_total	2.71	2.96	3.21	2.94	3.03	3.13
<b>WE</b>	C_comp	2.40	2.65	2.90	NA	NA	NA
	C_package	0.54	0.54	0.54	NA	NA	NA
	C_total	2.94	3.19	3.44	3.30	3.42	3.55
<b>DM</b>	C_comp	2.30	2.55	2.80	NA	NA	NA
	C_package	0.52	0.55	0.56	NA	NA	NA
	C_total	2.82	3.10	3.36	3.05	3.18	3.31

Insert component name here **MT48LC2M32B2B5**

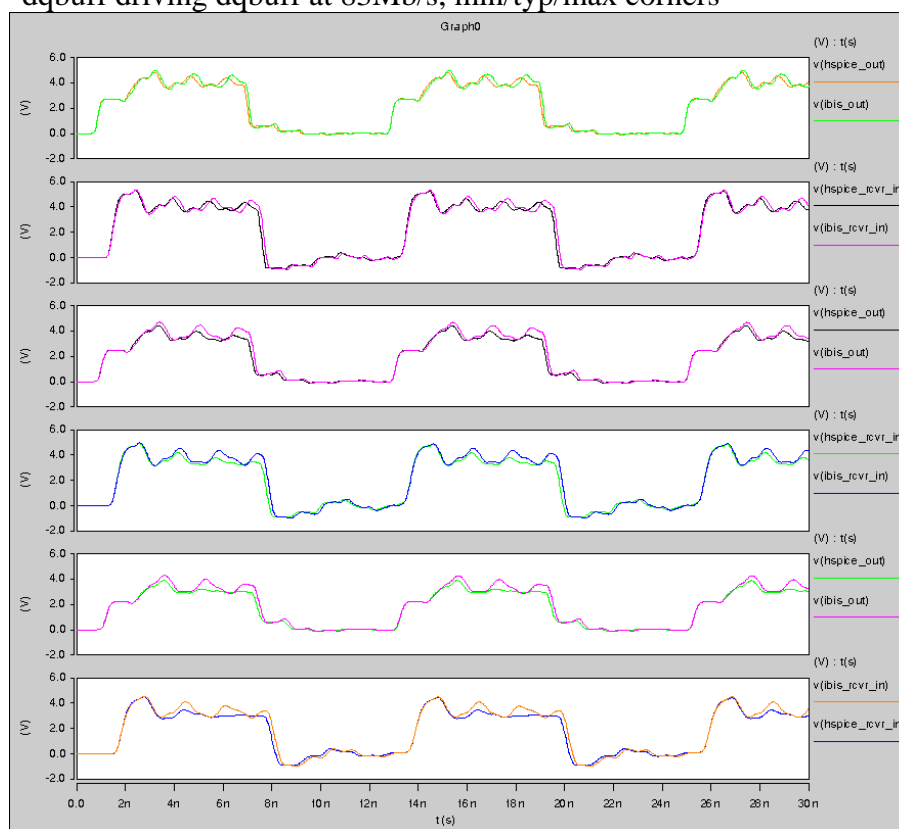
		IBIS			Measured		
		min	typ	max	min	typ	max
<b>DQ</b>	C_comp	3.80	4.15	4.50	NA	NA	NA
	C_package	0.54	0.79	1.05	NA	NA	NA
	C_total	4.34	4.94	5.55	4.38	4.83	5.53
<b>INPUT</b>	C_comp	2.00	2.25	2.50	NA	NA	NA
	C_package	1.06	1.27	1.63	NA	NA	NA
	C_total	3.06	3.52	4.13	3.19	3.57	3.97

CLK	C_comp	2.20	2.45	2.70	NA	NA	NA
	C_package	1.22	1.22	1.22	NA	NA	NA
	C_total	3.42	3.67	3.92	3.74	3.84	3.95
WE	C_comp	2.40	2.65	2.90	NA	NA	NA
	C_package	1.33	1.33	1.33	NA	NA	NA
	C_total	3.73	3.98	4.23	3.79	3.98	4.18
DM	C_comp	2.30	2.55	2.80	NA	NA	NA
	C_package	0.52	0.74	0.96	NA	NA	NA
	C_total	2.82	3.29	3.76	2.97	3.23	3.53

3. ☐ If measured clamp current data is available provide an IBIS and Silicon clamp comparison for all models

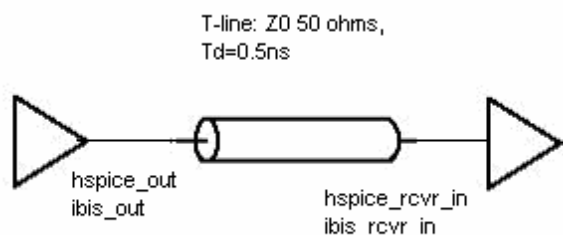
### IBIS vs HSPICE Correlation

1. ☒ For all output model or I/O model run Hspice transient simulation using encrypted netlist and using IBIS model (b-element).
  - a. ☒ Use the below setup and node naming conventions for the IBIS and Hspice deck file (.sp file). Indicate and update the setup diagram if it is different. Indicate version of Hspice simulator used for simulation 2007.03-SP1
  - b. ☒ Run simulation for all corner cases and at maximum allowable speed grade
    - i. dqbuff driving dqbuff at 83Mb/s, min/typ/max corners





## Setup



## Comments:

Model is matched to measurements of Pullup/Pulldown I-V data and input capacitance.

## Document Revision history

Rev 1.0 – 6/18/2008

- a. IBIS revision 2.2
- b. HSPICE revision 2.1