esign ID: Z11B

Description: 8Gb DDR4 SDRAM

Marketing device name(s): MT40A2G4SA, MT40A1G8SA, MT40A512M16LY, MT40A2G4Z11B, MT40A1G8Z11B, MT40A512M16Z11B

Valid speed grades DDR4-1600, DDR4-1866, DDR4-2133, DDR4-2666, DDR4-2400, DDR4-2933, DDR4-3200

Zip filename: z11b_ibis.zip

IBIS filename (Version 5.0): z11b.ibs, z11b_it.ibs **File rev:** 2.9.2

HSPICE filename: N/A **File rev:** .

Die revision: E

Date: February 27, 2023

Datasheet Link (from micron.com):

For support contact your local Micron FAE/Sales contacts
(more information at https://www.micron.com/support/sales-network)

Device Parameters

VDDQ **Slow:** 1.14V **Typical:** 1.20V **Fast:** 1.26V

VDD **Slow:** 1.14V **Typical:** 1.20V **Fast:** 1.26V

Junction Temperature (Commercial) **Slow:** 110C **Typical:** 50C **Fast:** 0C

Junction Temperature (Industrial) **Slow:** 110C **Typical:** 50C **Fast:** -40C

VDDQ/VSSQ Decoupling Capacitance (Approximate value at 10MHz) – Full Die: 6.7nF

Included in HSPICE DQ/DQS/DM models? Yes **Amount per DQ/DQS/DM model:** 304.4pF

Included in IBIS DQ/DQS/DM models? No, must be included with separate Spice subcircuit (.ckt files) found in the zip file.

VDDQ/VSSQ Decoupling Capacitance ESR – Full Die: 55mohm

VDDQ/VSSQ Decoupling Capacitance ESR – per DQ model: 1.2ohm

IBIS Quality Summary

1. ☒ Include the IBIS Quality Specification 2.0 Overall IBIS Quality level. For details on IBIS Quality, reference the quality specification and quality checklist on IBIS quality webpage http://www.ibis.org/quality_wip/checklist.html.

   Overall IBIS Quality Level: **IQ3MSX**

   Exceptions: **V-t length in Version 5.0 model is excessive due to inclusion of [Composite Current] I-t data.**

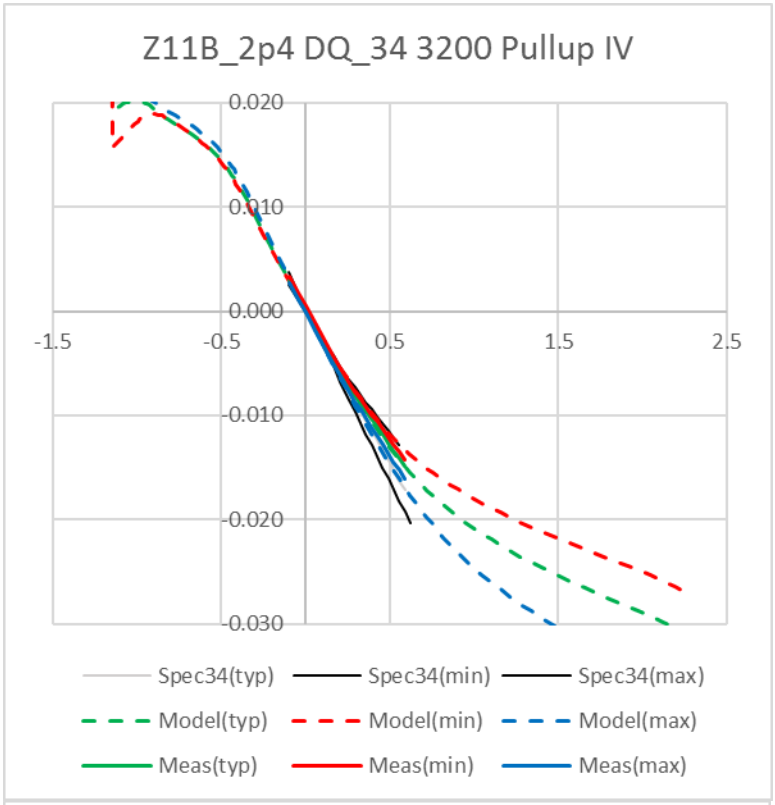
2. ☒ Include the filename of the IBIS Quality Checklist that accompanies this report.

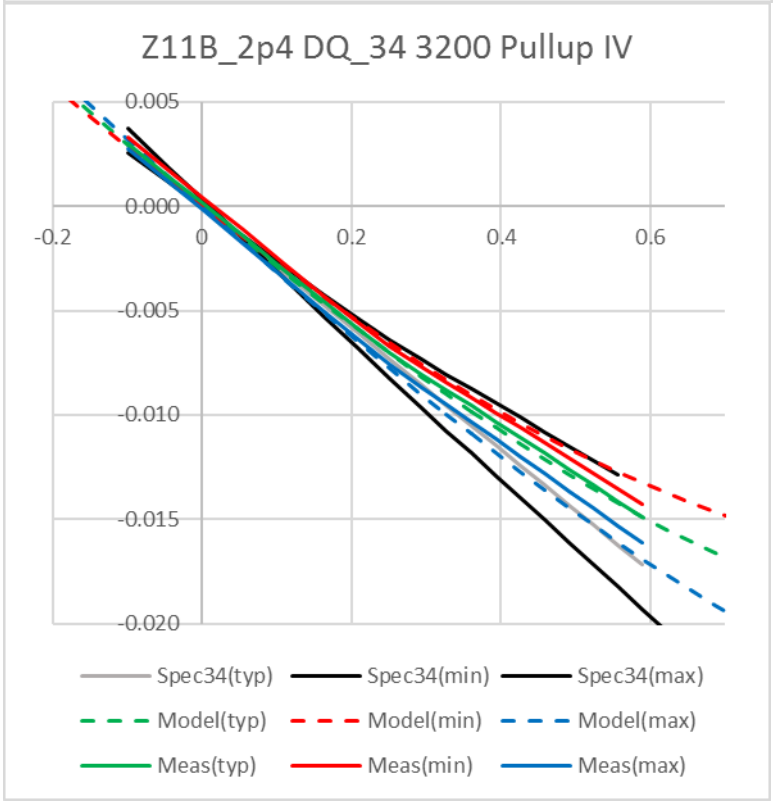
   Filename for Version 5.0 file: **z11b_ibis_quality_checklist.xls**

IBIS Model Correlation: datasheet

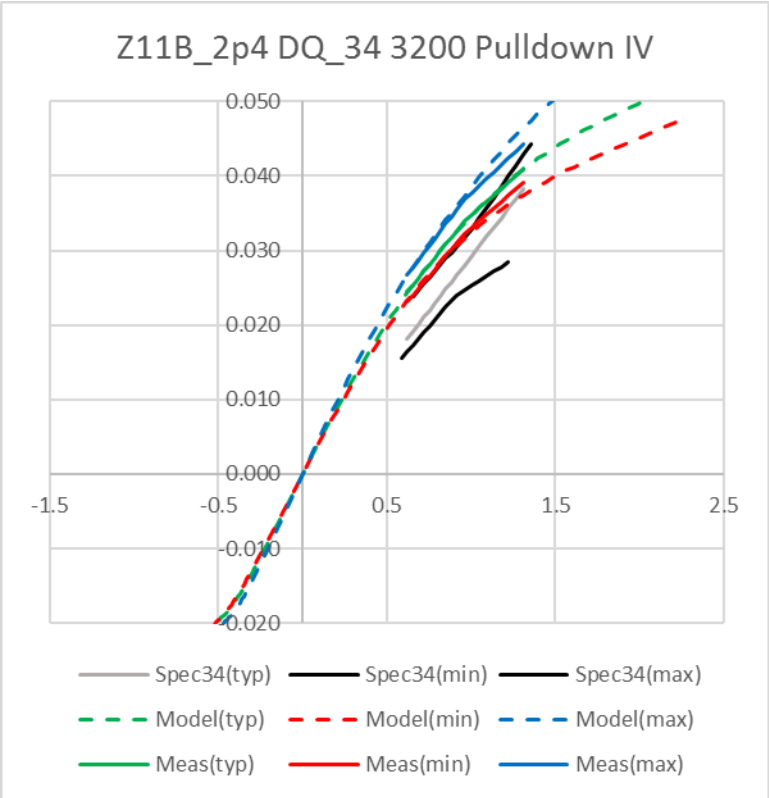
1. ☒ For Output or I/O model compare datasheet IOH/IOL data with IBIS pullup/pulldown data.

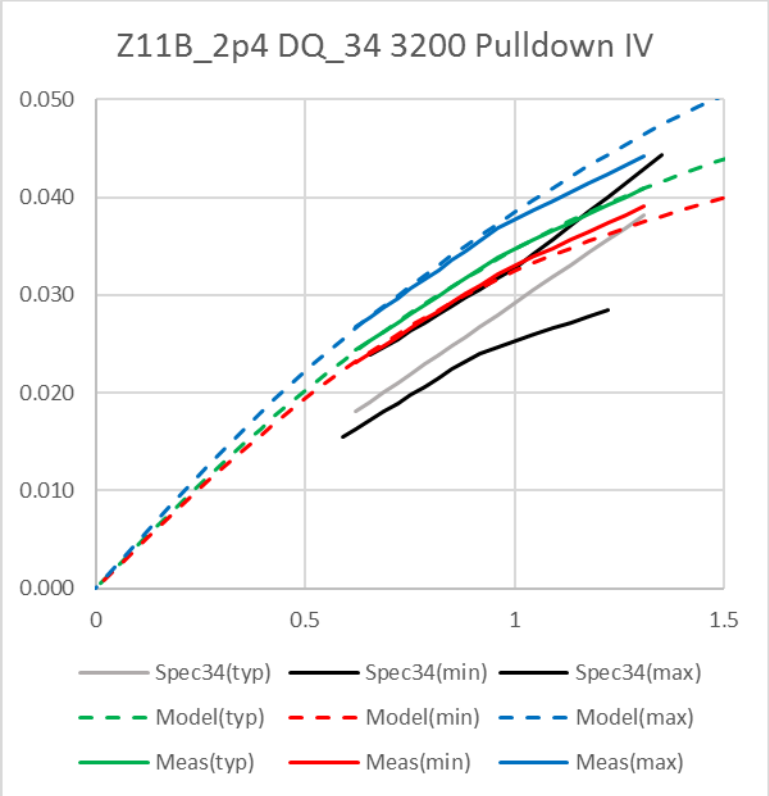
a. Model name: **DQ_34_3200**
   i. Pullup I-V versus **JEDEC** specification





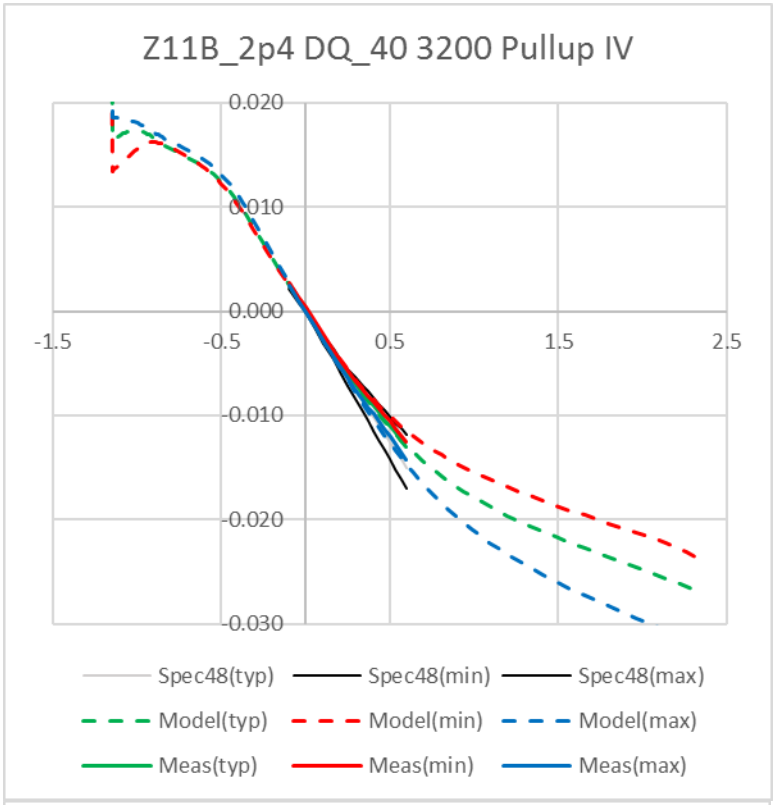
ii. Pulldown I-V versus **JEDEC** specification

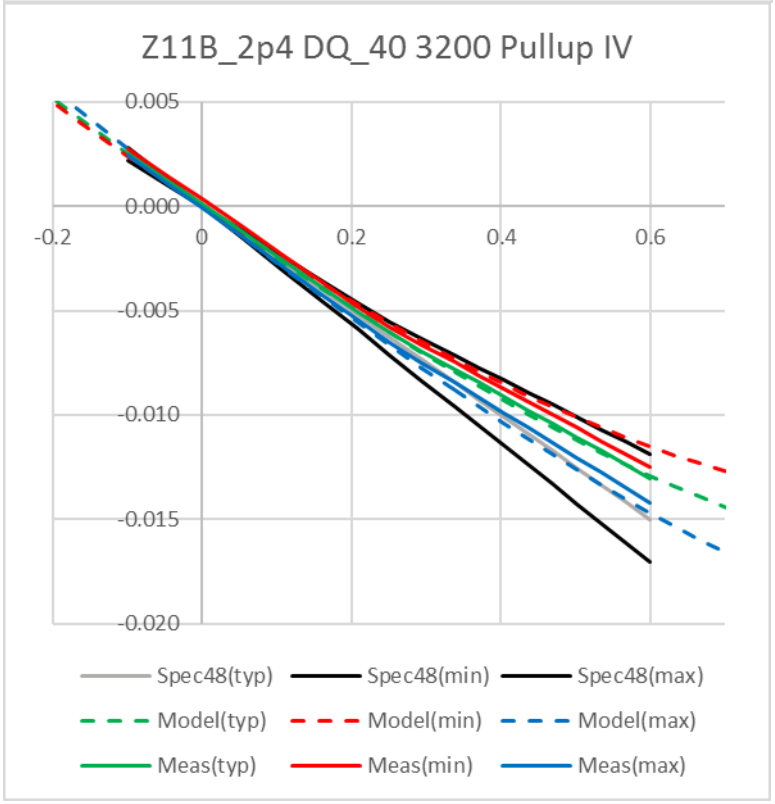




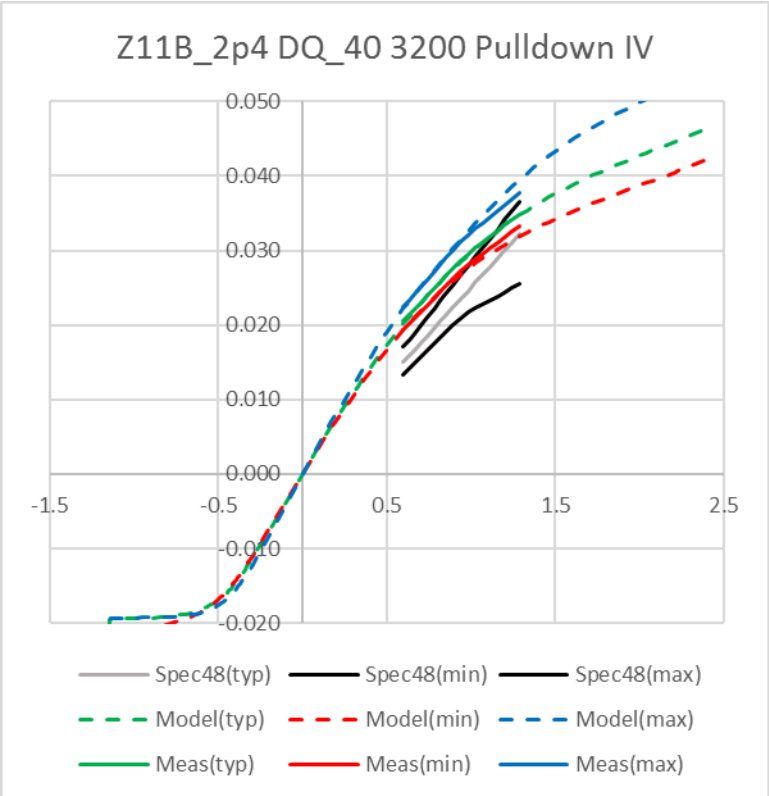
b. Model name: **DQ_40_3200**

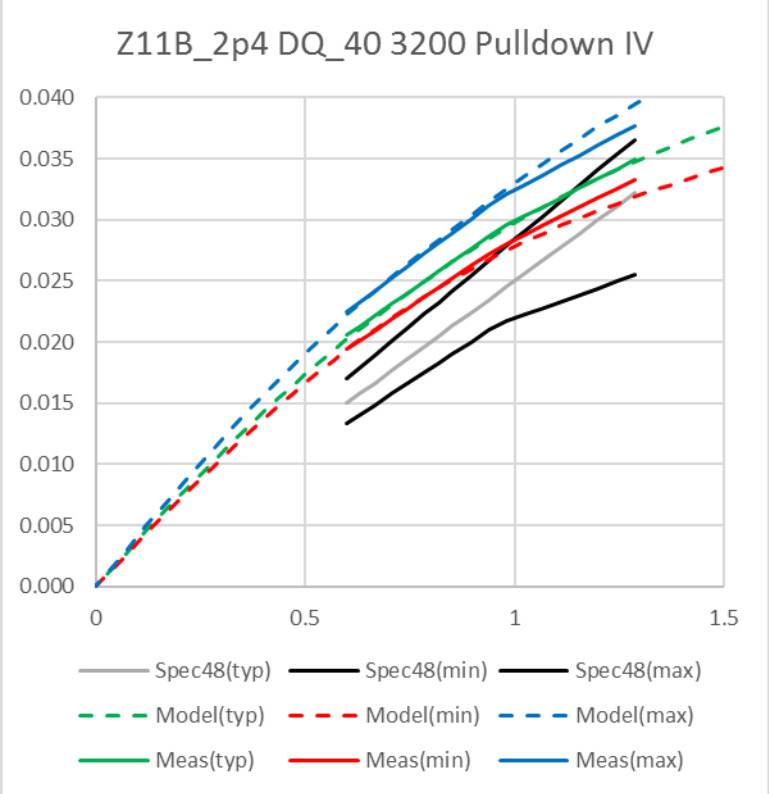
i. Pullup I-V versus **JEDEC** specification



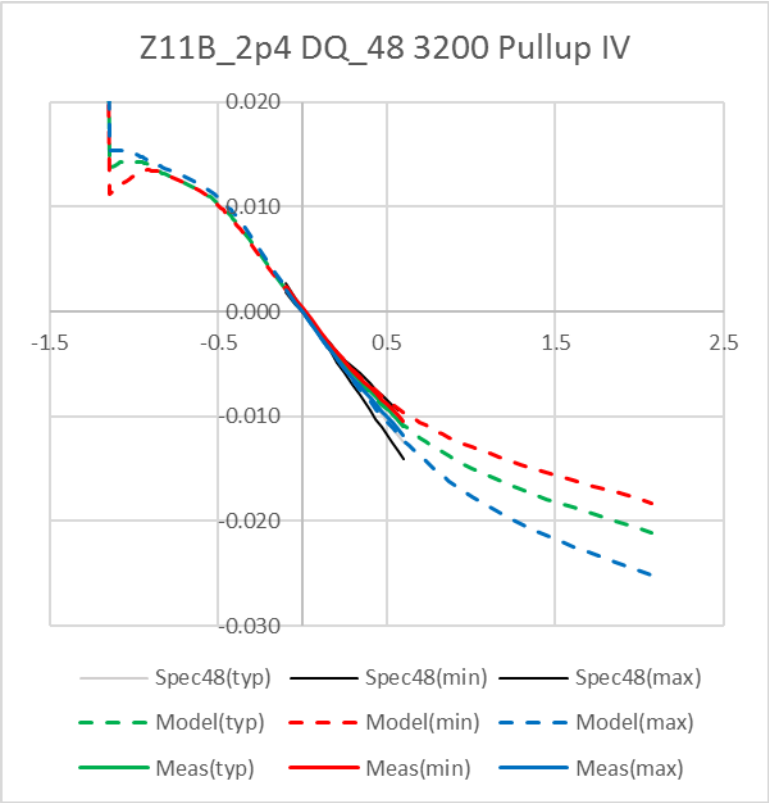


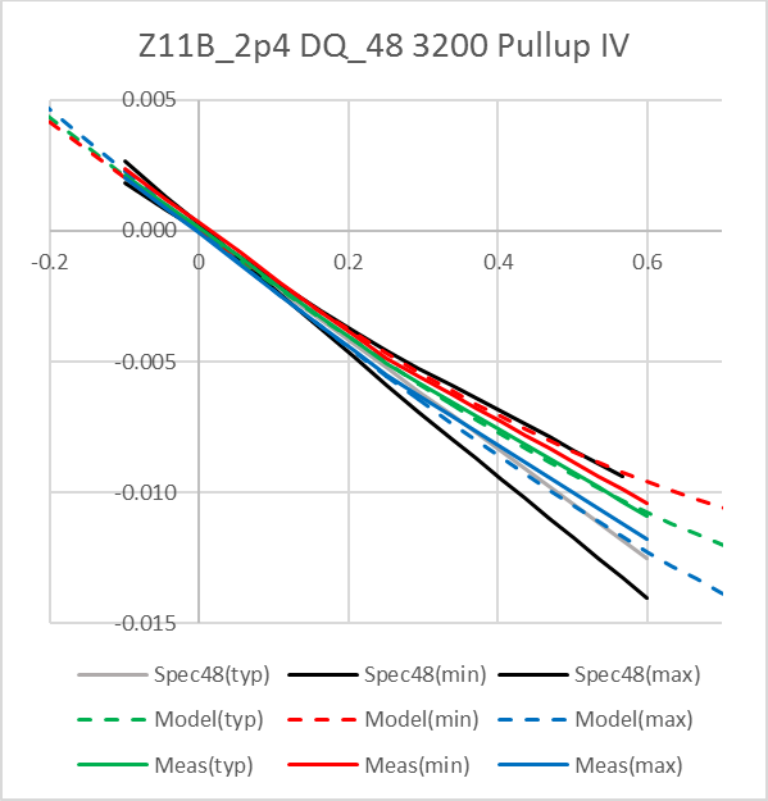
ii. Pulldown I-V versus **JEDEC** specification



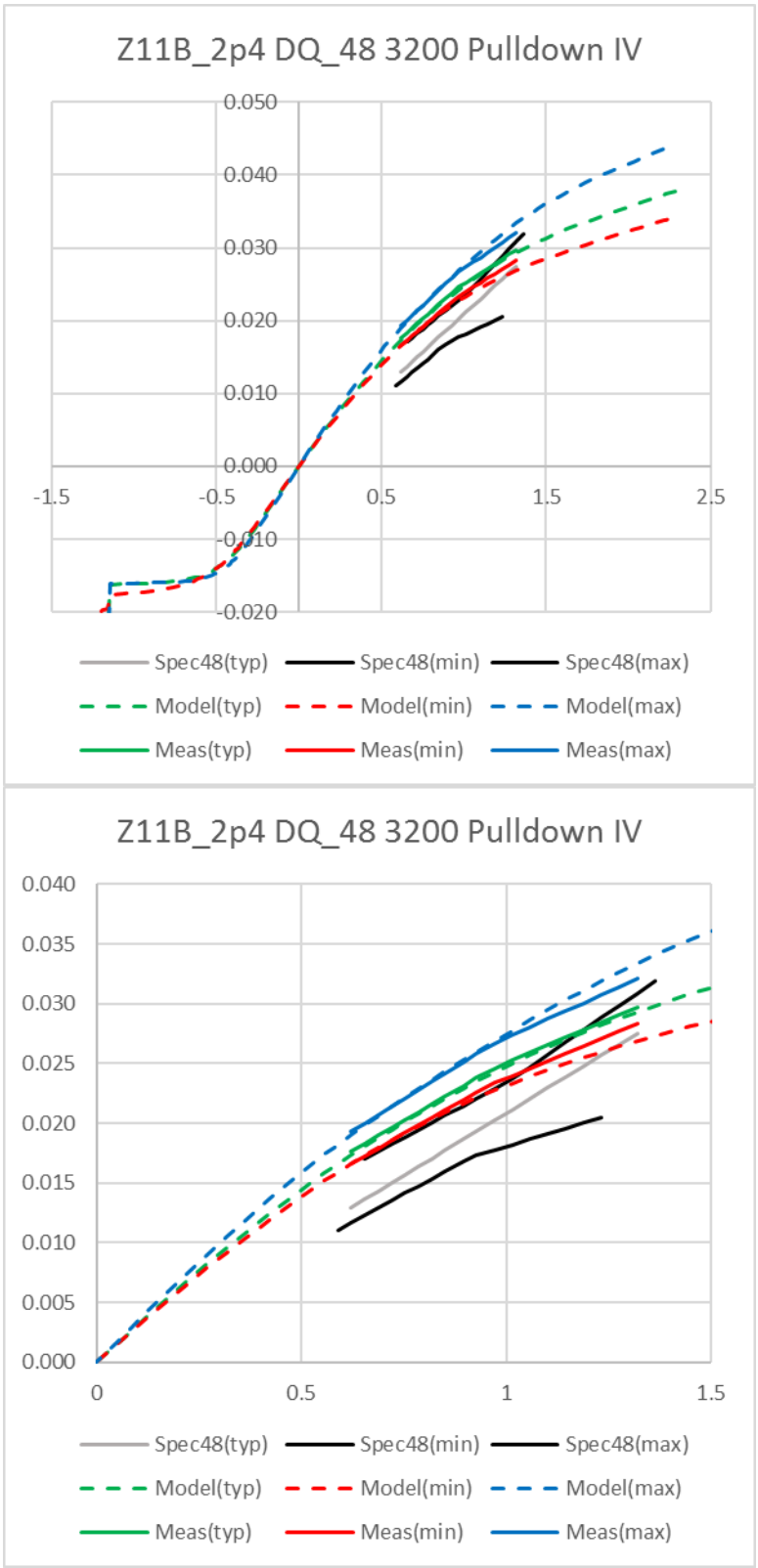


a. Model name: **DQ_48_3200**
   i. Pullup I-V versus **JEDEC** specification





i. Pulldown I-V versus **JEDEC** specification



2. ☒ Compare C_comp with datasheet Input Capacitance. Provide C_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16).

Component name:
MT40A2G4SA, MT40A1G8SA, MT40A512M16LY

Signal	IBIS die min [pF]	IBIS die max [pF]	Spec tot min [pF]	Spec tot max [pF]
DQ	0.778	0.878	**0.70**	**1.40**
INPUT	0.280	0.380	**0.20**	**0.70**
CLK	0.350	0.450	**0.20**	**0.70**
ALERT	0.768	0.868	**0.50**	**1.50**

3. ☒ Compare package impedance and time delay with datasheet specifications. Provide comparison table for all package combinations.

Component name:
MT40A2G4SA, MT40A1G8SA, MT40A512M16LY

Signal	Z pkg IBIS min [Ω]	Z pkg IBIS max [Ω]	Z pkg SPEC min [Ω]	Z pkg SPEC max [Ω]	Td pkg IBIS min [ps]	Td pkg IBIS max [ps]	Td pkg SPEC min [ps]	Td pkg SPEC max [ps]
IO	53.5	63.0	45	85	24.0	31.0	14	40
ADD/CMD	60.5	75.0	50	90	26.8	37.3	14	40
CTRL	62.7	71.4	50	90	23.5	31.1	14	40
CLK	56.9	67.5	50	90	27.0	29.5	14	42
ALERT	50.4	67.3	40	100	35.7	41.0	20	55

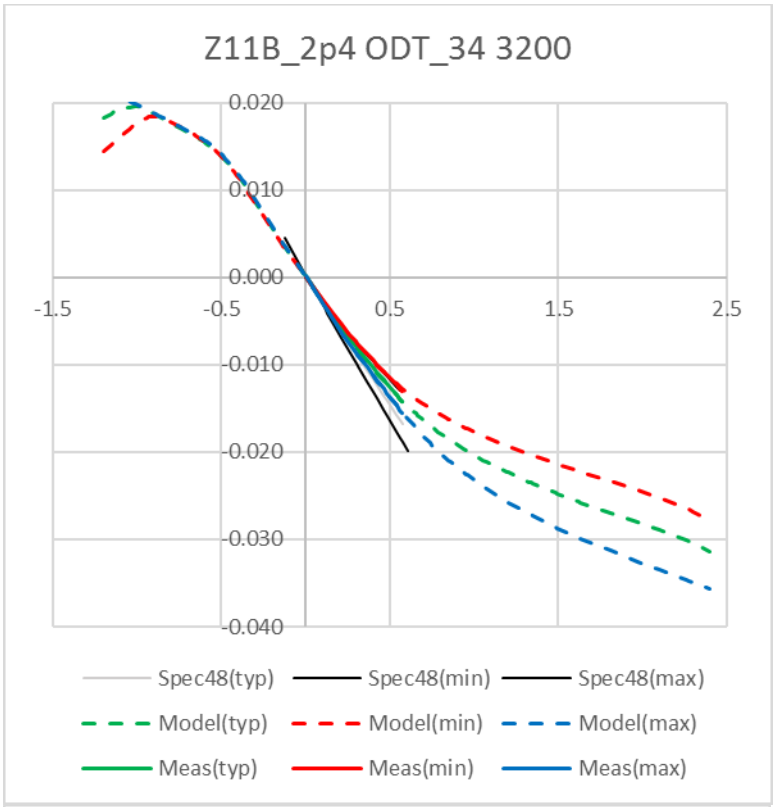
4. ☒ If slew rate specifications (rise/fall slew) are available from the datasheet, complete Spice simulations to generate slew rate data and provide a comparison table.

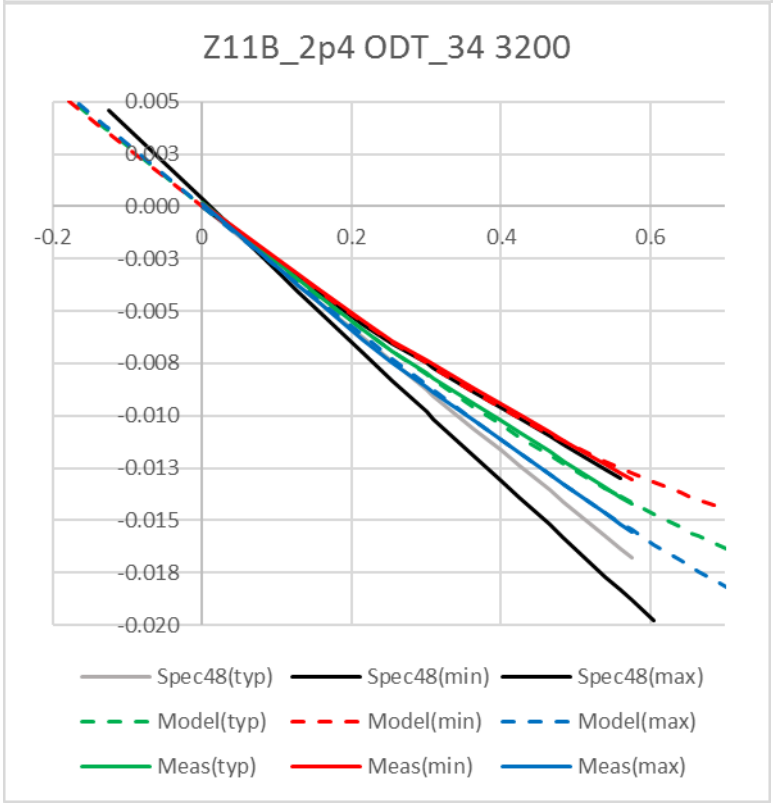
Model	IBIS slew rate RISE [V/ns] min	IBIS slew rate RISE [V/ns] typ	IBIS slew rate RISE [V/ns] max	SPEC slew rate RISE [V/ns] min	SPEC slew rate RISE [V/ns] max
DQ_34_3200	4.41	6.41	8.78	**4.0**	**9.0**

Model	IBIS slew rate FALL [V/ns] min	IBIS slew rate FALL [V/ns] typ	IBIS slew rate FALL [V/ns] max	SPEC slew rate FALL [V/ns] min	SPEC slew rate FALL [V/ns] max
DQ_34_3200	8.13	11.15	14.82	**4.0**	**9.0**

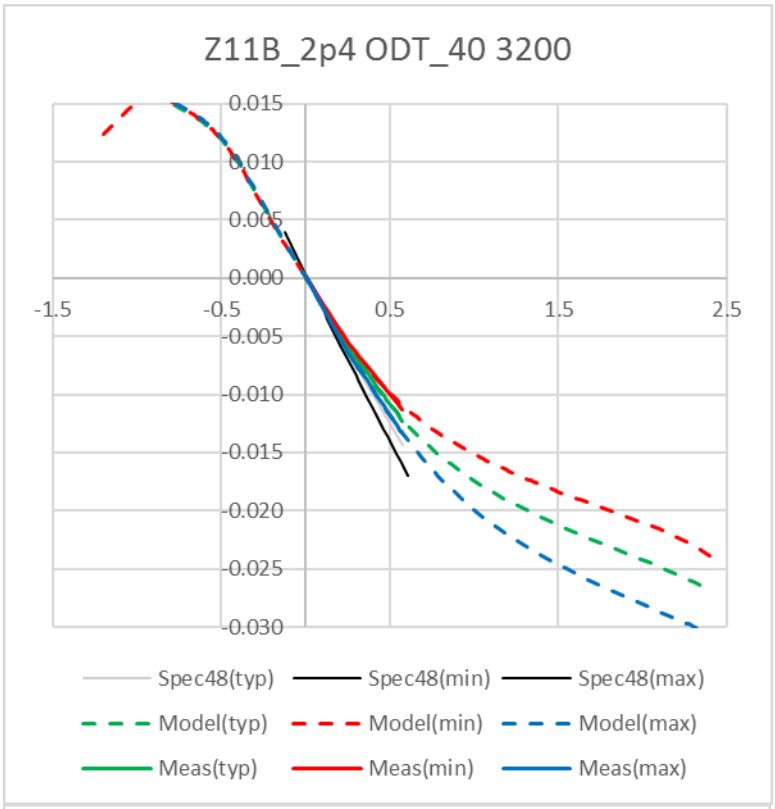
5. ☒ Compare ODT data with datasheet.

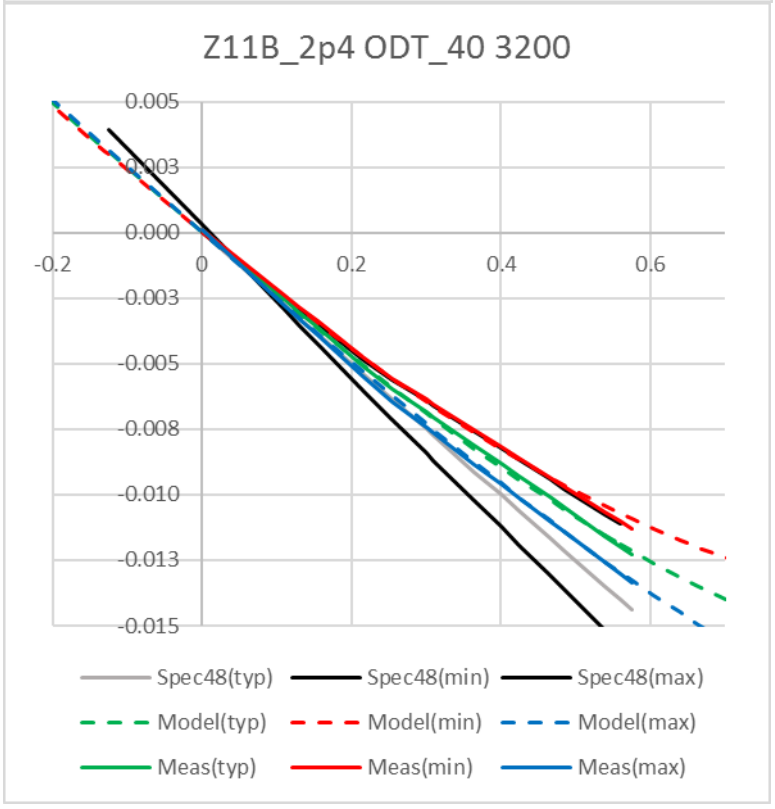
a. **ODT34**



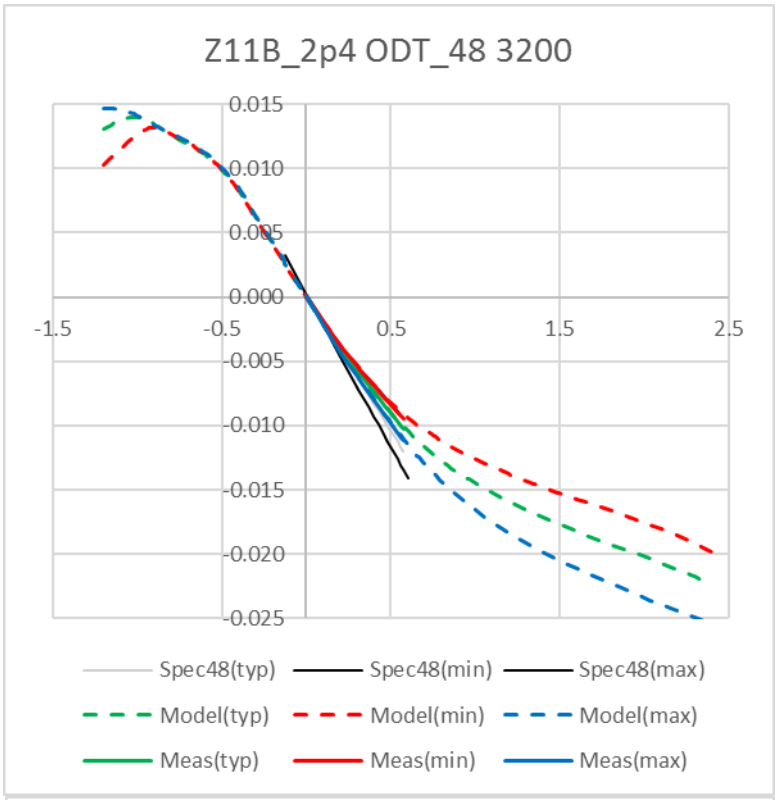


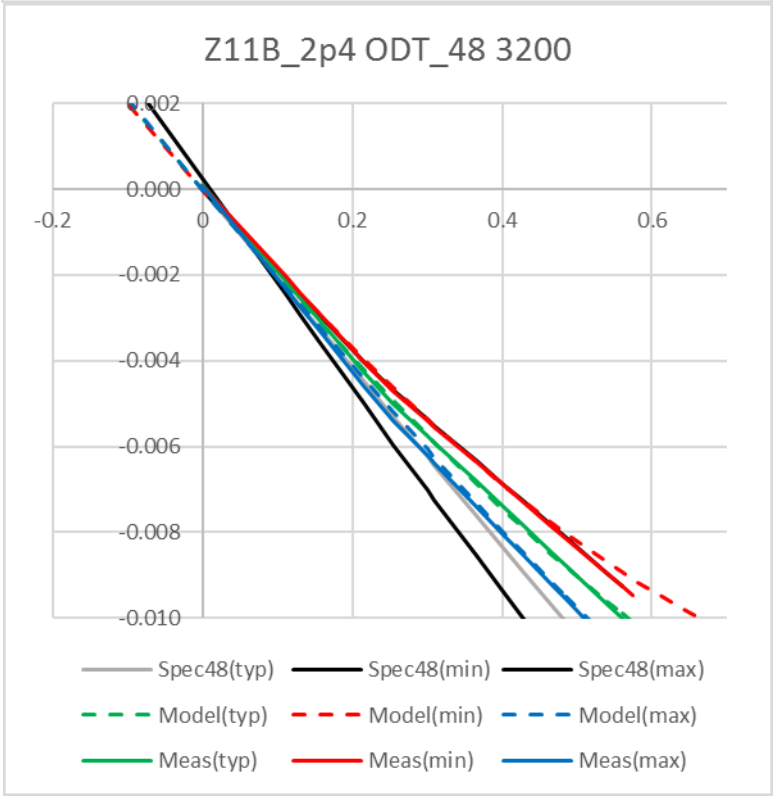
b. **ODT40**



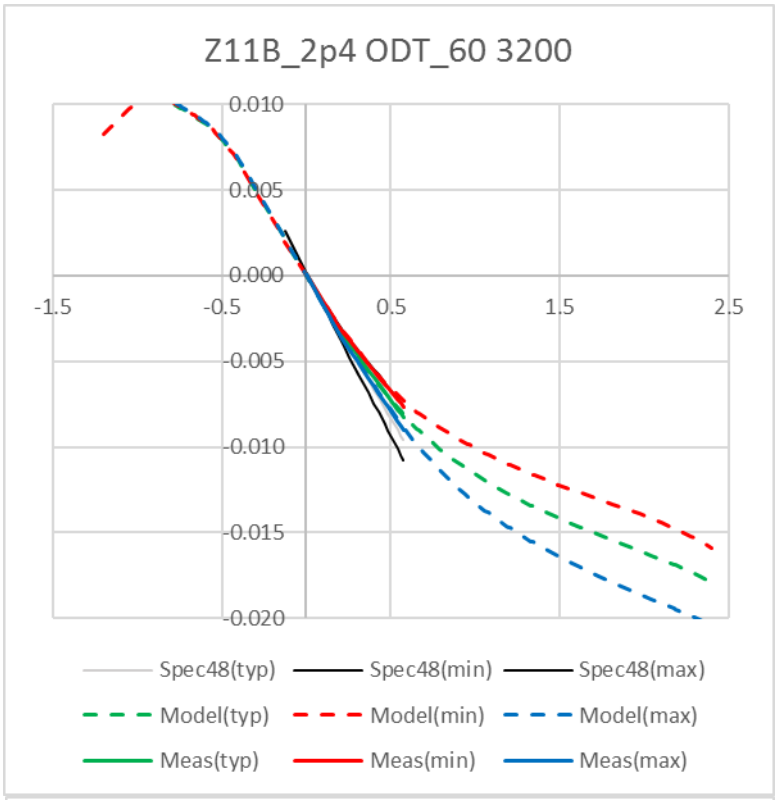


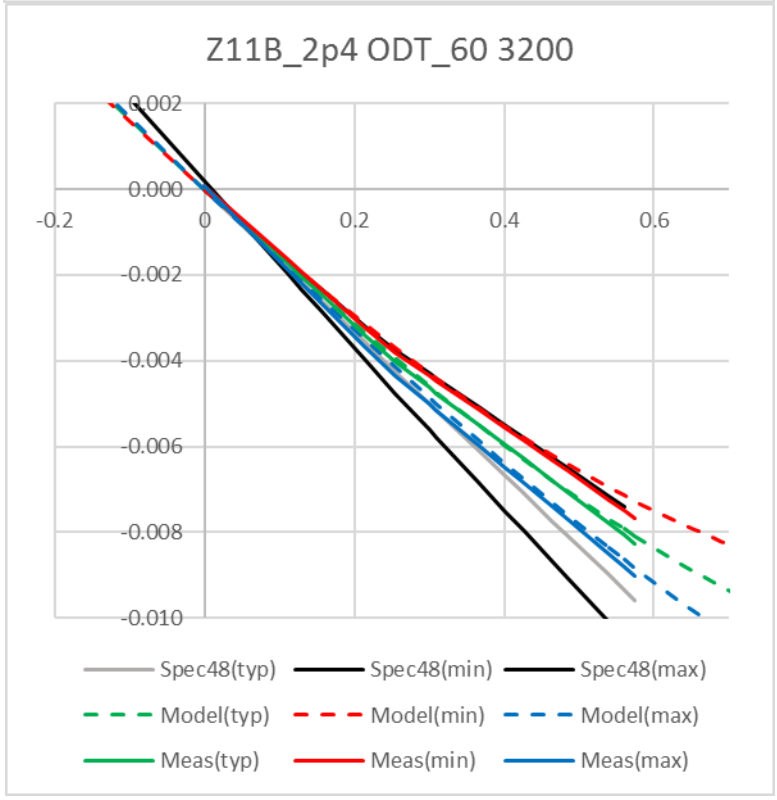
c. **ODT48**



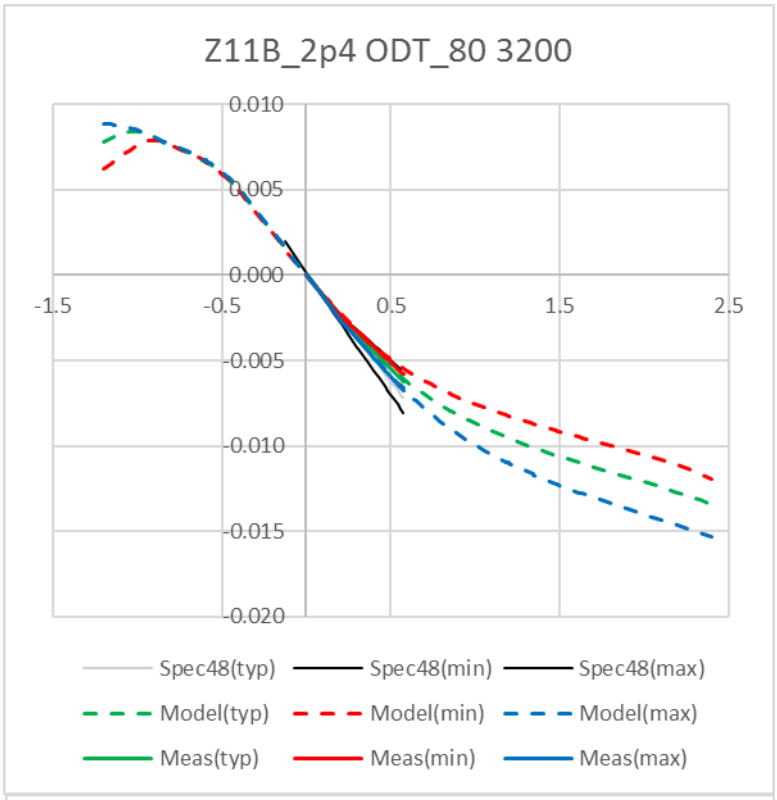


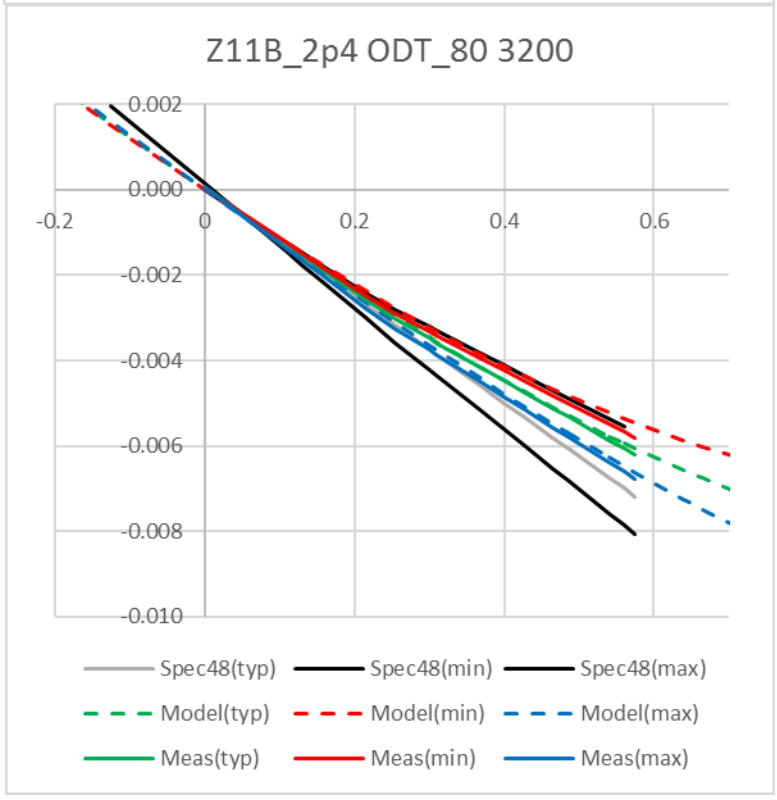
d. **ODT60**



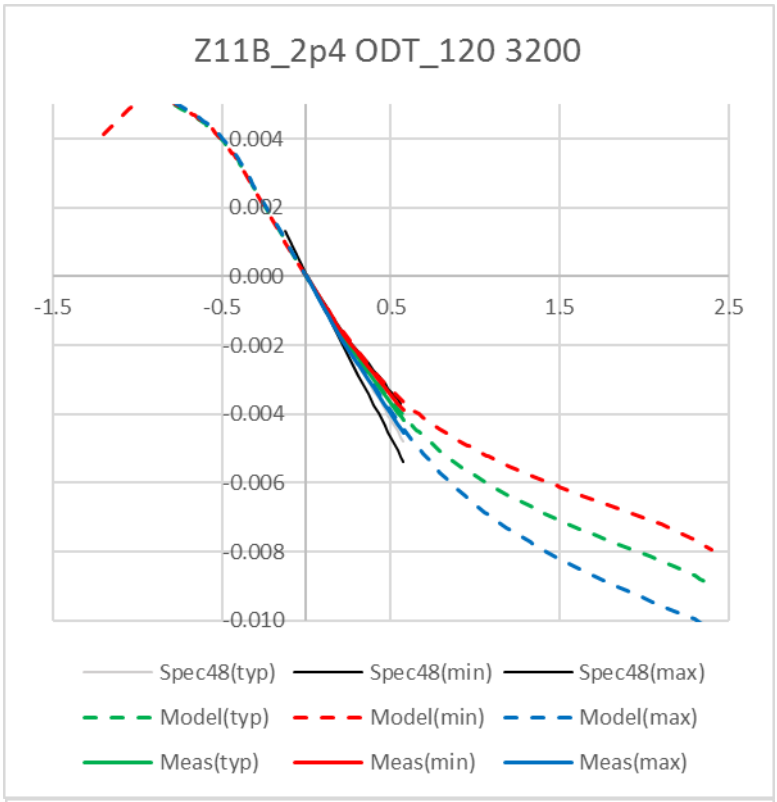


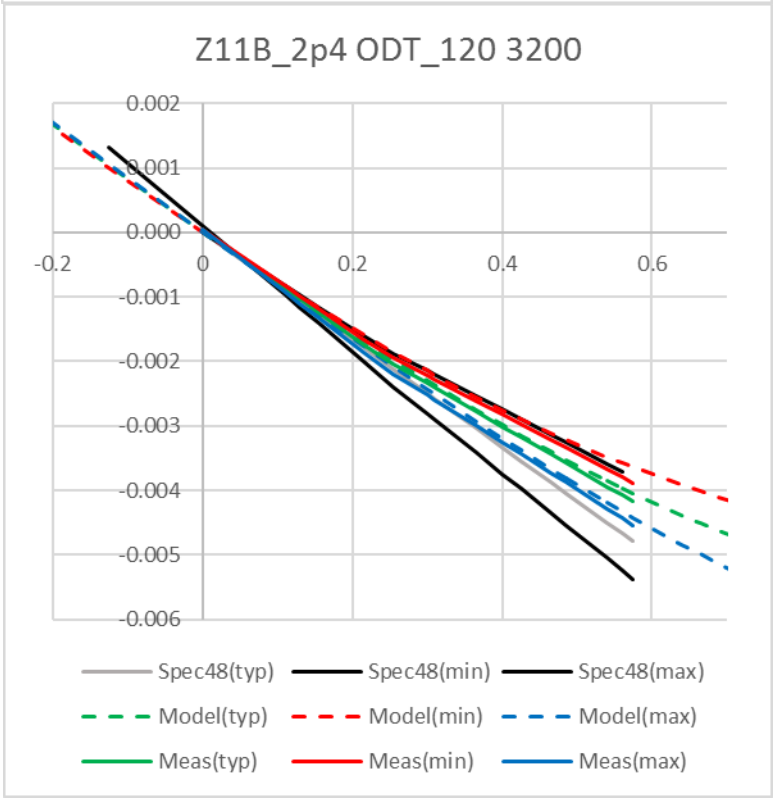
e. **ODT80**



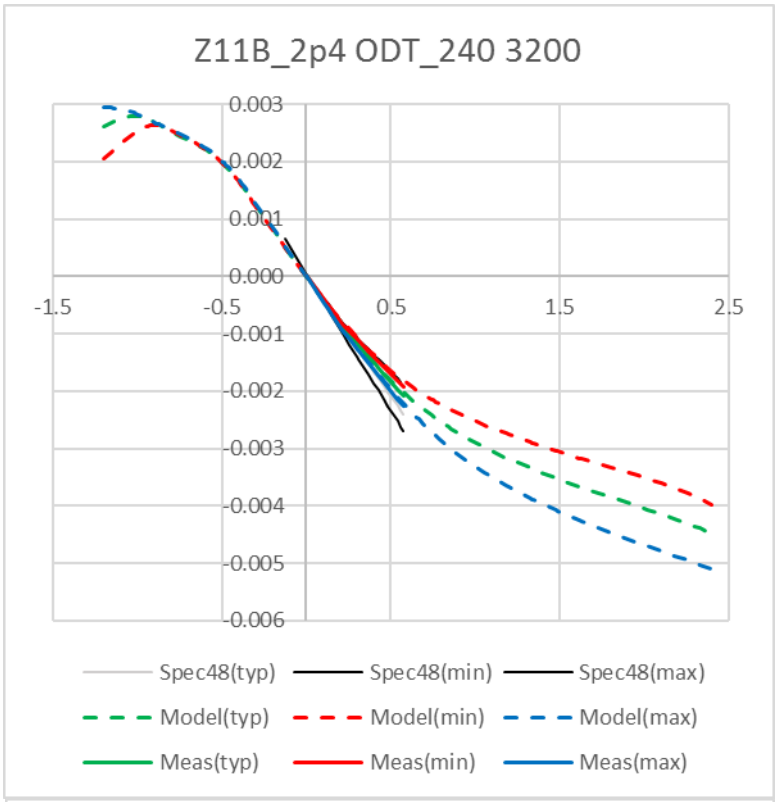


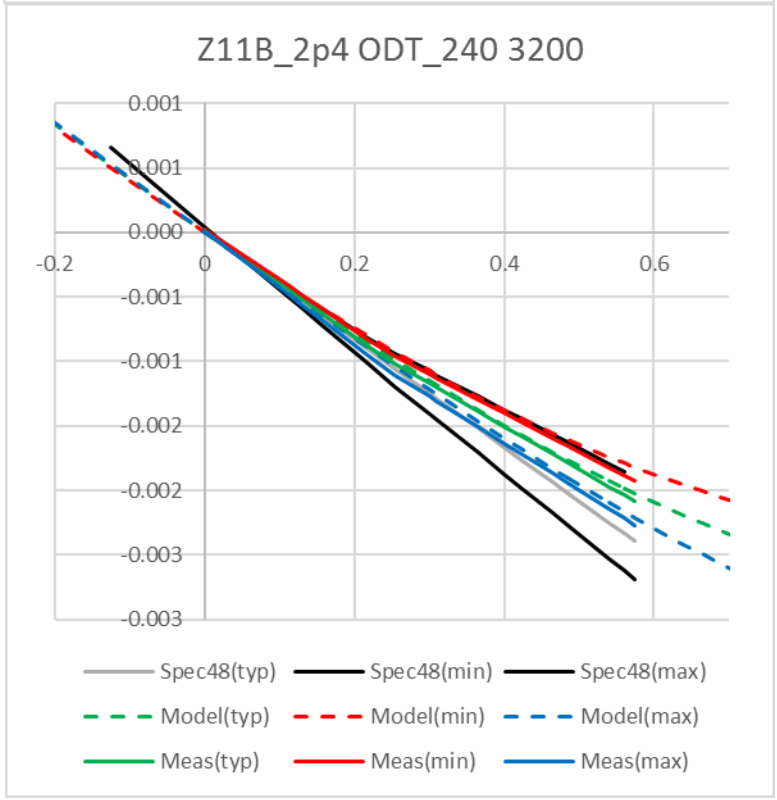
f. **ODT120**





g. **ODT240**

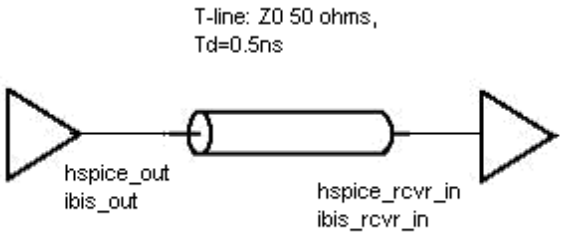




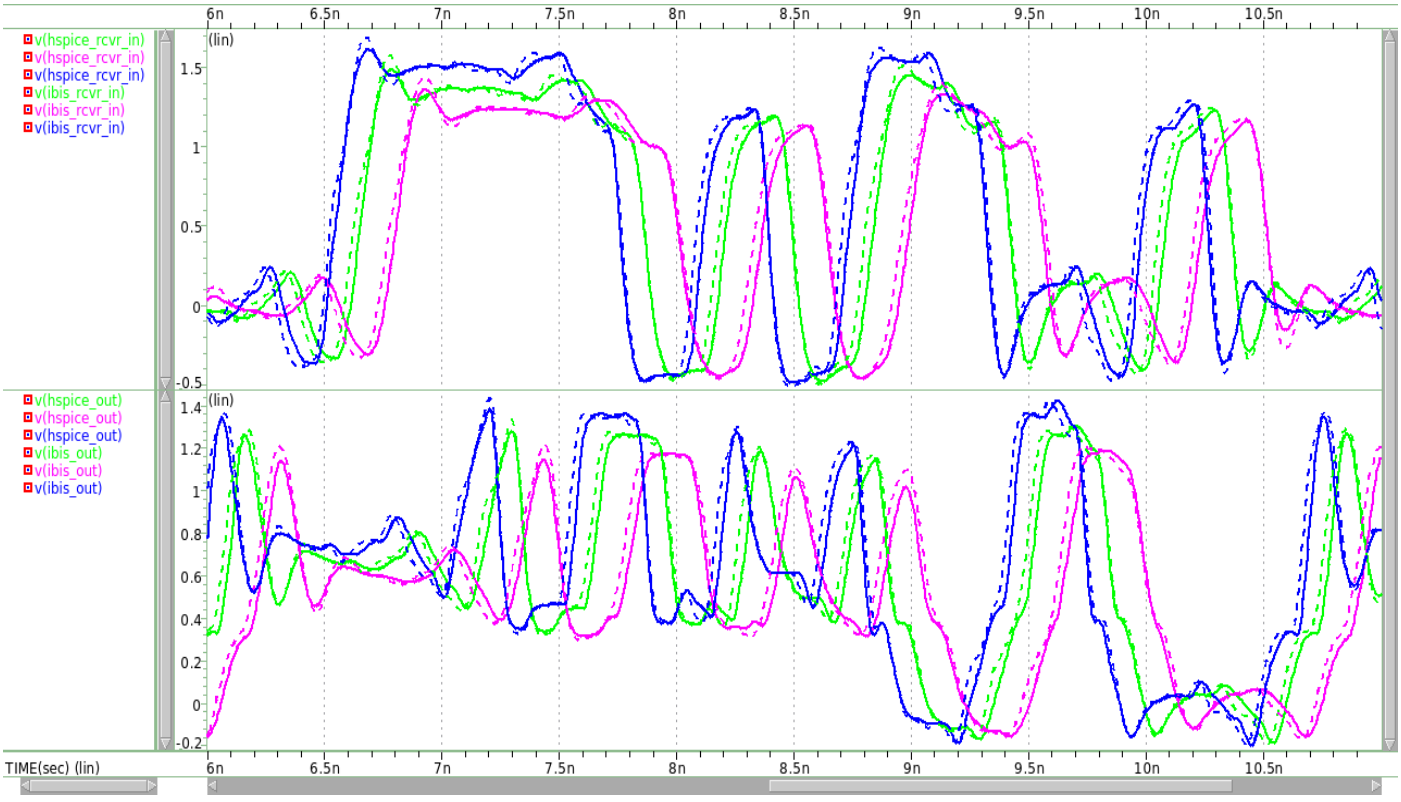
IBIS Model Correlation: IBIS vs Spice (Driver-Receiver)

1. ☒ For all Output or I/O models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element).
   a. ☒ Use the setup and node naming conventions shown below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations: **HSPICE 2016.03**
   b. ☒ Run simulations for all corners cases and at fastest speed grades, testing ODT models as loads when applicable

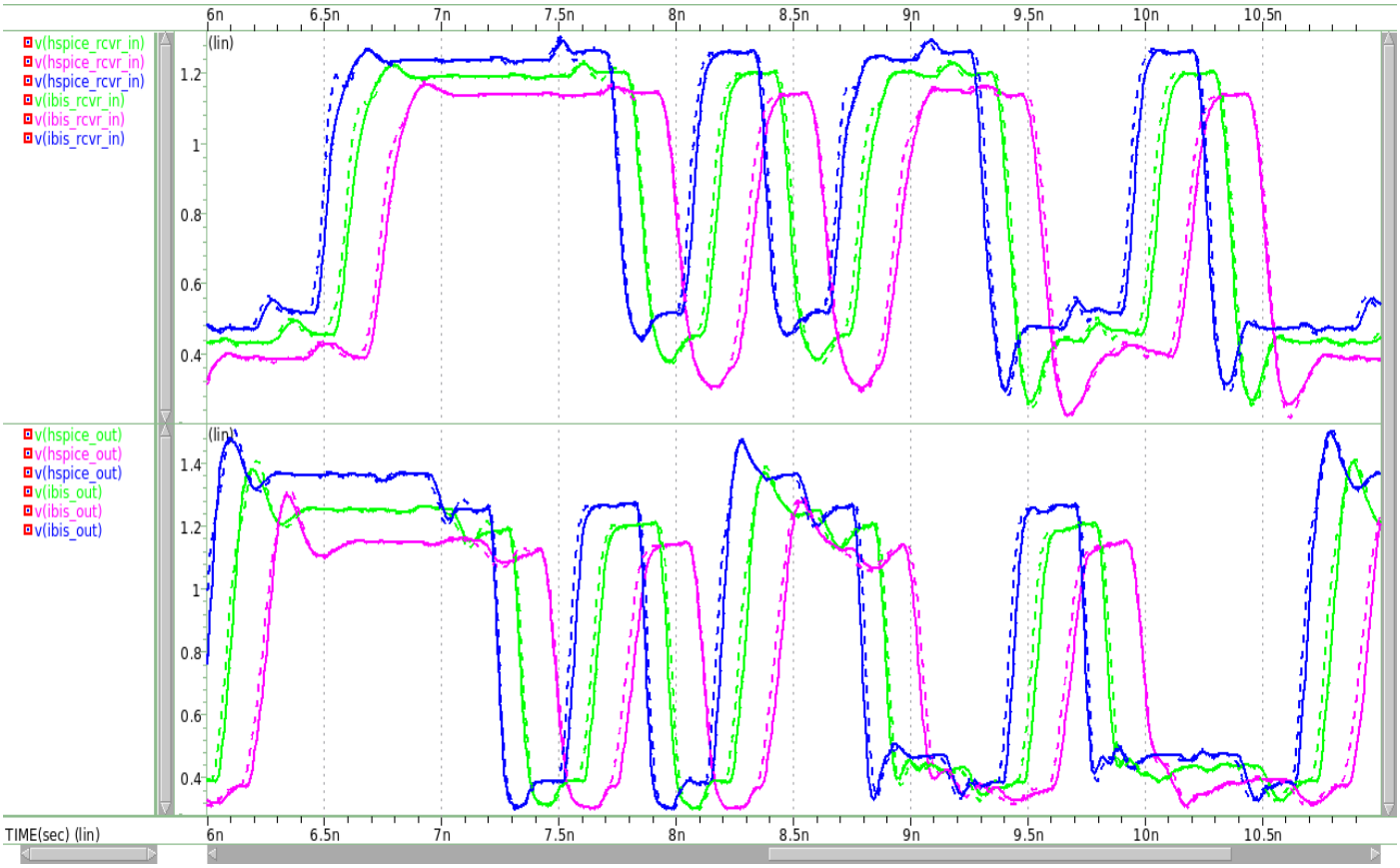
SETUP:



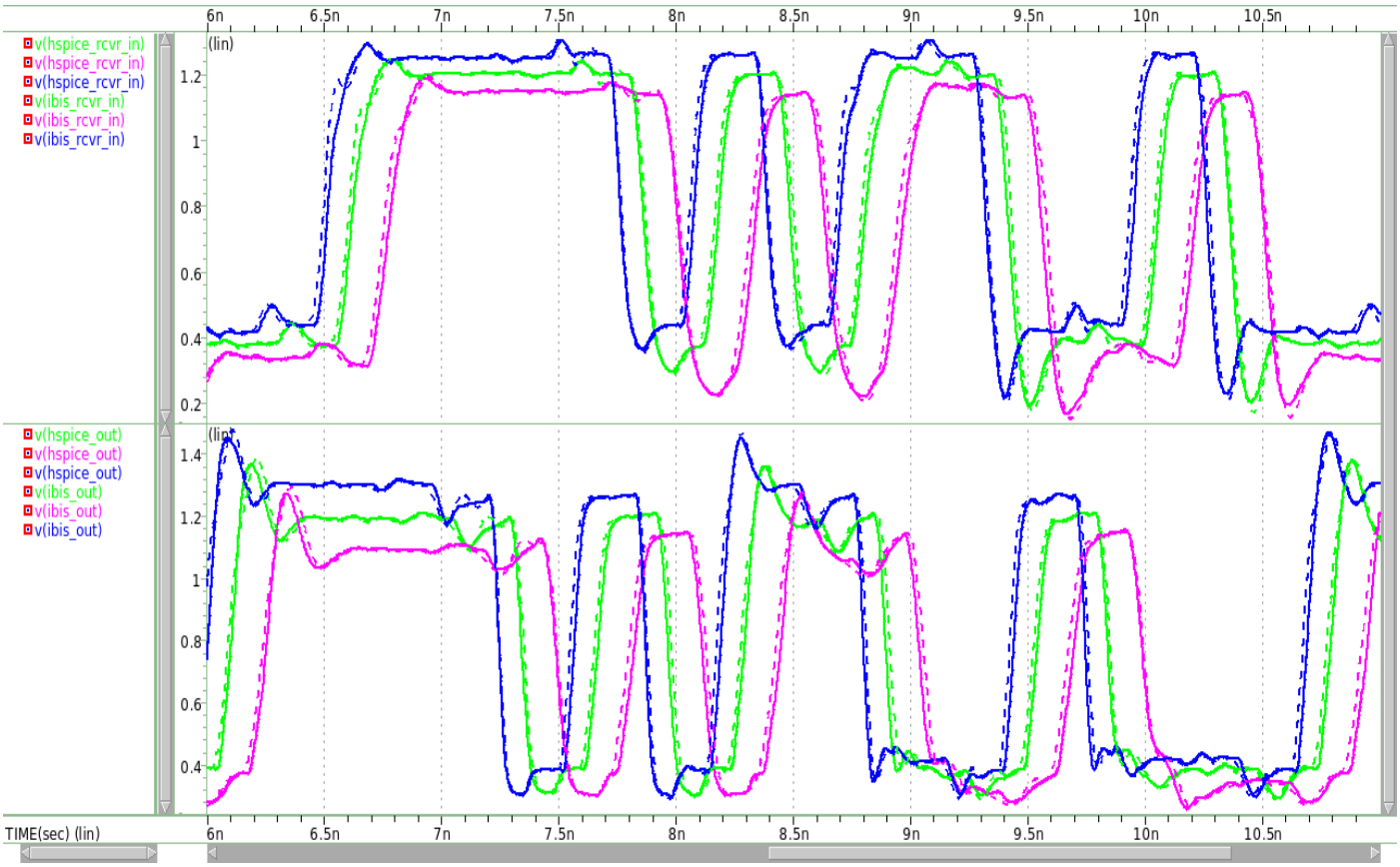
i. **DQ_34_3200** driving **DQ_34_3200**



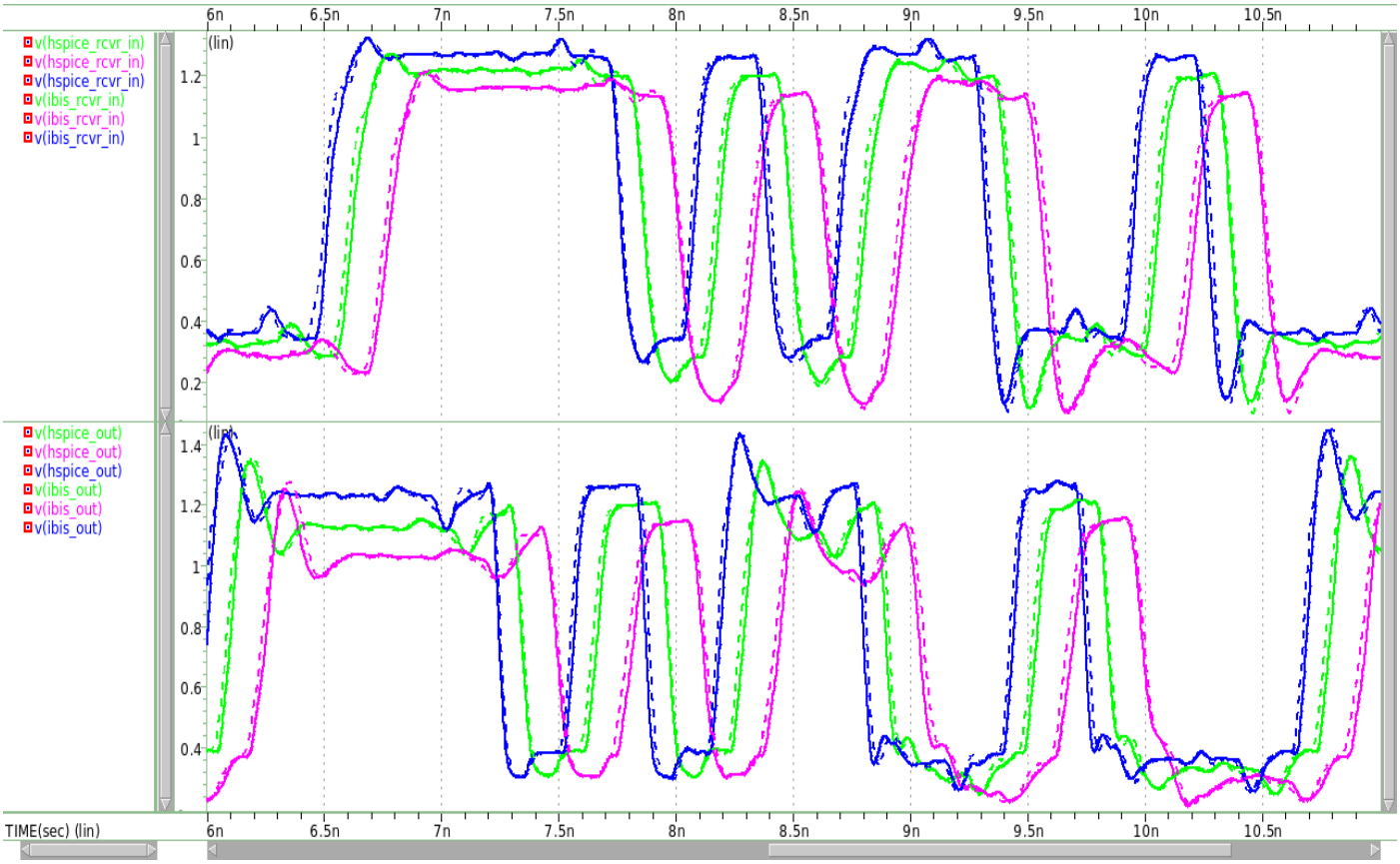
ii. **DQ_34_3200** driving **DQ_IN_ODT34_3200**



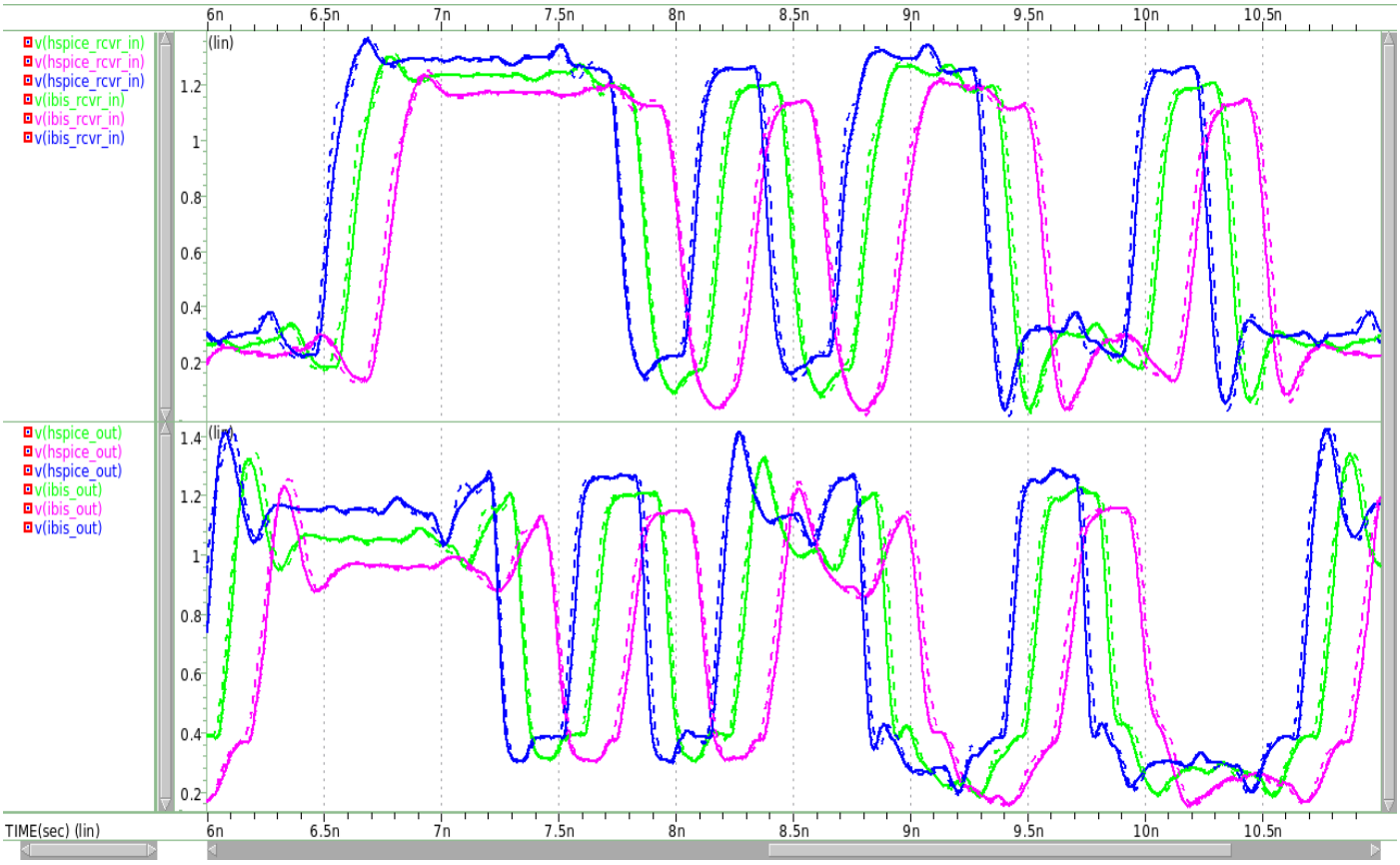
iii. **DQ_34_3200** driving **DQ_IN_ODT40_3200**



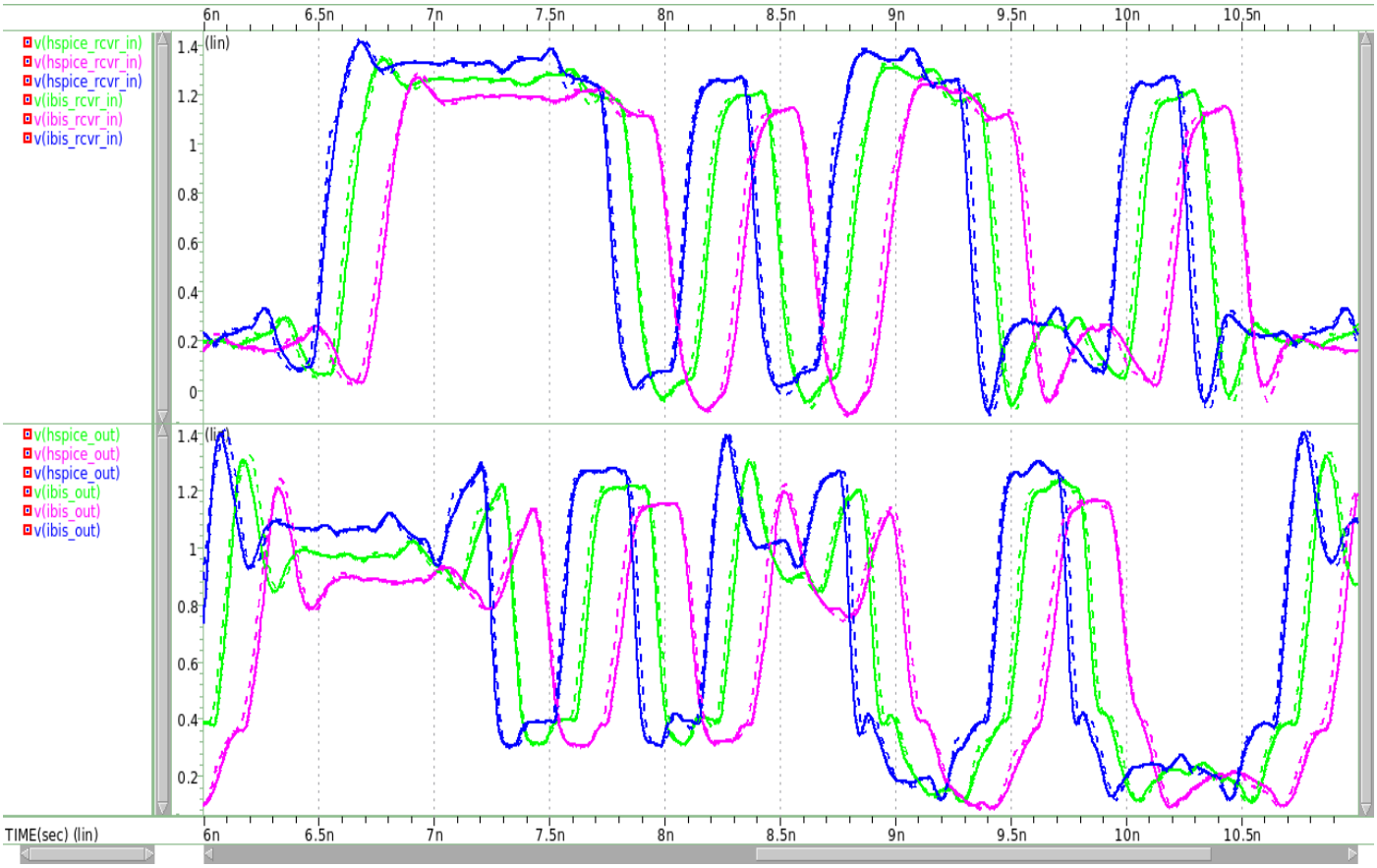
iv. **DQ_34_3200** driving **DQ_IN_ODT48_3200**



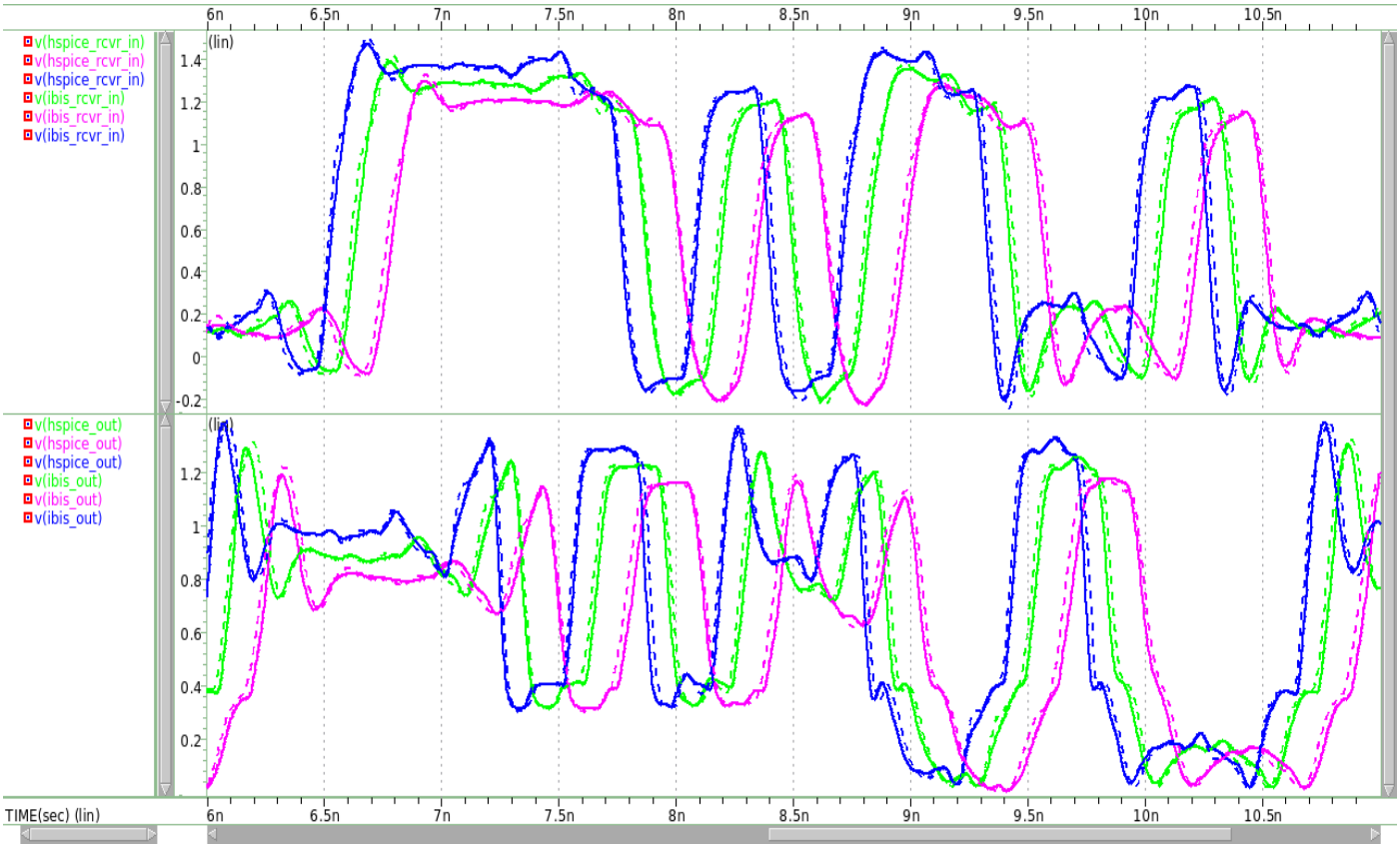
v. **DQ_34_3200** driving **DQ_IN_ODT60_3200**



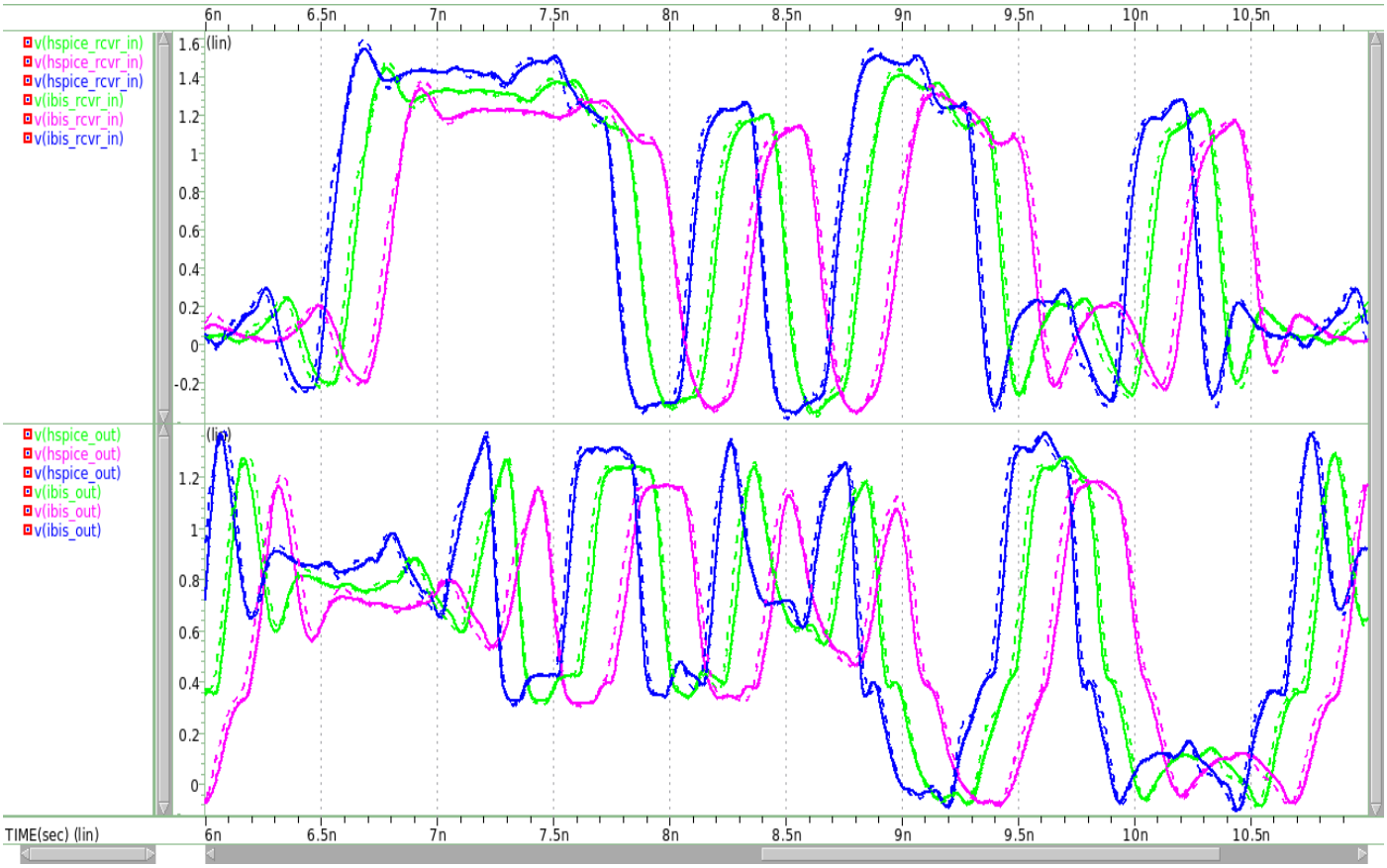
vi. **DQ_34_3200** driving **DQ_IN_ODT80_3200**



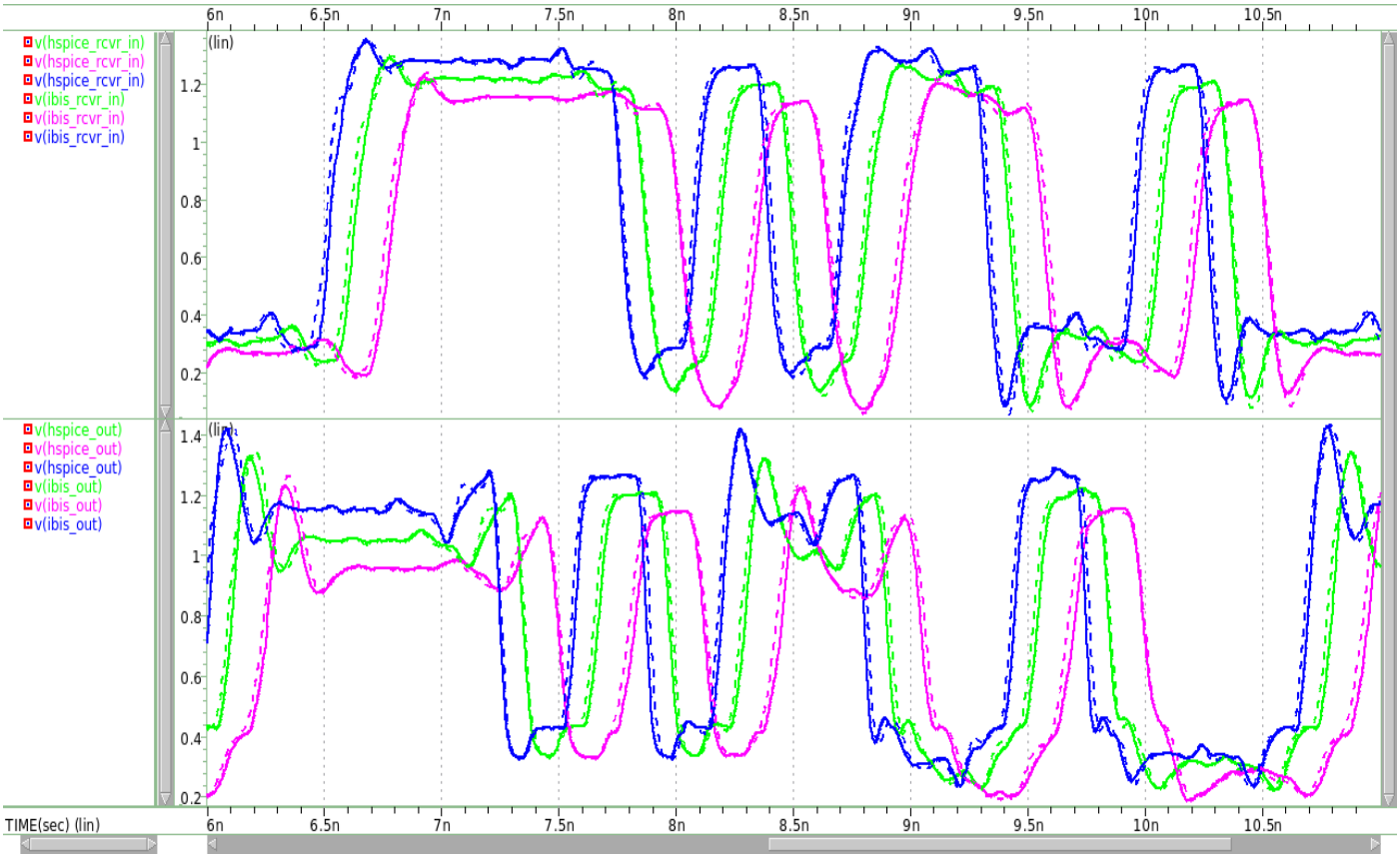
vii. **DQ_34_3200** driving **DQ_IN_ODT120_3200**



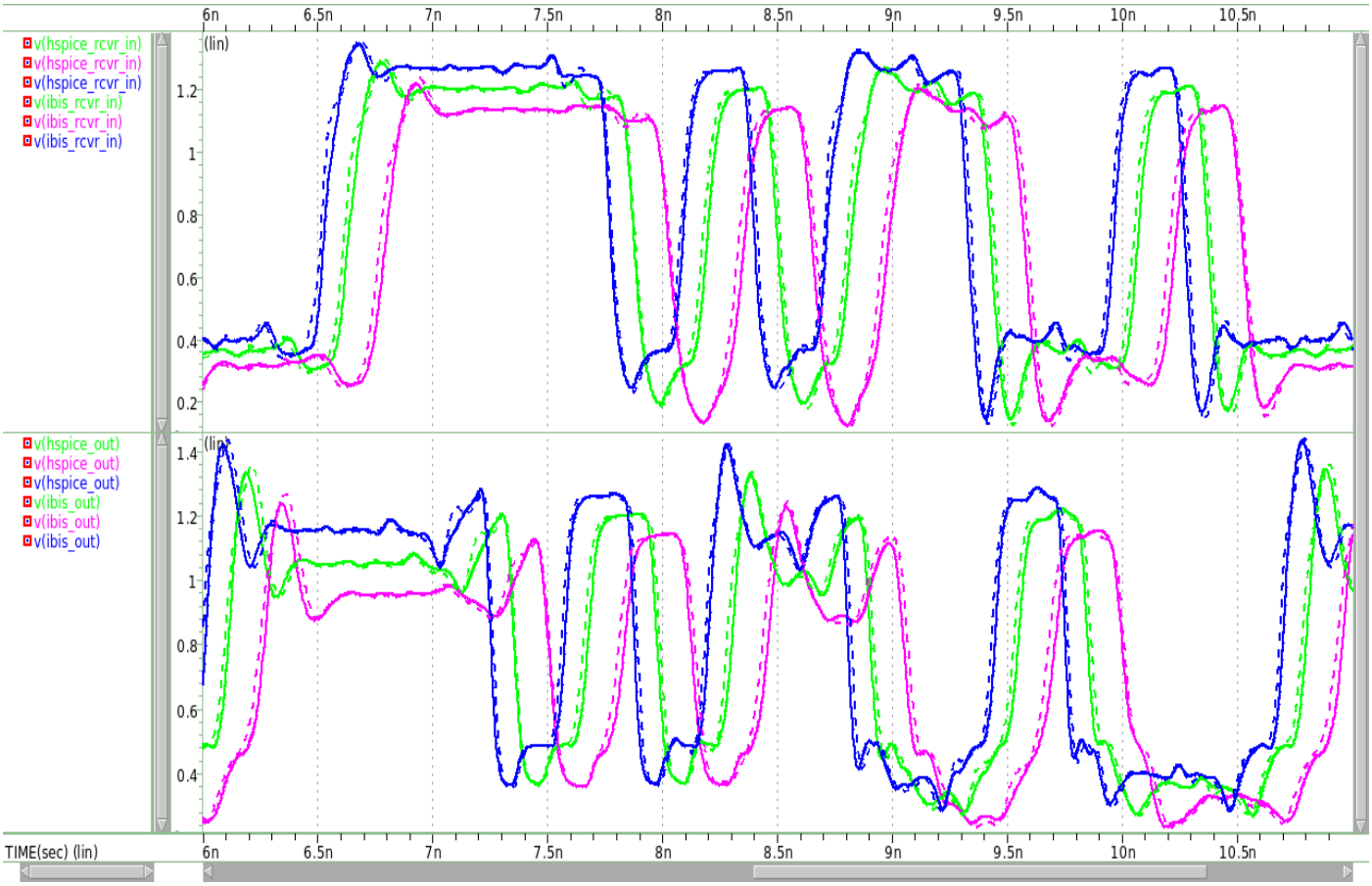
viii. **DQ_34_3200** driving **DQ_IN_ODT240_3200**



ix. **DQ_40_3200** driving **DQ_IN_ODT60_3200**



x. **DQ_48_3200** driving **DQ_IN_ODT60_3200**



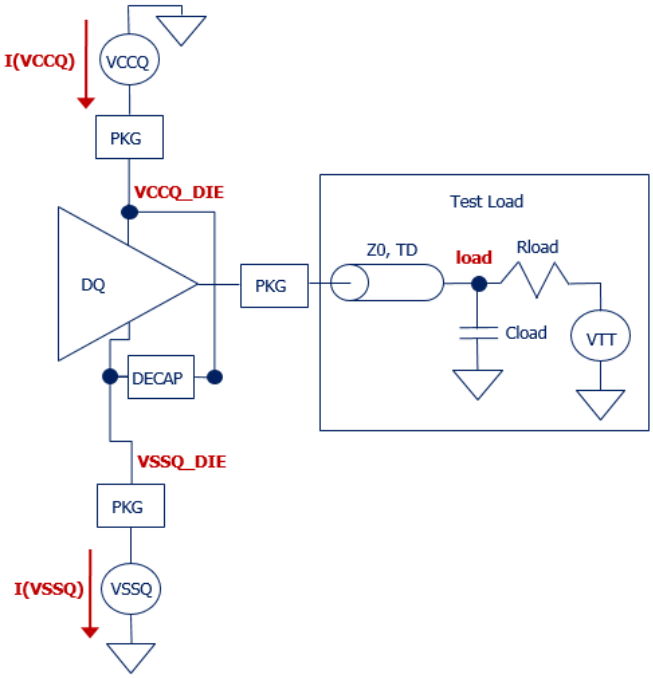
IBIS Model Correlation: IBIS vs Spice (Driver Load)

1. ☒ For all Output or I/O IBIS Version 5.0 power-aware models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element) with a non-ideal power supply connection.

   a. ☒ Use the setup and node naming conventions shown in Setup B below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations: **HSPICE 2016.03-1**

   b. ☒ Run simulations for all corner cases and at fastest speed grades

SETUP B:



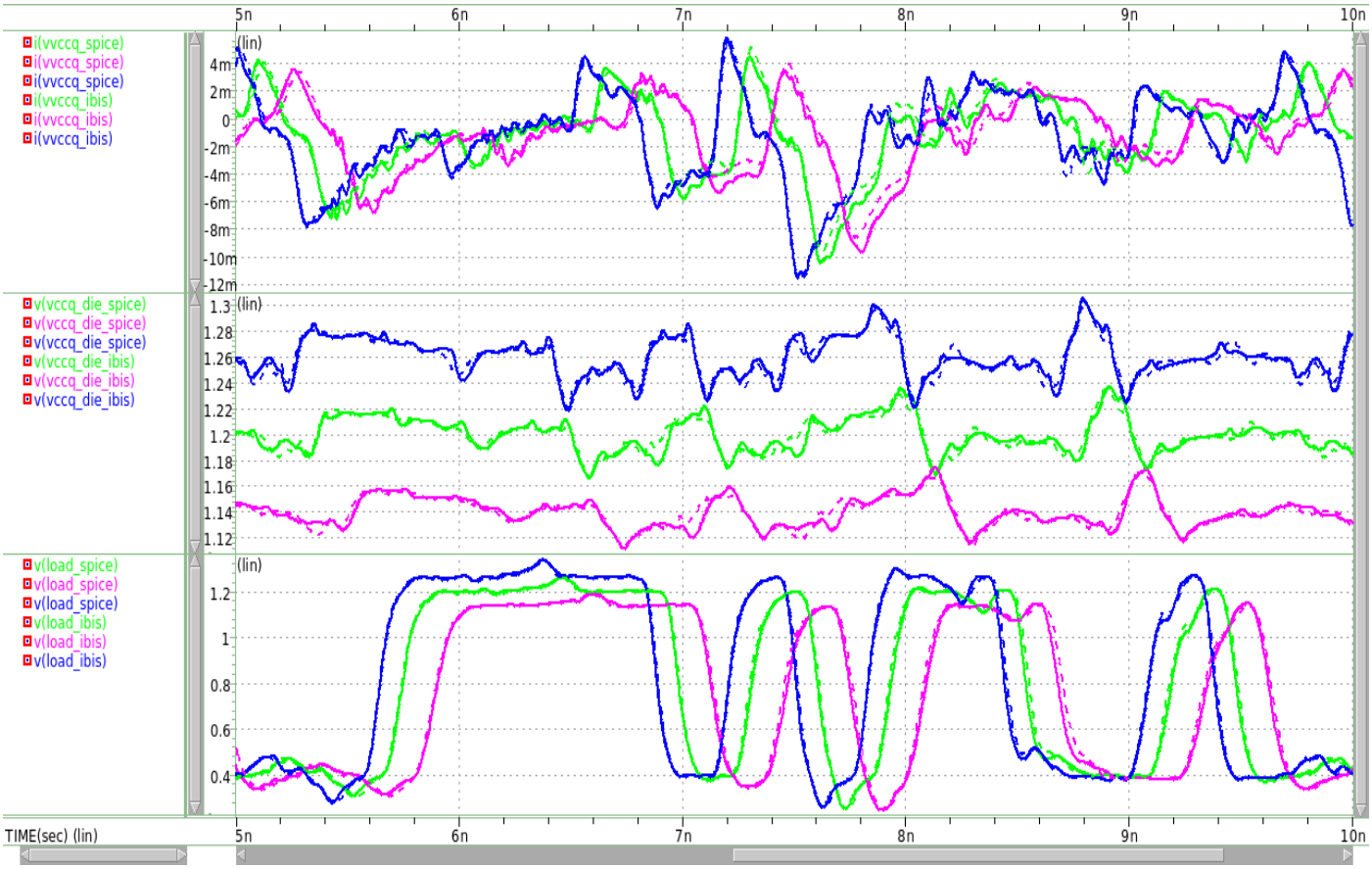
Test Load Values

Z0	=	50 Ω
Td	=	200 ps
Cload	=	5 pF
Rload	=	50 Ω
VTT	=	VDDQ

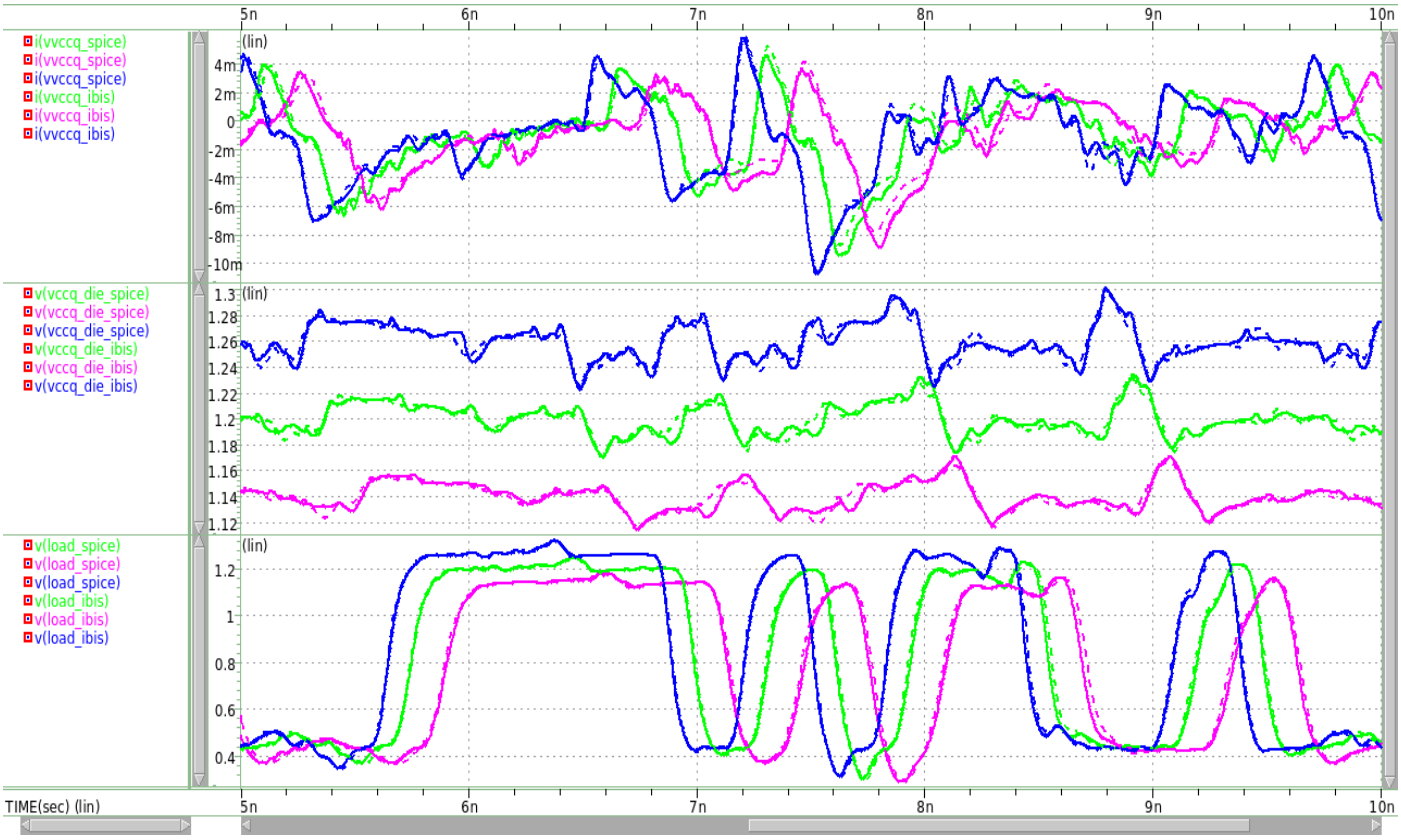
Package Model used for correlation

Lpkg	PAD	BALL	1.25n	0.25
Lpkg_vccq	vccq_die	vccq_ball	1.25n	0.25
Lpkg_vssq	vssq_die	vssq_ball	0.10n	0.05
K1	Lpkg_vccq	Lpkg_vssq	0.20	
K2	Lpkg	Lpkg_vccq	0.40	
K3	Lpkg	Lpkg_vssq	0.20	
Cpkg_vccq	BALL	vccq_ball	0.20p	
Cpkg_vssq	BALL	vssq_ball	0.20p	
Cpkg_vccq_vssq	vccq_ball	vssq_ball	0.40p	

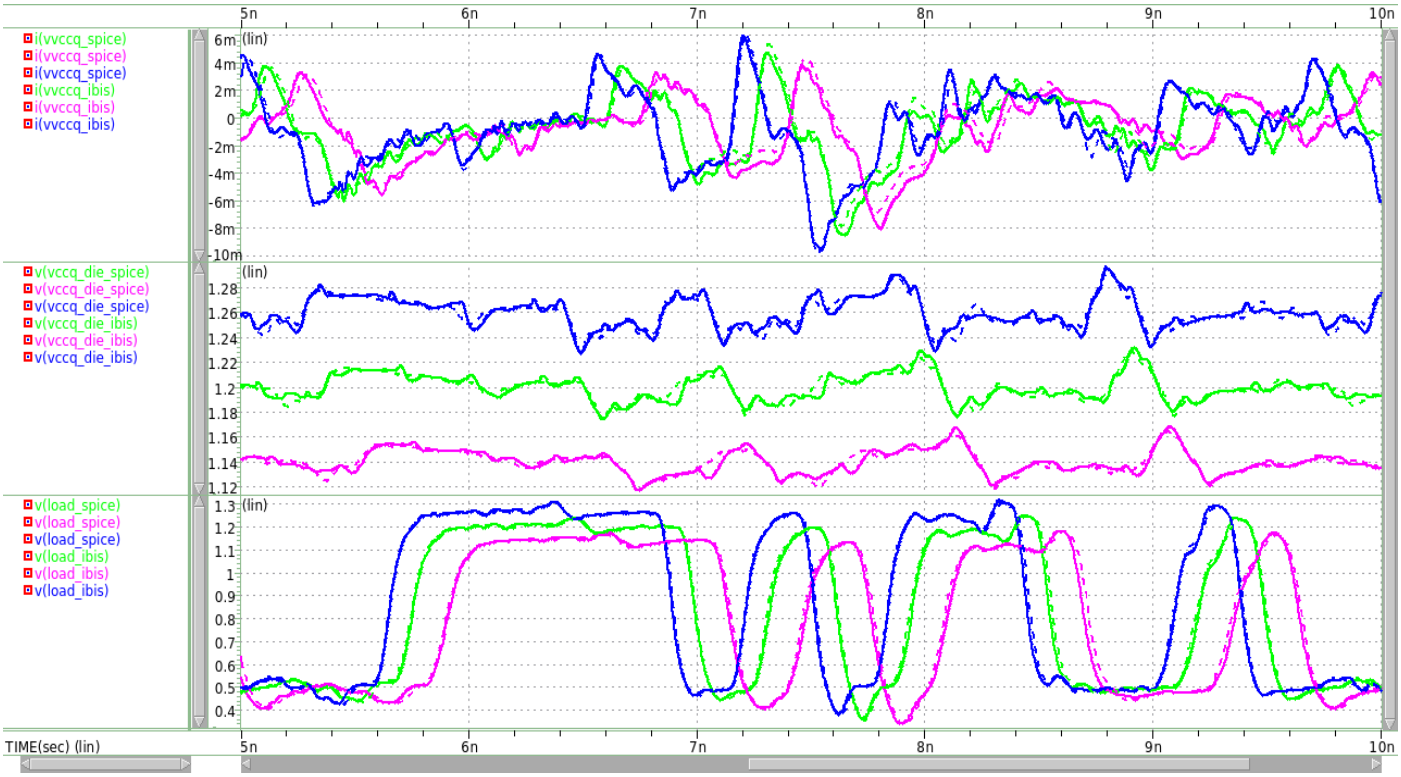
i. DQ_34_3200



ii. DQ_40_3200



iii. **DQ_48_3200**



Comments

1. **IBIS model may not reflect current speed grade availability.**
2. **C_comp is compared with the DDR4-2666 specification only.**
3. **Slew rate is based on HSPICE simulation with a 50ohm load to VDDQ. This includes simple package parasitics for pin and power/gnd nets**

Document Revision History

Rev **2.9.2** - Date **February 27, 2023**
- a. IBIS revision (Version 5.0) **2.9.2**

Rev **2.9.1** - Date **August 12, 2022**
- b. IBIS revision (Version 5.0) **2.9.1**
- c. HSPICE revision **2.7.1**

Rev **2.8.2** - Date **January 11, 2021**
- d. IBIS revision (Version 5.0) **2.8.1**
- e. HSPICE revision **2.7.1**

Rev **2.8.1** - Date **August 20, 2020**
- f. IBIS revision (Version 5.0) **2.8.1**
- g. HSPICE revision **2.7.1**

Rev **2.7** - Date **May 7, 2020**
- h. IBIS revision (Version 5.0) **2.7**
- i. HSPICE revision **2.7**

