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## **IBIS/HSpice Model Quality Report**

Design ID: **U88B**

Description: **1Gb x4, x8, x16 DDR2 SDRAM**

Marketing device name(s): **MT47H256M4SH, MT47H128M8SH, MT47H64M16NF, MT47H256M4U88B, MT47H128M8U88B, MT47H64M16U88B**

Valid speed grades: **DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066**

Zip filename: **u88b\_auto\_ibis.zip**

IBIS filename: **u88b\_ait.ibs, u88b\_aat.ibs, u88b\_aut.ibs** File rev: **2.2**

HSpice filename: **u88b\_auto\_hspice.zip** File rev: **2.1**

EBD filename (if applicable): File rev:

Die rev: **M**

Date: **February 5, 2016**

Datasheet link: [http://www.micron.com/~/media/documents/products/data-sheet/dram/ddr2/u88b\\_1gb\\_ddr2\\_ait\\_aat.pdf](http://www.micron.com/~/media/documents/products/data-sheet/dram/ddr2/u88b_1gb_ddr2_ait_aat.pdf)

[http://www.micron.com/~/media/documents/products/data-sheet/dram/ddr2/1gb\\_ddr2\\_automotive\\_aut\\_addendum.pdf](http://www.micron.com/~/media/documents/products/data-sheet/dram/ddr2/1gb_ddr2_automotive_aut_addendum.pdf)

E-mail [modelsupport@micron.com](mailto:modelsupport@micron.com) for questions regarding Quality Report.

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### **Device Parameters**

VDDQ – Slow: **1.7V** Typical: **1.8V** Fast: **1.9V**

VDD – Slow: **1.7V** Typical: **1.8V** Fast: **1.9V**

Junction Temperature (Automotive Industrial) - Slow: **110C** Typical: **50C** Fast: **-40C**

Junction Temperature (Automotive) - Slow: **120C** Typical: **50C** Fast: **-40C**

Junction Temperature (Automotive Ultra-high) - Slow: **140C** Typical: **50C** Fast: **-40C**

VDDQ/VSSQ Decoupling Capacitance: **9.89nF**

Included in HSPICE DQ/DQS models? **Yes** Amount per DQ/DQS model: **430pF/860pF**

VDDQ/VSSQ Decoupling Capacitance Series Resistance: **~2 ohms**

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### **IBIS Quality Summary**

1. ☒ Include the IBIS Quality Specification 2.0 Overall IBIS Quality level. For details on IBIS Quality, reference the quality specification and quality checklist on IBIS quality webpage [http://www.eda.org/pub/ibis/quality\\_wip/](http://www.eda.org/pub/ibis/quality_wip/).

Overall IBIS Quality Level: **IQ3MSX**

Exceptions: **Overshoot parameters not available from datasheet, Tslew\_ac/Tdiffslew\_ac not available from datasheet set high**

2. ☒ Include the filename of the IBIS Quality Checklist that accompanies this report.

Filename: [u88b\\_auto\\_ibis\\_quality\\_checklist.xls](#)

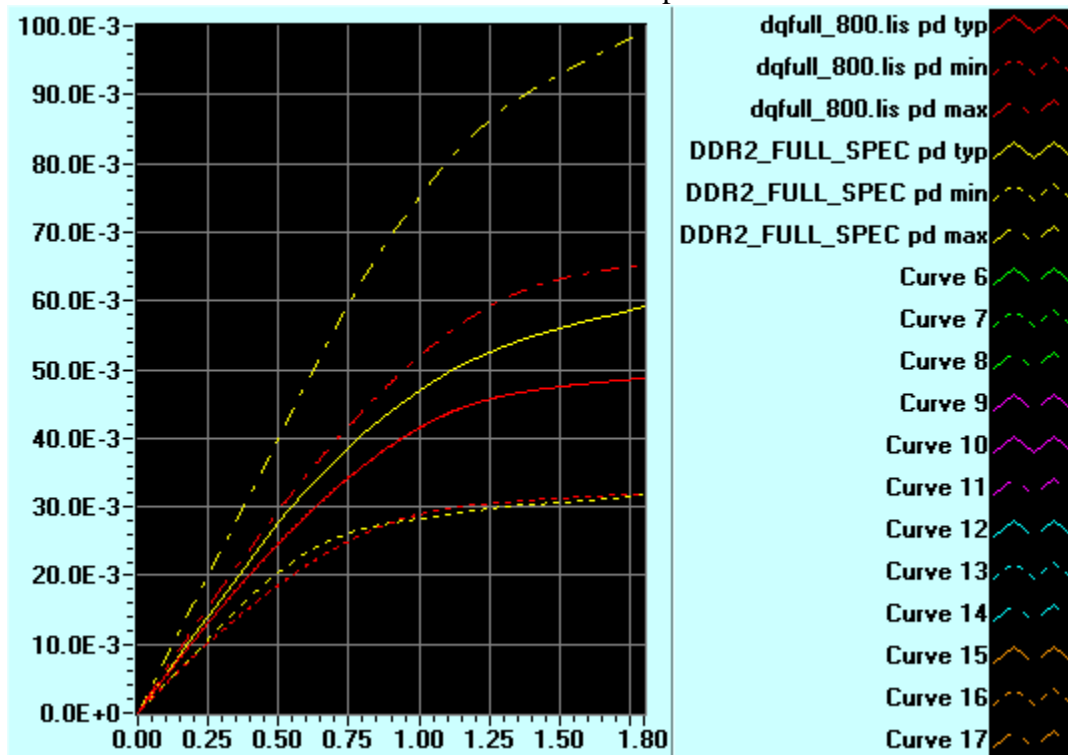
## IBIS MODEL Correlation

### Datasheet Correlation

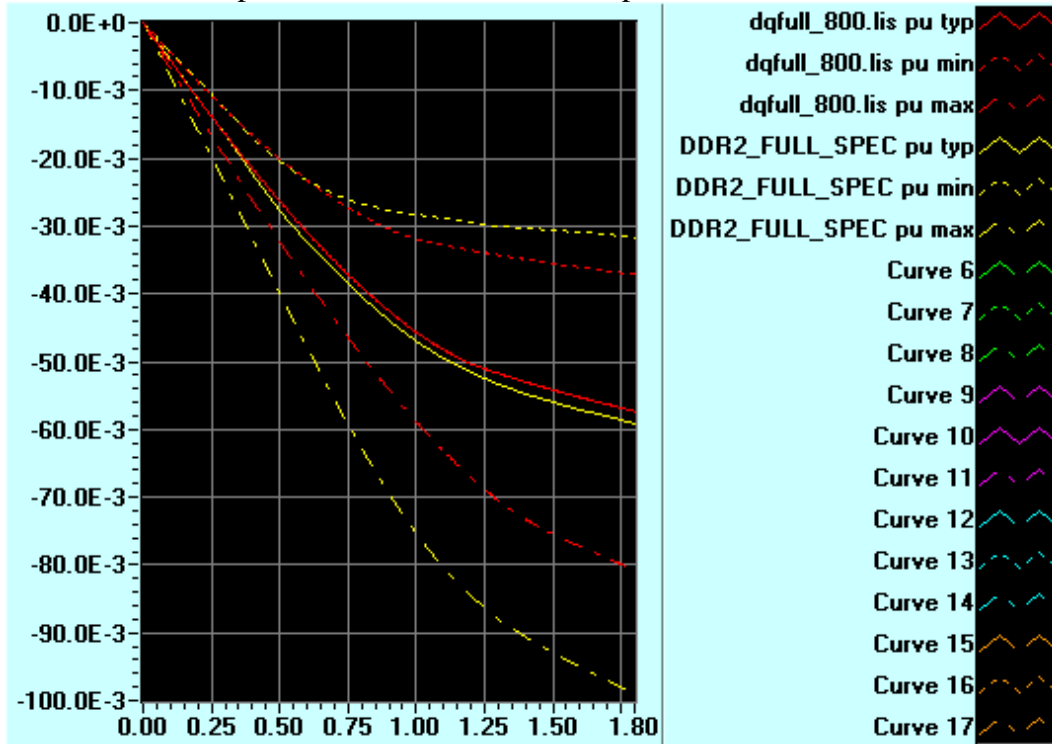
1. ☒ For Output or I/O model compare datasheet IOH/IOL data with IBIS pullup/pulldown data.

a. Model name: [DQ\\_FULL\\_800](#)

i. Pulldown I-V versus [JEDEC DDR2](#) specification

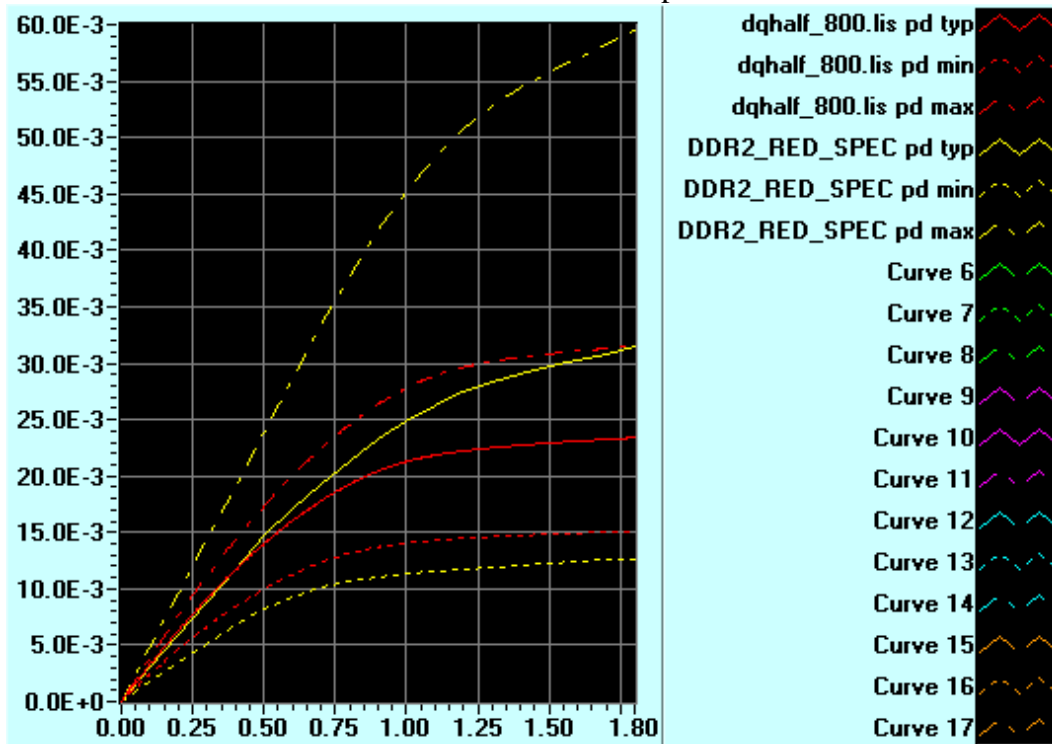


ii. Pullup I-V versus JEDEC DDR2 specification

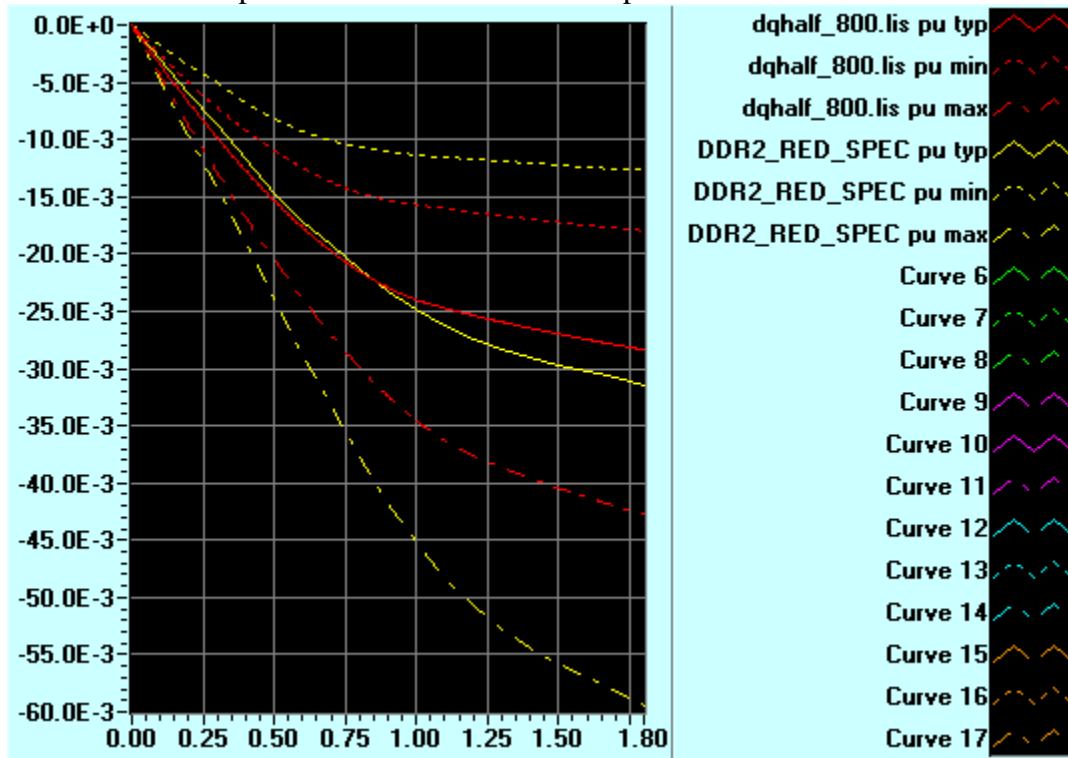


b. Model name: **DQ\_HALF\_800**

i. Pulldown I-V versus JEDEC DDR2 specification



ii. Pullup I-V versus JEDEC DDR2 specification



2. ☒ Compare C\_comp with datasheet Input C. Provide C\_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16).

Component name: **MT47H256M4SH, MT47H128M8SH (60-Ball x4/x8)**

		IBIS		Datasheet	
		Min	max	min	max
DQ	C_comp	2.30	2.45	NA	NA
	C package	0.28	0.54	NA	NA
	C_total	2.58	2.99	2.50	4.00
INPUT	C_comp	1.00	1.10	NA	NA
	C package	0.20	0.40	NA	NA
	C_total	1.20	1.50	1.00	2.00
CLK	C_comp	0.98	1.08	NA	NA
	C package	0.28	0.31	NA	NA
	C_total	1.26	1.39	1.00	2.00

Component name: **MT47H64M16NF (84-Ball x16)**

		IBIS		Datasheet	
		min	max	min	max
<b>DQ</b>	C_comp	2.30	2.45	NA	NA
	C_package	0.28	0.54	NA	NA
	C_total	2.58	2.99	2.50	4.00
<b>INPUT</b>	C_comp	1.00	1.10	NA	NA
	C_package	0.24	0.44	NA	NA
	C_total	1.24	1.54	1.00	2.00
<b>CLK</b>	C_comp	0.98	1.08	NA	NA
	C_package	0.33	0.35	NA	NA
	C_total	1.30	1.43	1.00	2.00

3. ☒ If slew rate specifications (rise/fall slew) are available from the datasheet, complete Spice simulations to generate slew rate data and provide a comparison table.

		IBIS			Datasheet	
Model	Slew Rate (V/ns)	min	typ	max	min	max
<b>DQ Full</b>	Rising	1.537	2.928	4.915	1.500	5.000
	Falling	1.532	2.900	5.286	1.500	5.000
<b>DQ Half</b>	Rising	1.058	2.075	3.707	1.500	5.000
	Falling	0.916	1.945	3.719	1.500	5.000

4. ☒ Compare ODT data with datasheet.

ODT calculated using the formula  $RTT = (V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IH(ac)}) - I(V_{IL(ac)}))$

ODT50	TYP	SLOW	FAST
Vil (V)	0.65	0.60	0.70
Vih (V)	1.15	1.10	1.20
Ivil (A)	-4.71E-03	-4.14E-03	-5.71E-03
Ivih (A)	4.86E-03	4.33E-03	5.93E-03
	TYP	SLOW	FAST
Rtt (Model) (ohms)	52.24	59.01	42.97
Rtt (datasheet) (ohms)	50	60	40

ODT75	TYP	SLOW	FAST
Vil (V)	0.65	0.60	0.70
Vih (V)	1.15	1.10	1.20
Ivil (A)	-3.14E-03	-2.76E-03	-3.81E-03
Ivih (A)	3.24E-03	2.89E-03	3.95E-03
	TYP	SLOW	FAST
Rtt (Model) (ohms)	78.36	88.52	64.45
Rtt (datasheet) (ohms)	75	90	60

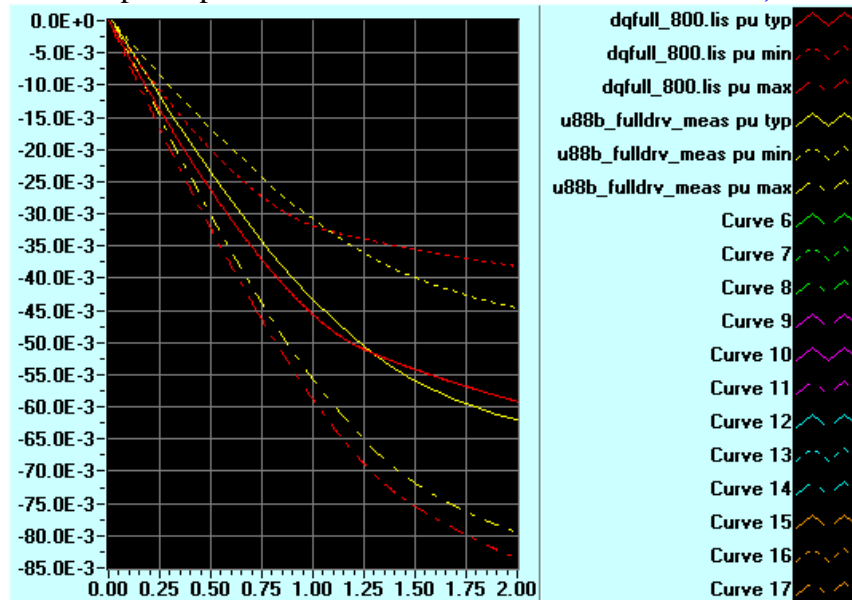
ODT150	TYP	SLOW	FAST
Vil (V)	0.65	0.60	0.70
Vih (V)	1.15	1.10	1.20
Ivil (A)	-1.57E-03	-1.38E-03	-1.90E-03
Ivih (A)	1.62E-03	1.44E-03	1.97E-03
	TYP	SLOW	FAST
Rtt (Model) (ohms)	156.73	177.05	128.91
Rtt (datasheet) (ohms)	150	180	120

## Measurement Correlation

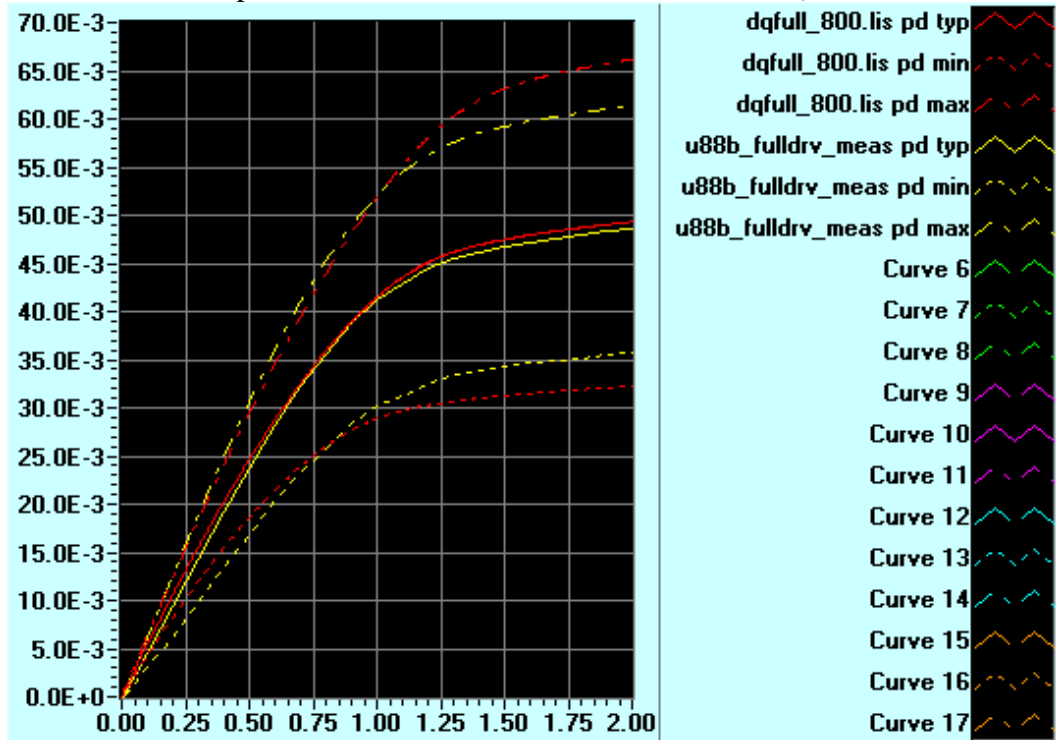
1. ☒ For Output or I/O models compare measured IOH/IOL data with IBIS pullup/pulldown data. If the measurement conditions are different than the IBIS conditions, run Spice simulations using the same measurement conditions such as VCC, temperature, and process. Include measurement conditions in the image labels.

a. Model name: **DQ\_FULL\_800**

i. Pullup comparison. Measurement conditions: **-5C/1.7V, 88C/1.9V**

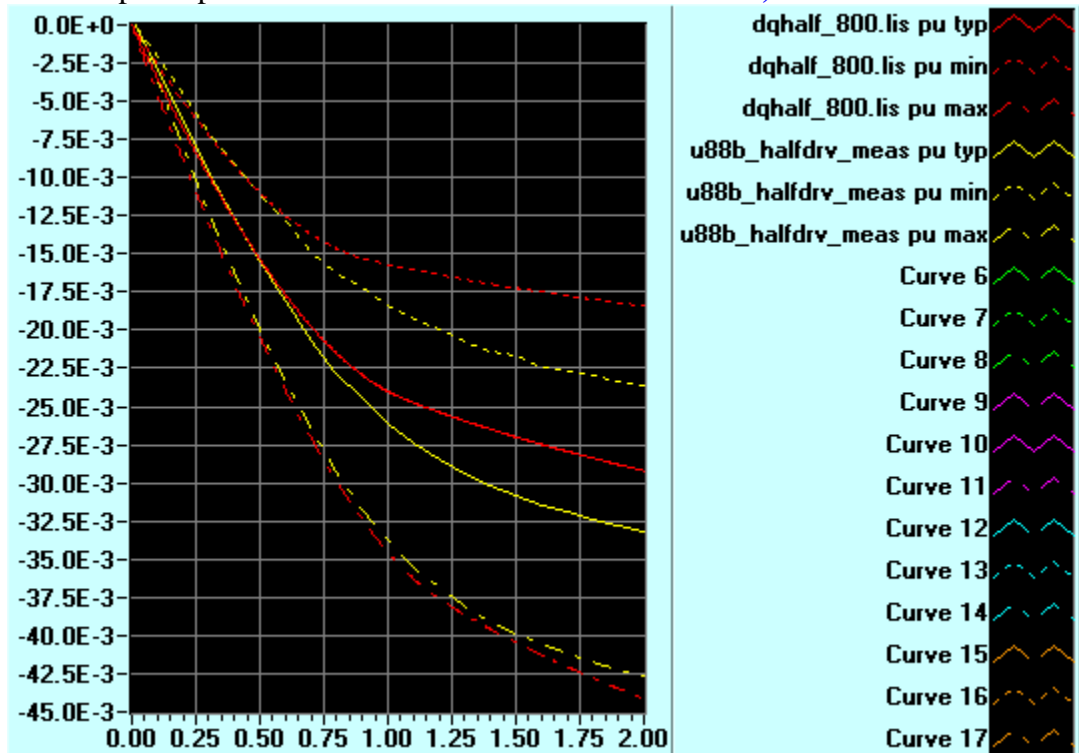


ii. Pulldown comparison. Measurement conditions: **-5C/1.7V, 88C/1.9V**

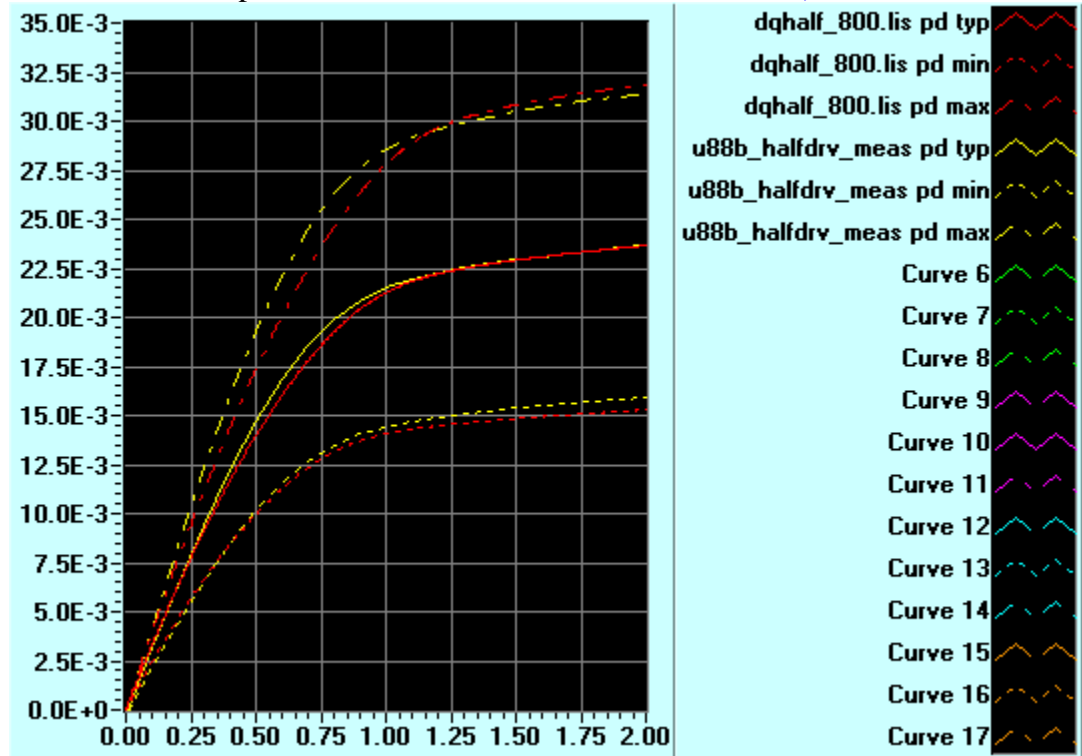


b. Model name: **DQ\_HALF\_800**

i. Pullup comparison. Measurement conditions: **-5C/1.7V, 88C/1.9V**



ii. Pulldown comparison. Measurement conditions: **-5C/1.7V, 88C/1.9V**



2. ☒ Compare C\_comp with measured C\_comp. Provide C\_comp comparison table for all models and for all package combinations (i.e x4, x8 and x16).

Component name: **MT47H128M8SH**

		IBIS			Measured		
		min	Typ	max	min	typ	max
DQ	C_comp	2.30	2.38	2.45	NA	NA	NA
	C package	0.28	0.40	0.54	NA	NA	NA
	C_total	2.58	2.78	2.99	2.67	2.83	3.02
INPUT	C_comp	1.00	1.05	1.10	NA	NA	NA
	C package	0.20	0.30	0.40	NA	NA	NA
	C_total	1.20	1.35	1.50	1.24	1.34	1.50
CLK	C_comp	0.98	1.03	1.08	NA	NA	NA
	C package	0.28	0.30	0.31	NA	NA	NA
	C_total	1.26	1.32	1.39	1.31	1.34	1.37



3. ☒ If measured ODT data is available, provide an IBIS versus measurement comparison.

ODT50	TYP	SLOW	FAST
Rtt (Model) (ohms)	52.24	59.01	42.97
Rtt (Measurement) (ohms)	53.50	61.00	46.00

ODT75	TYP	SLOW	FAST
Rtt (Model) (ohms)	78.36	88.52	64.45
Rtt (Measurement) (ohms)	78.20	87.00	68.00

ODT150	TYP	SLOW	FAST
Rtt (Model) (ohms)	156.73	177.05	128.91
Rtt (Measurement) (ohms)	151.00	172.00	134.00

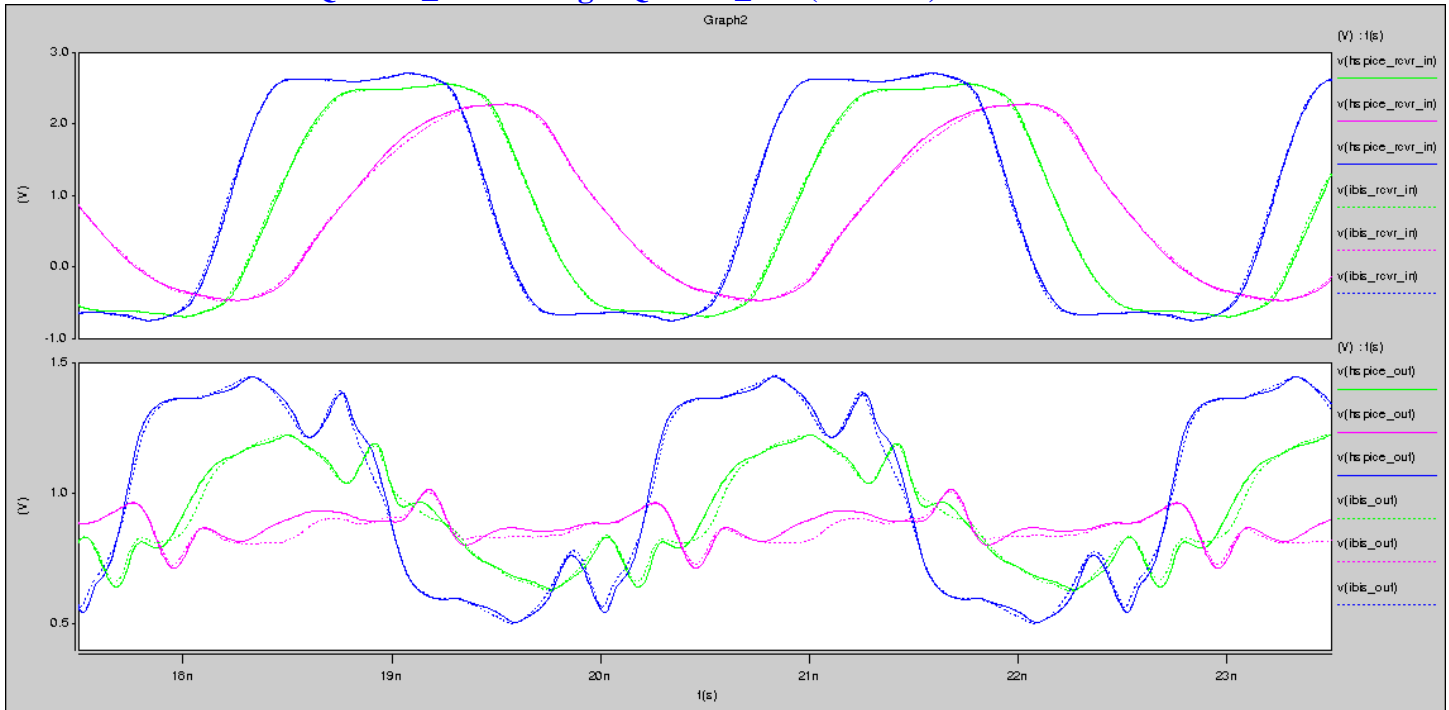
4. ☒ If slew rate data (rise/fall slew) is available from measurements, complete Spice simulations to generate slew rate data and provide a comparison table.

Model	Slew Rate (V/ns)	IBIS			Measurement	
		min	typ	max	min	max
DQ_FULL	Rising	1.801	2.297	2.950	1.832	3.125
	Falling	1.829	2.286	2.853	1.846	3.017
DQ_HALF	Rising	1.271	1.641	2.032	1.180	2.151
	Falling	1.225	1.536	1.883	1.147	2.113

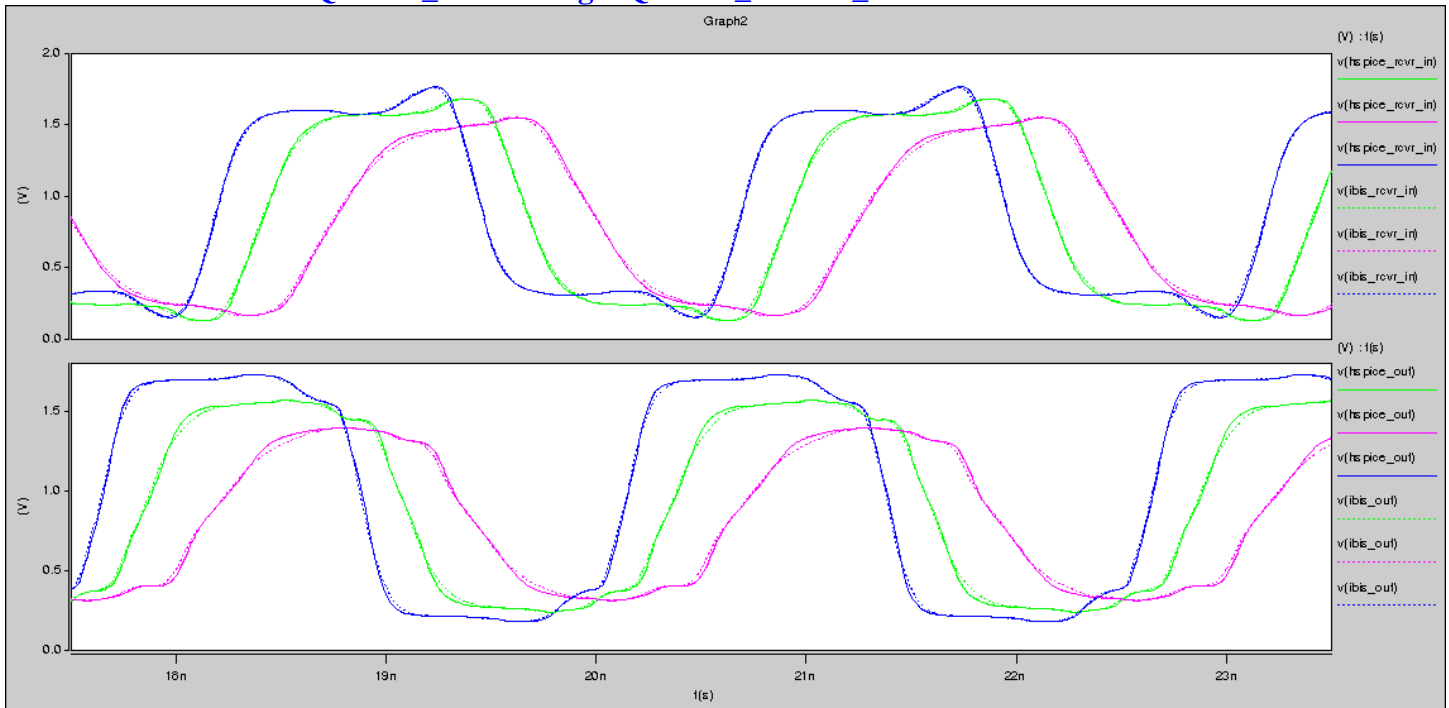
## IBIS vs Spice Correlation

1. ☒ For all Output or I/O models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element).
  - a. ☒ Use the setup and node naming conventions shown below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations: **HSpice 2013.03-SP1**
  - b. ☒ Run simulations for all corners cases and at fastest speed grades, testing ODT models as loads when applicable.

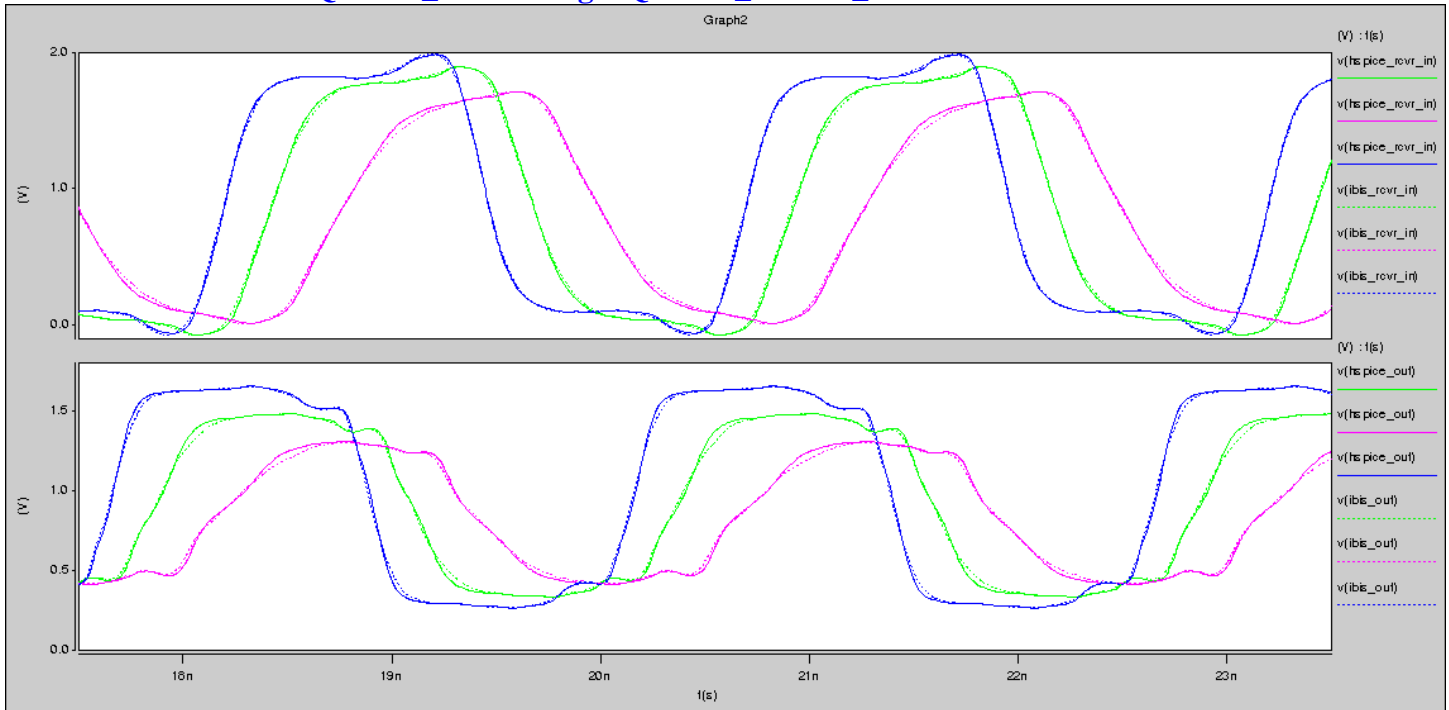
i. DQFULL\_800 driving DQFULL\_800 (no ODT)



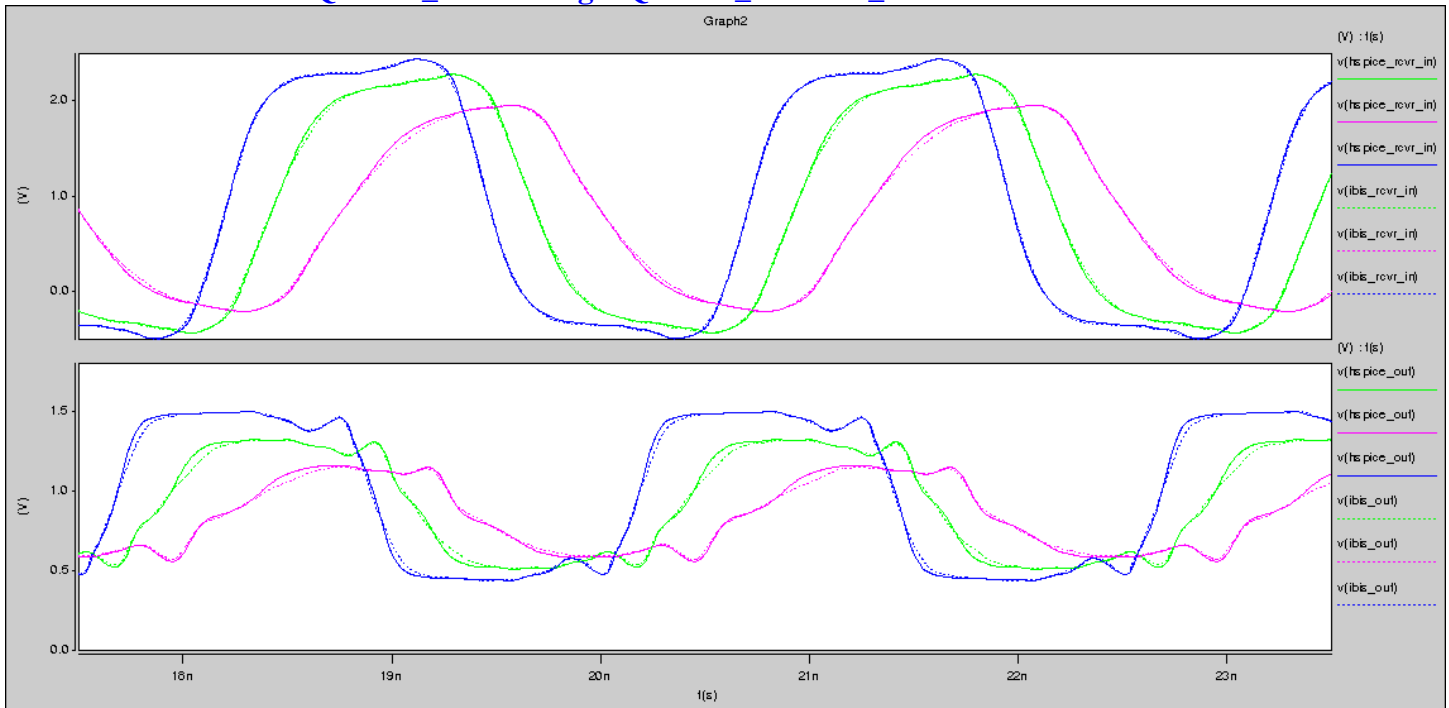
ii. DQFULL\_800 driving DQFULL\_ODT50\_800



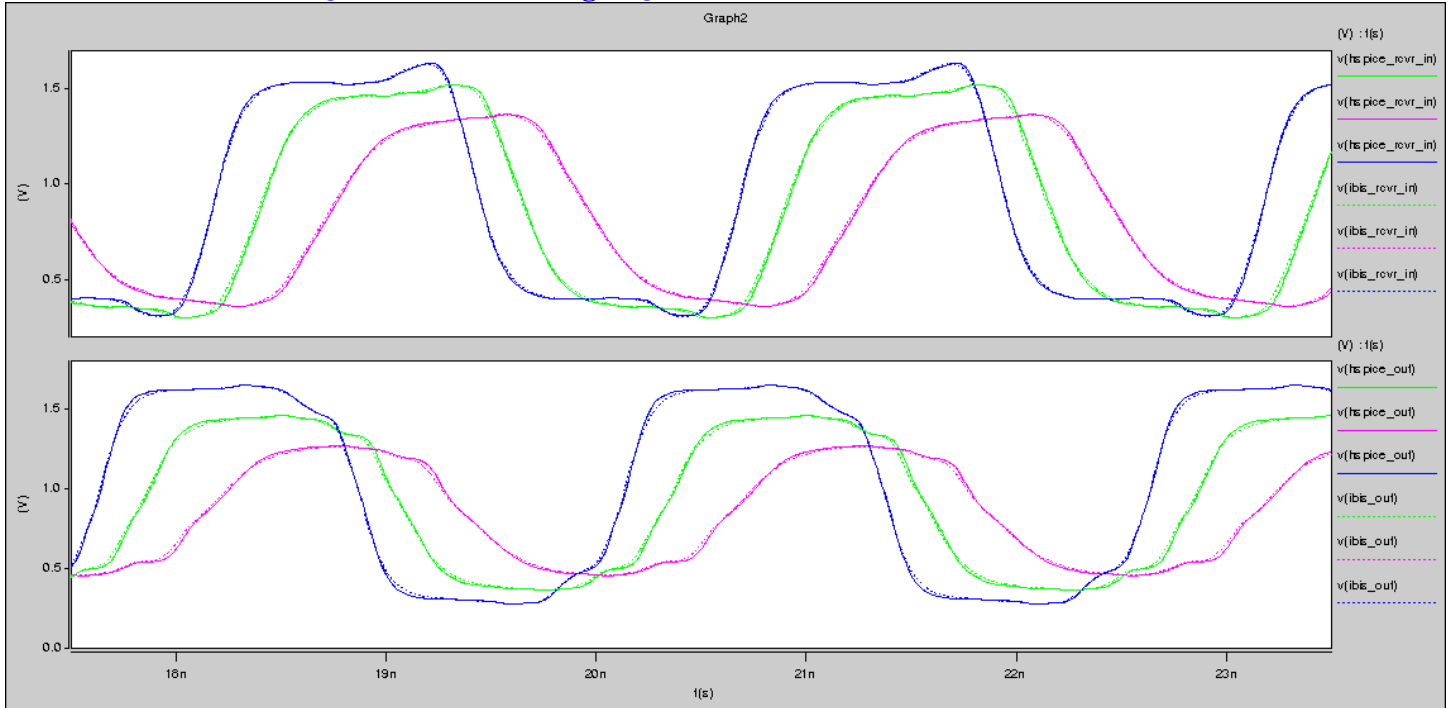
### iii. DQFULL\_800 driving DQFULL\_ODT75\_800



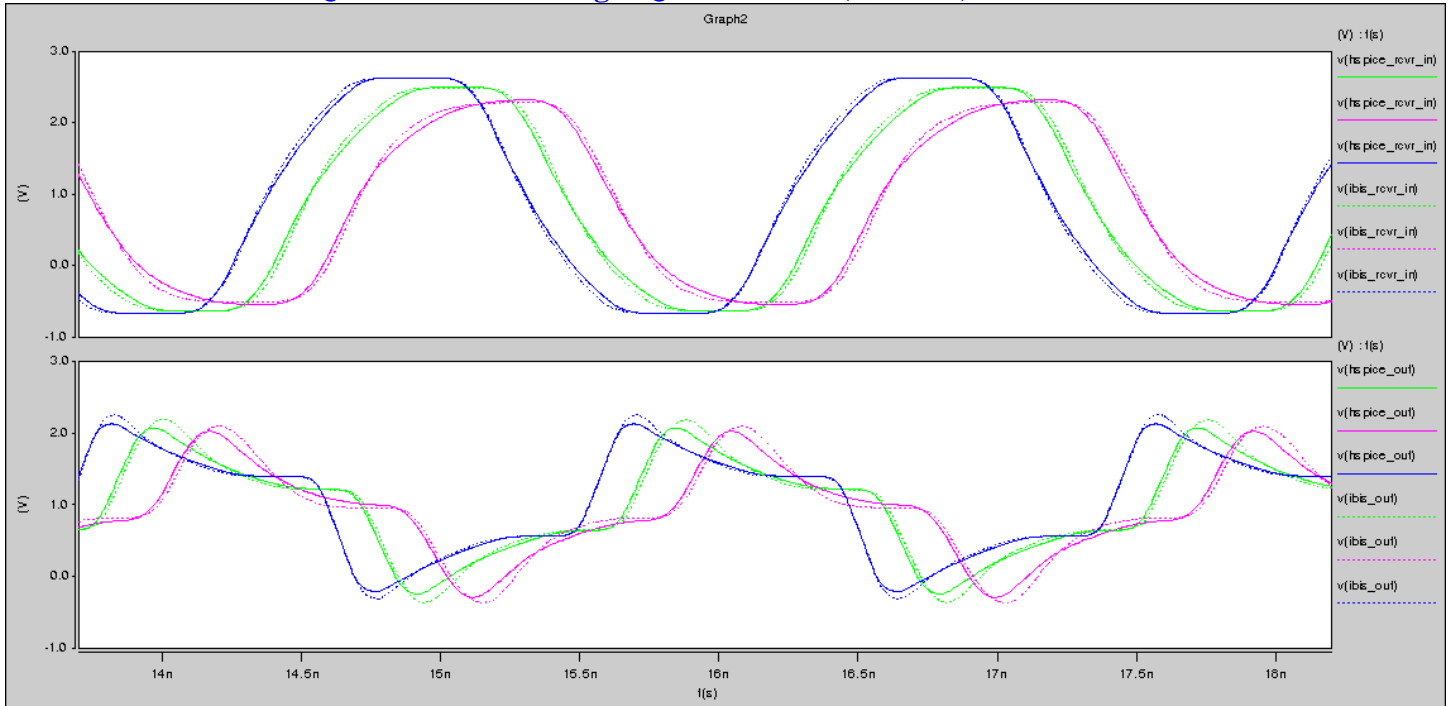
### iv. DQFULL\_800 driving DQFULL\_ODT150\_800



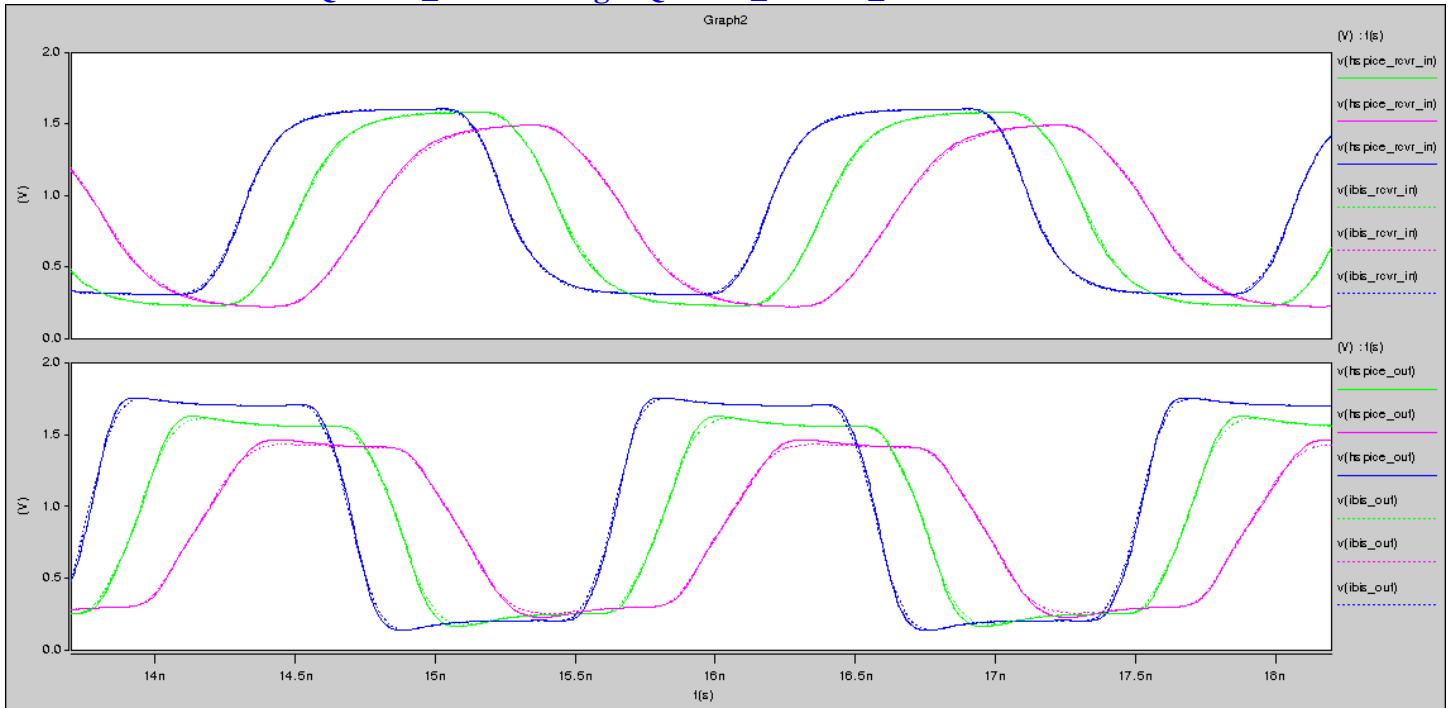
### v. DQHALF\_800 driving DQHALF\_ODT50\_800



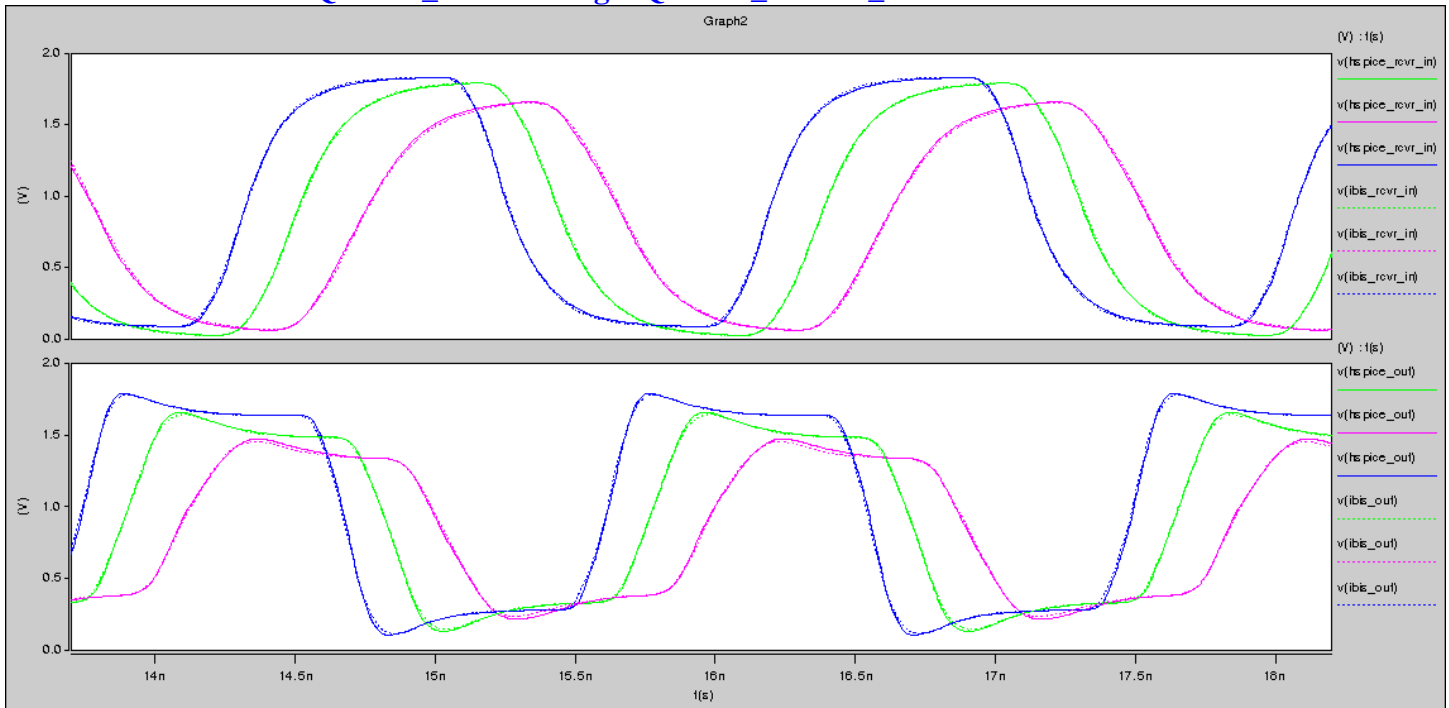
### vi. DQFULL\_1066 driving DQFULL\_1066 (no ODT)



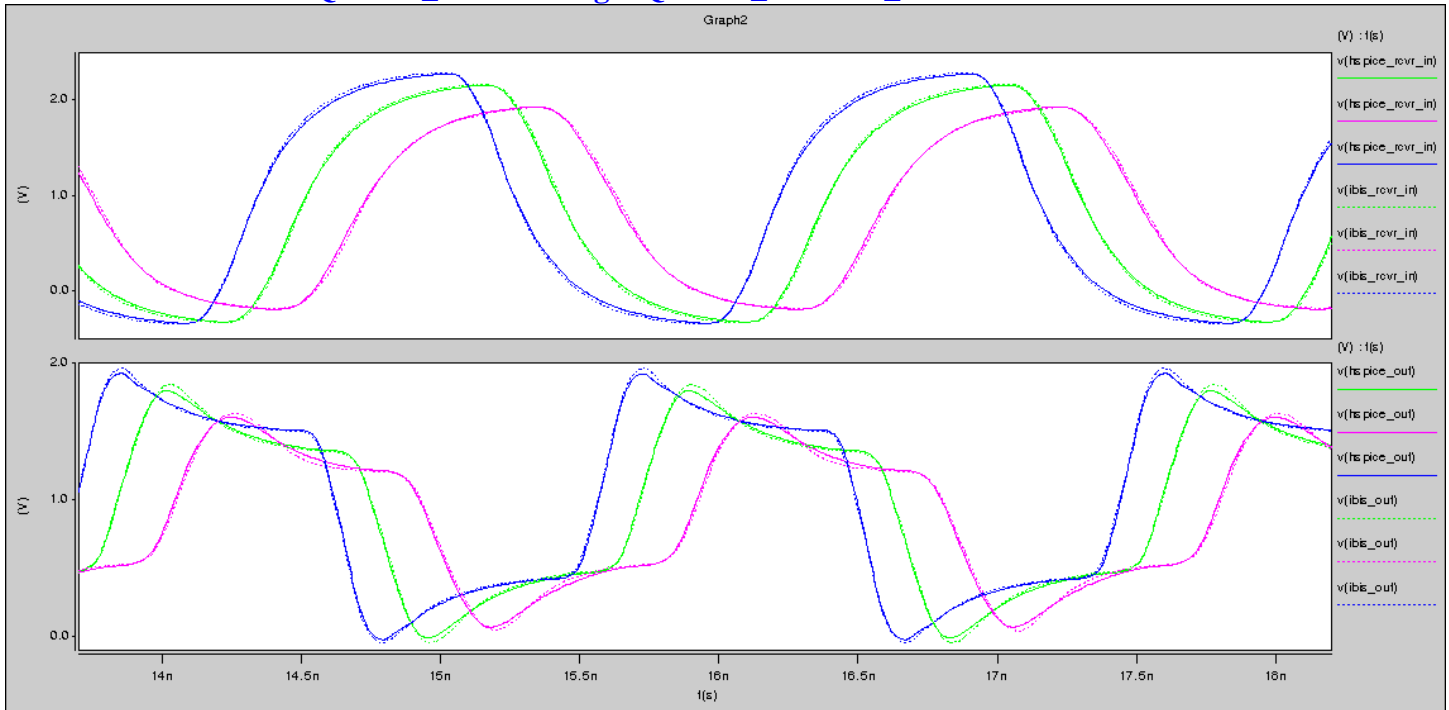
### vii. DQFULL\_1066 driving DQFULL\_ODT50\_1066



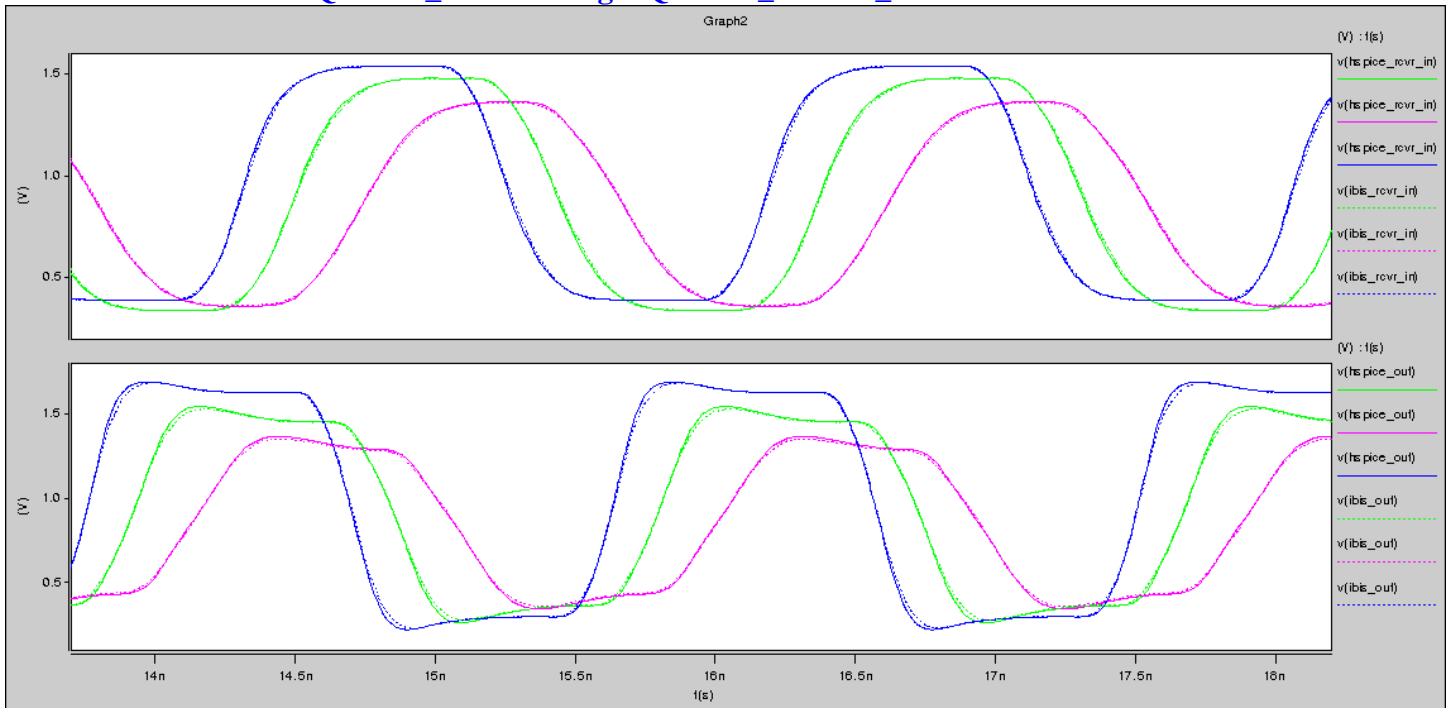
### viii. DQFULL\_1066 driving DQFULL\_ODT75\_1066



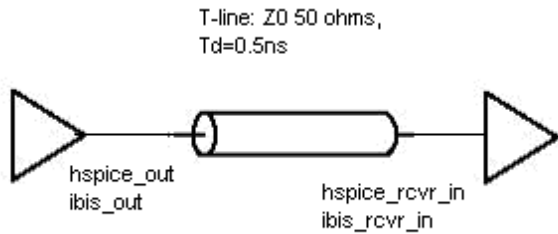
### ix. DQFULL\_1066 driving DQFULL\_ODT150\_1066



### x. DQHALF\_1066 driving DQHALF\_ODT50\_1066



## Setup



## Comments:

1. The following models must be overclocked by the simulator: DQ\_FULL\_1066 and DQ\_HALF\_1066. The duration of the V-t curves is greater than the bit time. This was necessary to match the end points to the DC expected points with small error. Most simulators support overclocking, while simulators that do not support this will flag errors/warnings.
2. Slew rate is based on HSPICE simulation with a 25ohm to Vtt load. This includes simple package parasitics.

## Document Revision History

Rev **1.0** - Date **6/19/2013**

- a. IBIS revision **1.0**
- b. HSpice revision **1.0**

Rev **2.0** - Date **11/19/2013**

- a. IBIS revision **2.0**
- b. HSpice revision **2.0**

Rev **2.1** - Date **2/18/2014**

- a. IBIS revision **2.1**
- b. HSpice revision **2.0**

Rev **2.11** - Date **10/12/2015 (added AUT)**

- a. IBIS revision **2.1**
- b. HSpice revision **2.1**

Rev **2.2** - Date **2/5/2016**

- a. IBIS revision **2.2**
- b. HSpice revision **2.1**