IBIS/HSPICE Model Quality Report

Design ID: T67A
Description: 512Mb DDR SDRAM
Marketing device name(s): MT46V128M4TG, MT46V64M8TG, MT46V32M16TG, MT46V128M4P, MT46V64M8P, MT46V32M16P, MT46V128M4CV, MT46V64M8CV, MT46V32M16CV, MT46V128M4CY, MT46V64M8CY, MT46V32M16CY, MT46V128M4T67A, MT46V64M8T67A, MT46V32M16T67A
Valid speed grades: DDR-266/333/400
Zip filename: t67a_ibis.zip
IBIS filename: t67a.ibs, t67a_at.ibs, t67a_it.ibs **File rev:** 2.3
HSpice filename: t67a_hspice.zip **File rev:** 2.0
EBD filename (if applicable): N/A **File rev:** N/A
Die rev: J
Date: April 8, 2013
Datasheet link: go to http://www.micron.com/my.html and search columns for t67a

E-mail modelsupport@micron.com for questions regarding Quality Report.

Device Parameters

VDDQ – Slow: 2.3 **Typical:** 2.5 **Fast:** 2.7
VDD – Slow: 2.3 **Typical:** 2.5 **Fast:** 2.7
VDDQ-DDR400 - Slow: 2.5 **Typical:** 2.6 **Fast:** 2.7
VDD –DDR400- Slow: 2.5 **Typical:** 2.6 **Fast:** 2.7
Junction Temperature (Commercial) - Slow: 85C **Typical:** 50C **Fast:** 0C
Junction Temperature (Industrial) - Slow: 100C **Typical:** 50C **Fast:** 0C
Junction Temperature (Automotive) - Slow: 120C **Typical:** 50C **Fast:** 0C
VDDQ/VSSQ Decoupling Capacitance: 2.8nF
Included in HSPICE DQ/DQS models? YES **Amount per DQ/DQS model:** 141pF/282pF
VDDQ/VSSQ Decoupling Capacitance Series Resistance: 5.1 Ohms

IBIS Quality Summary

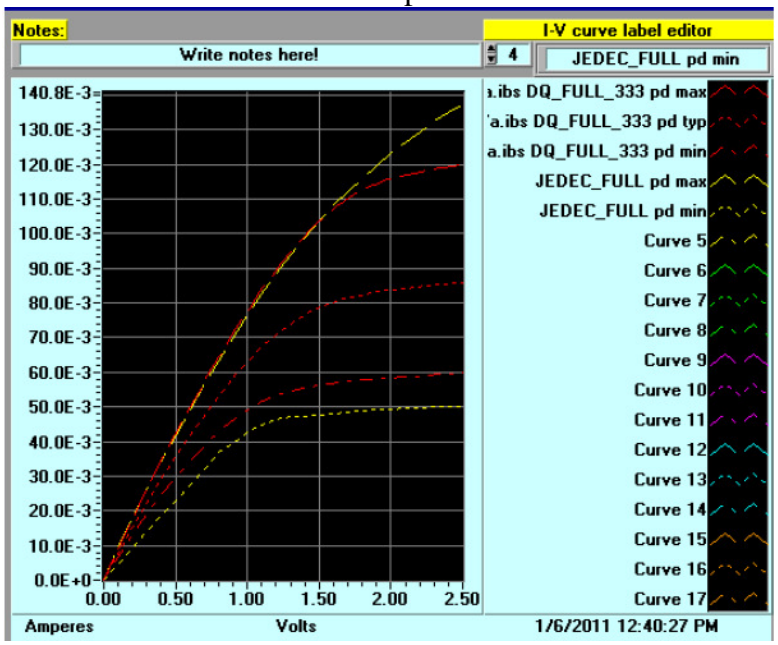
1. ☒ Include the IBIS Quality Specification 2.0 Overall IBIS Quality level. For details on IBIS Quality, reference the quality specification and quality checklist on IBIS quality webpage http://www.eda.org/pub/ibis/quality_wip/.

   Overall IBIS Quality Level: 3MS
   Exceptions: 0
2. ☒ Include the filename of the IBIS Quality Checklist that accompanies this report.
   Filename: t67a_ibis_quality_2.2_checklist.xls

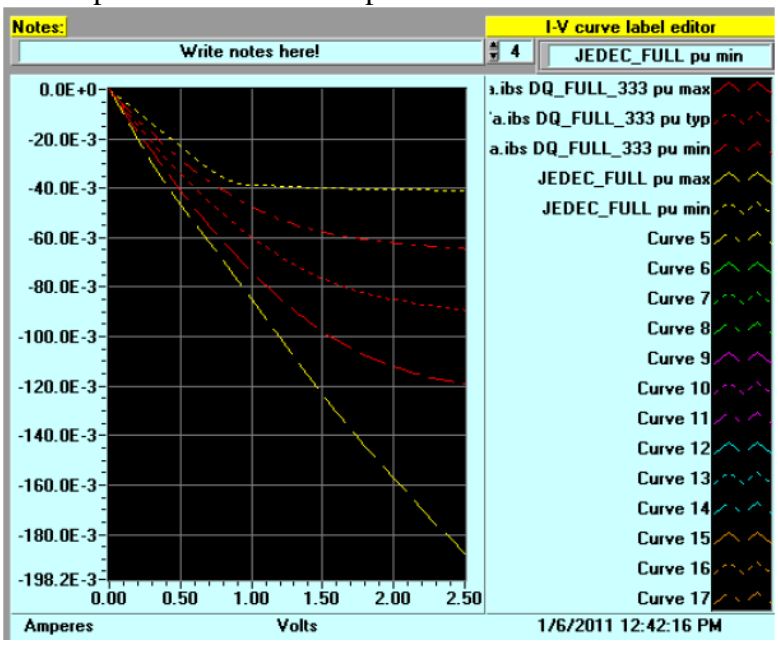
IBIS MODEL Correlation

Datasheet Correlation

1. ☒ For Output or I/O model compare datasheet IOH/IOL data with IBIS pullup/pulldown data.
   a. Model name: **DQ_FULL_333**
      i. Pulldown I-V versus **DDR1** specification

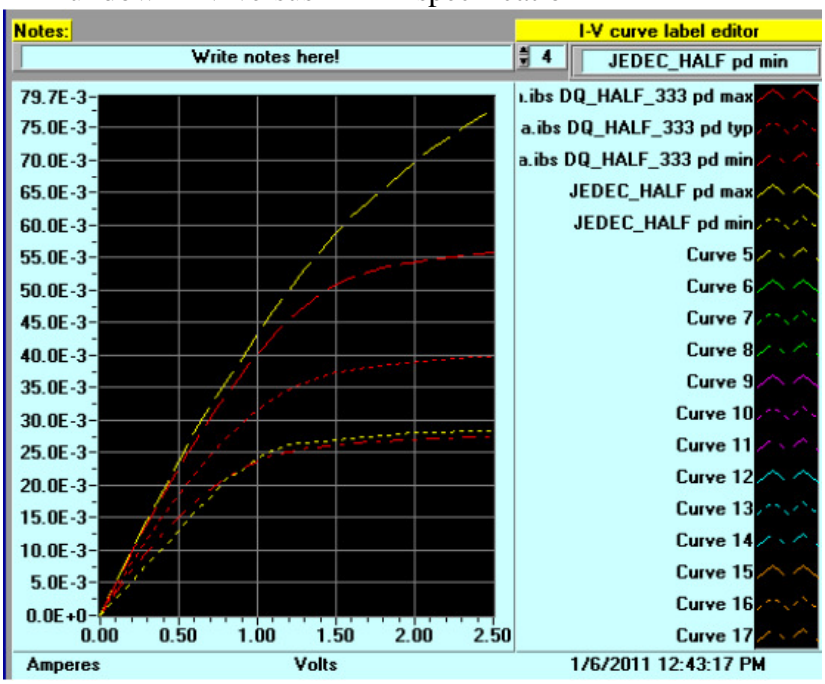


      ii. Pullup I-V versus **DDR1** specification

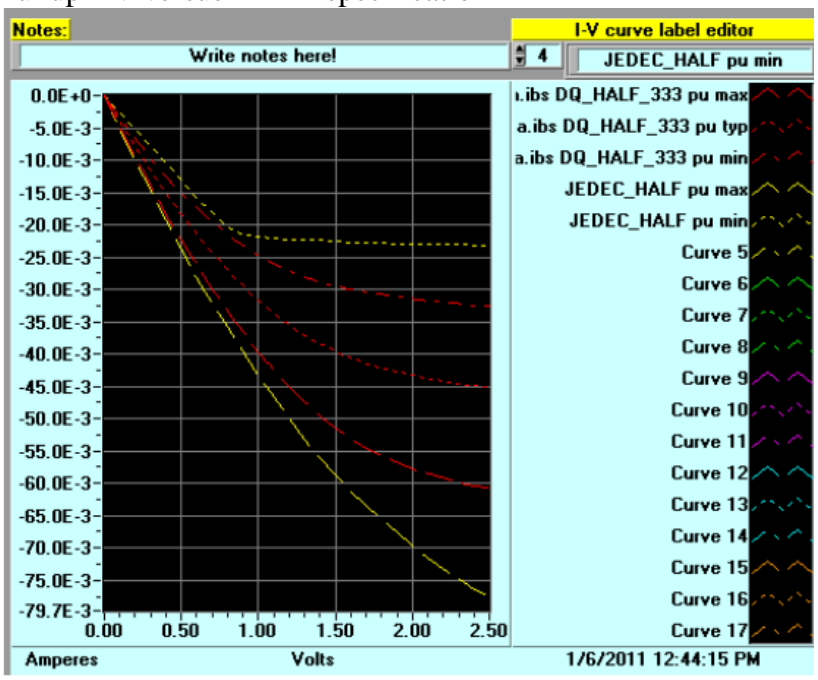


b. Model name: **DQ_HALF_333**

i. Pulldown I-V versus **DDR1** specification

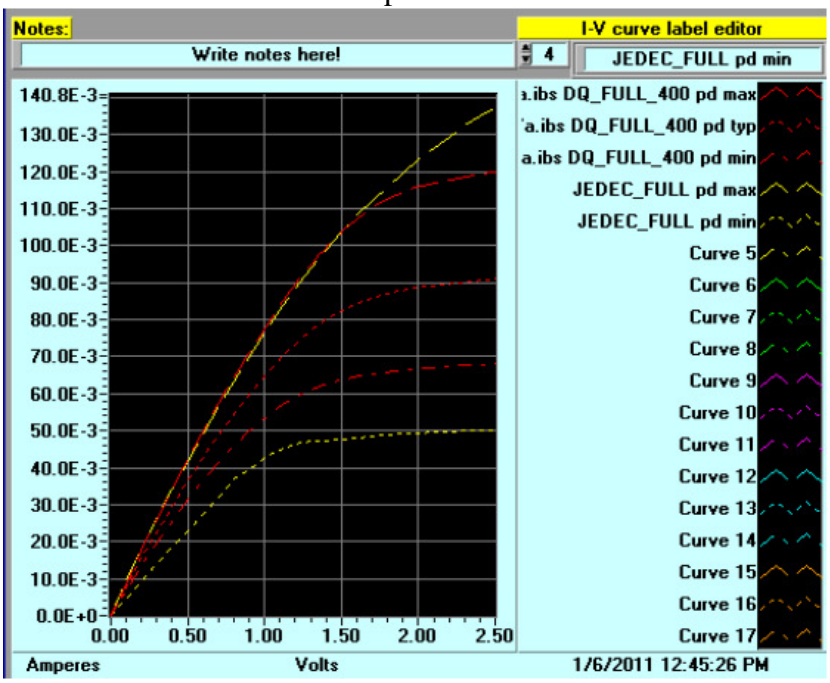


ii. Pullup I-V versus **DDR1** specification

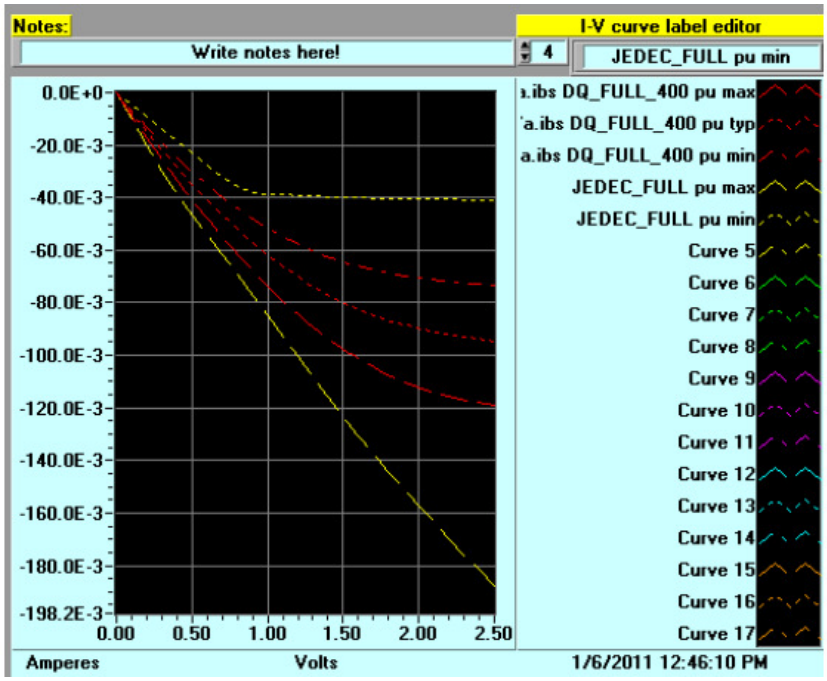


c. Model name: **DQ_FULL_400**

i. Pulldown I-V versus **DDR1** specification

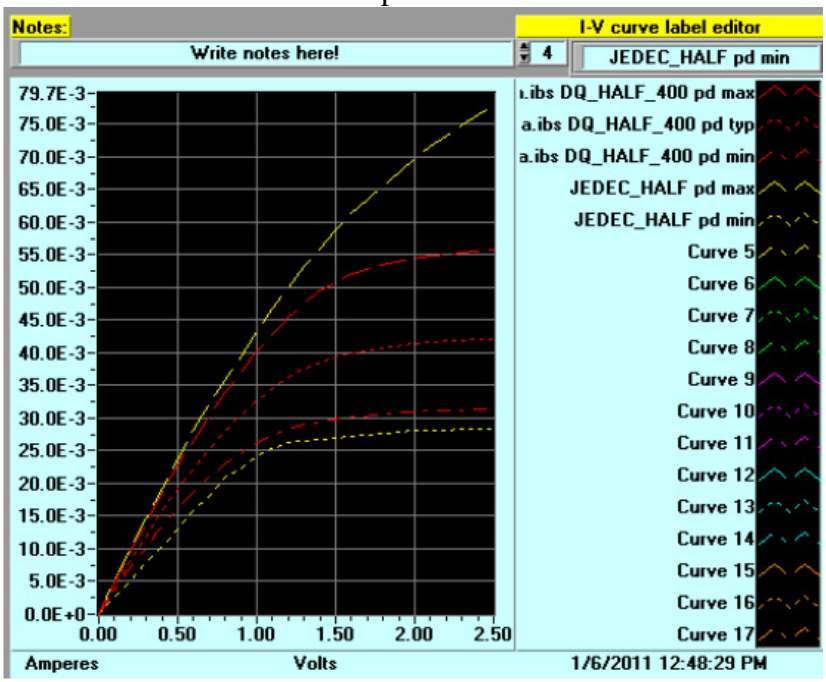


ii. Pullup I-V versus **DDR1** specification

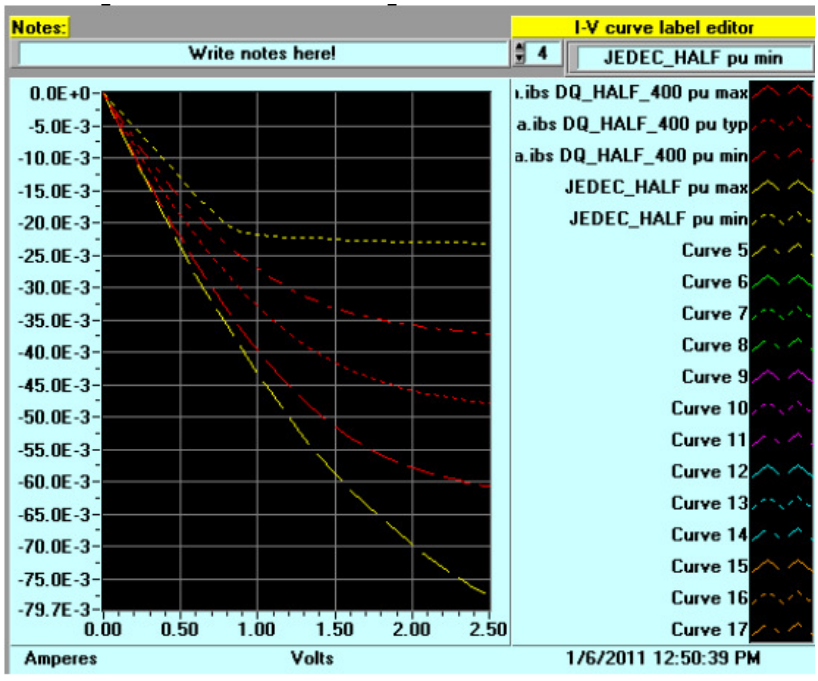


d. Model name: **DQ_HALF_400**

i. Pulldown I-V versus **DDR1** specification



ii. Pullup I-V versus **DDR1** specification



2. ☒ Compare C_comp with datasheet Input C. Provide C_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16).

Component name: **MT46V32M16CV (x16 FBGA)**

		IBIS		Datasheet	
		min	max	min	max
DQ	C_comp	3.389	3.689	NA	NA
	C package	0.289	0.566	NA	NA
	C_total	3.678	4.255	3.500	4.500
INPUT	C_comp	1.025	1.225	NA	NA
	C package	0.234	0.510	NA	NA
	C_total	1.259	1.735	1.500	2.500
CLK	C_comp	1.063	1.263	NA	NA
	C package	0.231	0.290	NA	NA
	C_total	1.294	1.553	1.500	2.500

Component name: **MT46V32M16TG (x16 TSOP)**

		IBIS		Datasheet	
		min	max	min	max
DQ	C_comp	3.389	3.689	NA	NA
	C package	0.970	1.500	NA	NA
	C_total	4.359	5.189	4.000	5.000
INPUT	C_comp	1.025	1.225	NA	NA
	C package	1.000	1.490	NA	NA
	C_total	2.025	2.715	2.000	3.000
CLK	C_comp	1.063	1.263	NA	NA
	C package	0.970	1.010	NA	NA
	C_total	2.033	2.273	2.000	3.000

3. ☐ **Not Included.** If slew rate specifications (rise/fall slew) are available from the datasheet, complete HSpice simulations to generate slew rate data and provide a comparison table.

		IBIS			Datasheet	
Model	Slew Rate (V/ns)	min	typ	max	min	max
DQ Full	Rising					
	Falling					
DQ Half	Rising					
	Falling					

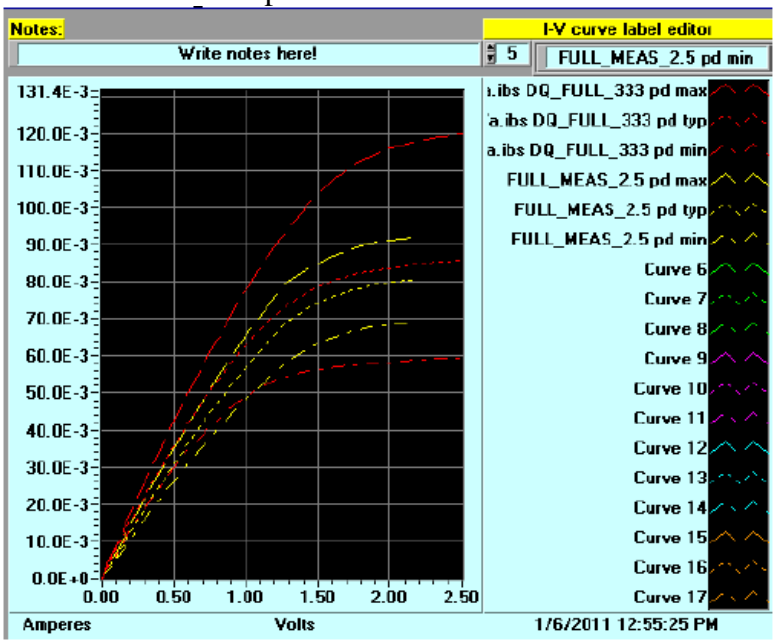
4. ☐ **Not Applicable for DDR1.** Compare ODT data with datasheet.

ODT calculated using the formula $RTT=(V_{IH(ac)} - V_{IL(ac)})/|(I(V_{IH(ac)}) - I(V_{IL(ac)})|$

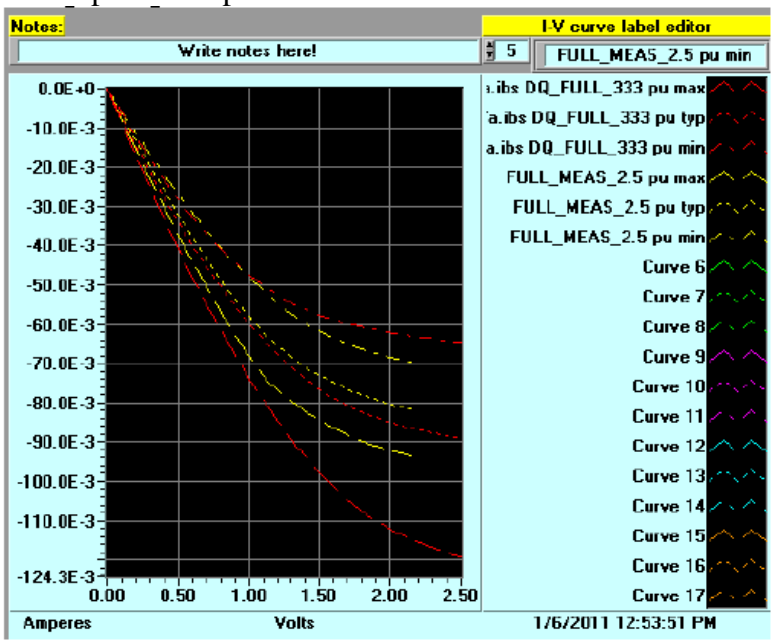
ODTXX	**TYP**	**MIN**	**MAX**
Vil (V)			
Vih (V)			
Ivil (A)			
Ivih (A)			
	TYP	**MIN**	**MAX**
Rtt (Model)			
Rtt (datasheet)	XX	XX	XX

Measurement Correlation

1. ☒ For Output or I/O models compare measured IOH/IOL data with IBIS pullup/pulldown data. If the measurement conditions are different than the IBIS conditions, run HSpice simulations using the same measurement conditions such as VCC, temperature, and process. Include measurement conditions in the pullup/pulldown images.
    a. Model name: **DQ_FULL_333**
        i. Pulldown I-V comparison

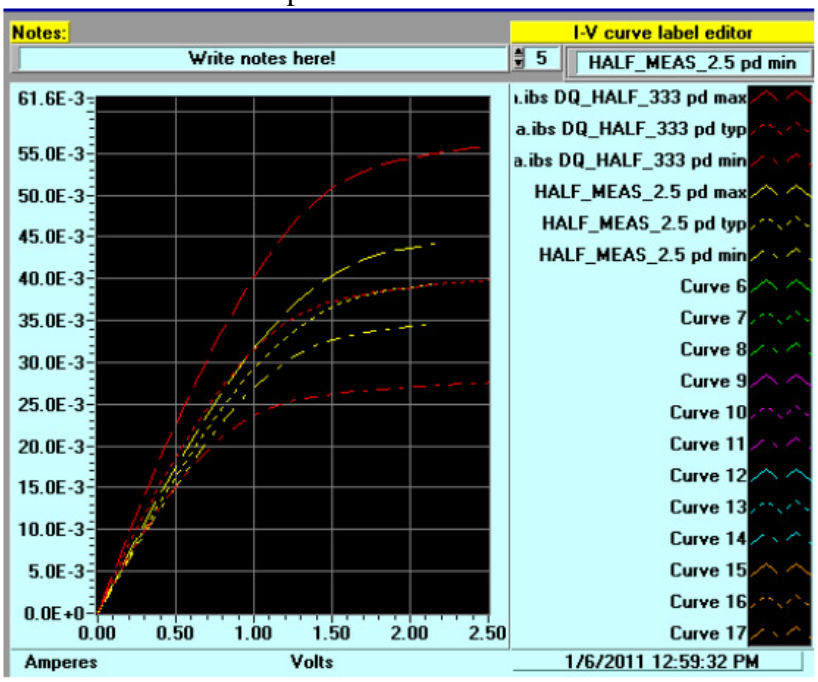


        ii. Pullup I-V comparison

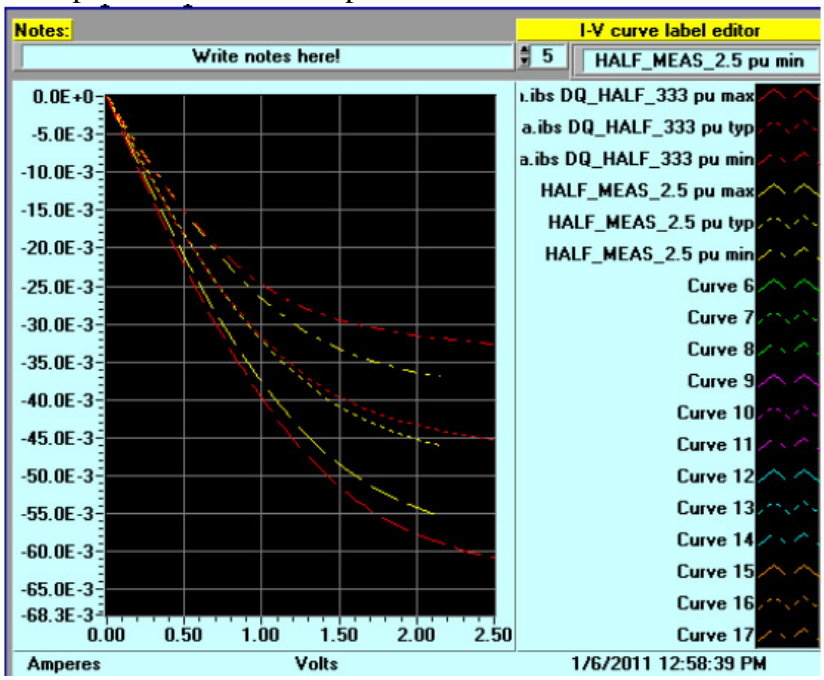


b. Model name: **DQ_HALF_333**

ii. Pulldown I-V comparison

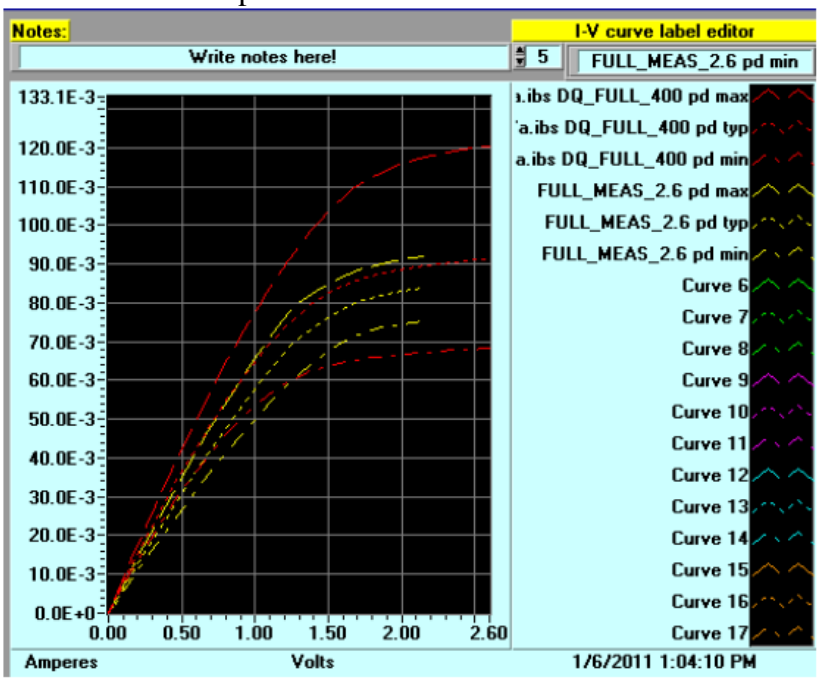


ii. Pullup I-V versus **DDR1** specification

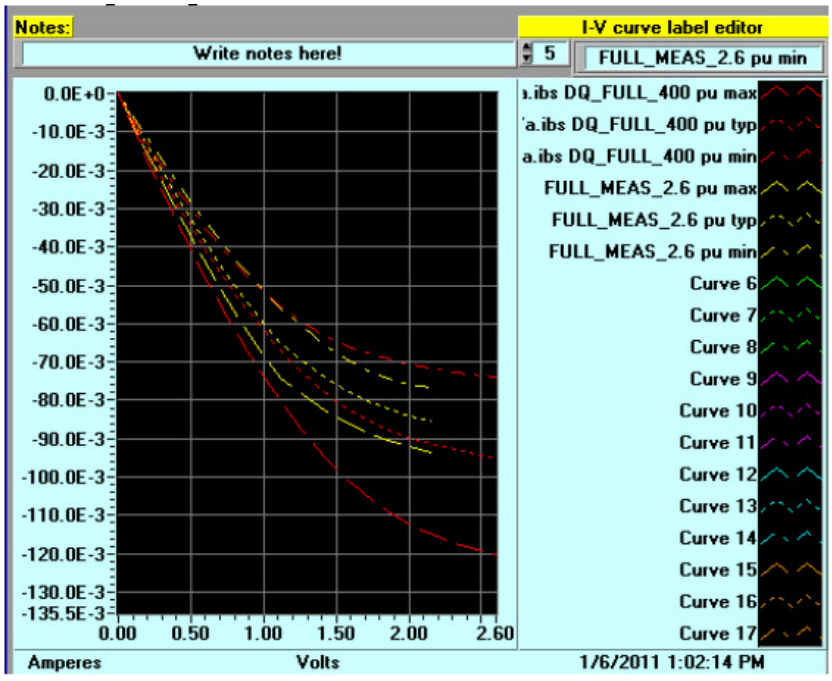


c. Model name: **DQ_FULL_400**

i. Pulldown I-V comparison

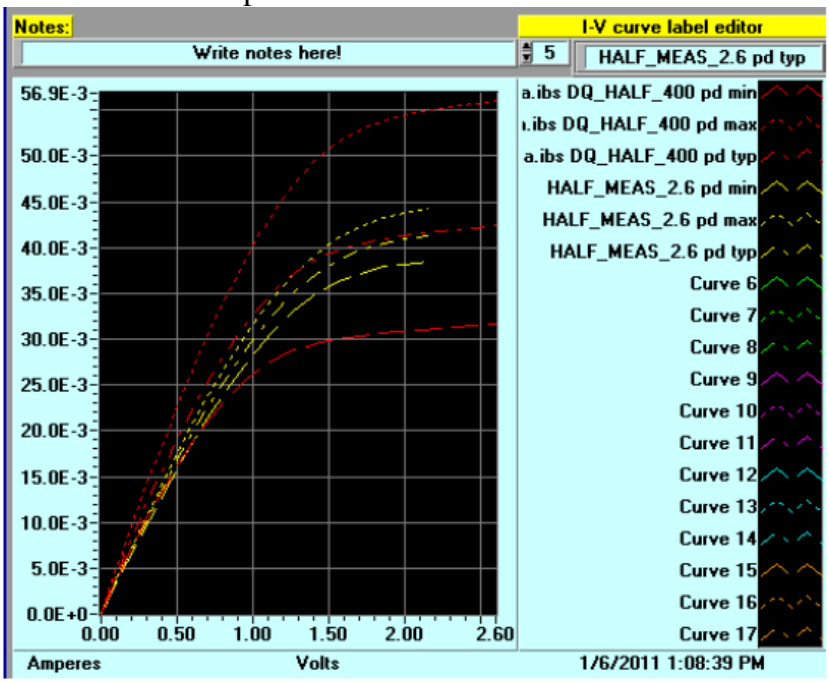


ii. Pullup I-V comparison

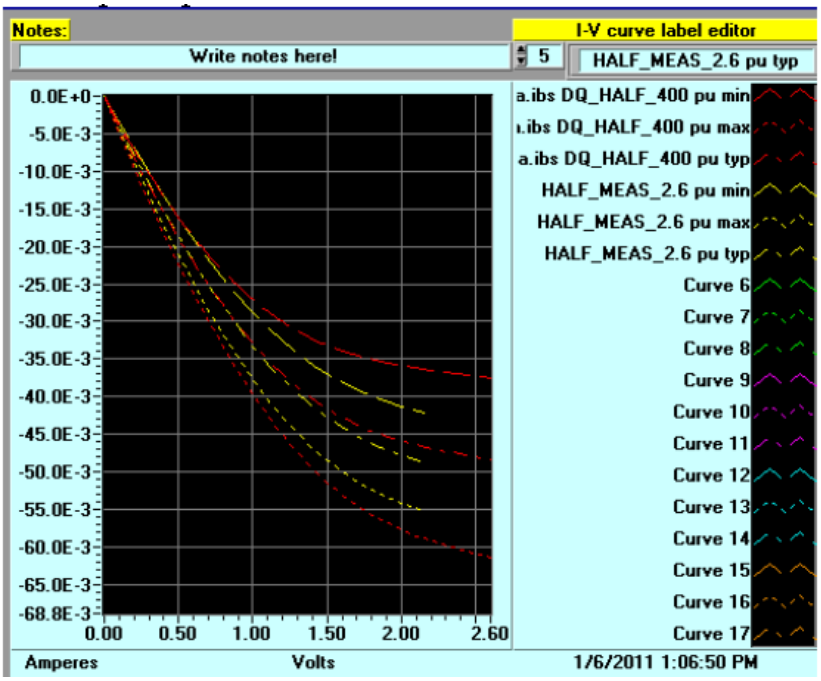


d. Model name: **DQ_HALF_400**

i. Pulldown I-V comparison



ii. Pullup I-V comparison



2. ☒ Compare C_comp with measured C_comp. Provide C_comp comparison table for all models and for all package combinations (i.e x4, x8 and x16).

Component name: **MT46V32M16CV (x16 FBGA)**

		IBIS			Measured		
		min	typ	max	min	typ	max
DQ	C_comp	3.389	3.539	3.689	NA	NA	NA
	C package	0.289	0.411	0.566	NA	NA	NA
	C_total	3.678	3.950	4.255	3.978	4.250	4.555
INPUT	C_comp	1.083	1.183	1.283	NA	NA	NA
	C package	0.234	0.350	0.510	NA	NA	NA
	C_total	1.317	1.533	1.793	1.241	1.457	1.717
CLK	C_comp	1.089	1.189	1.289	NA	NA	NA
	C package	0.231	0.260	0.290	NA	NA	NA
	C_total	1.320	1.450	1.579	1.403	1.533	1.662

Component name: **MT46V32M16TG (x16 TSOP)**

		IBIS			Measured		
		min	typ	max	min	typ	max
DQ	C_comp	3.389	3.539	3.689	NA	NA	NA
	C package	0.970	1.200	1.500	NA	NA	NA
	C_total	4.359	4.739	5.189	4.659	5.039	5.489
INPUT	C_comp	1.083	1.183	1.283	NA	NA	NA
	C package	1.000	1.290	1.490	NA	NA	NA
	C_total	2.083	2.473	2.773	2.007	2.397	2.697
CLK	C_comp	1.089	1.189	1.289	NA	NA	NA
	C package	0.970	0.990	1.010	NA	NA	NA
	C_total	2.059	2.179	2.299	2.142	2.262	2.382

3. ☐ If measured clamp current data is available provide an IBIS and measurement comparison for all models.
   Not Available
   a. Model name:
      i. Power-clamp comparison image
      ii. Gnd-clamp comparison image

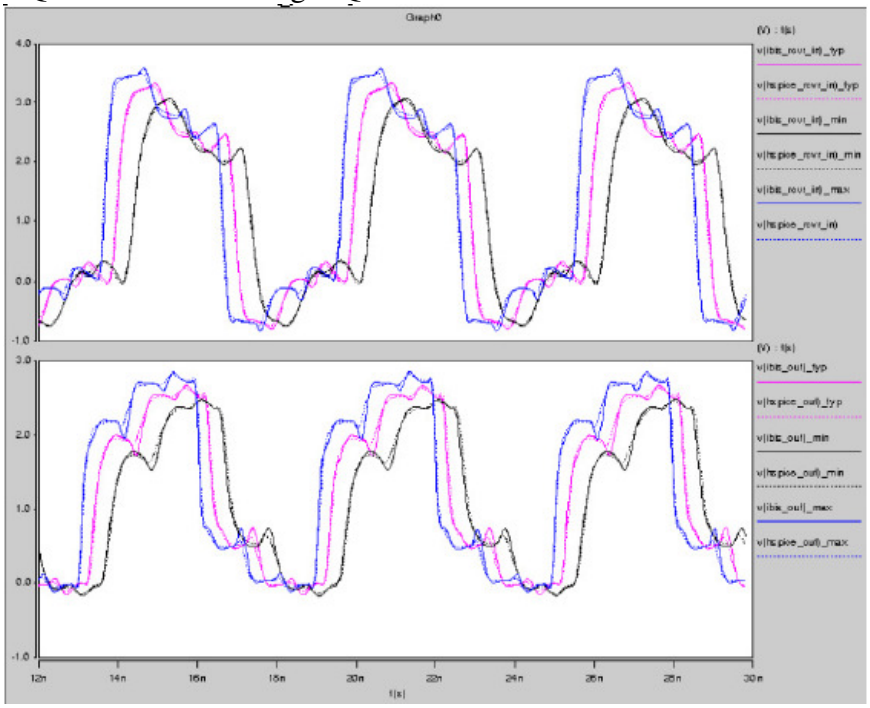
4. ☐ If slew rate data (rise/fall slew) is available from measurements, complete HSpice simulations to generate slew rate data and provide a comparison table.
   Not Available

		IBIS			Measurement	
Model	Slew Rate (V/ns)	min	typ	max	min	max
DQ_FULL	Rising					
	Falling					
DQ_HALF	Rising					
	Falling					

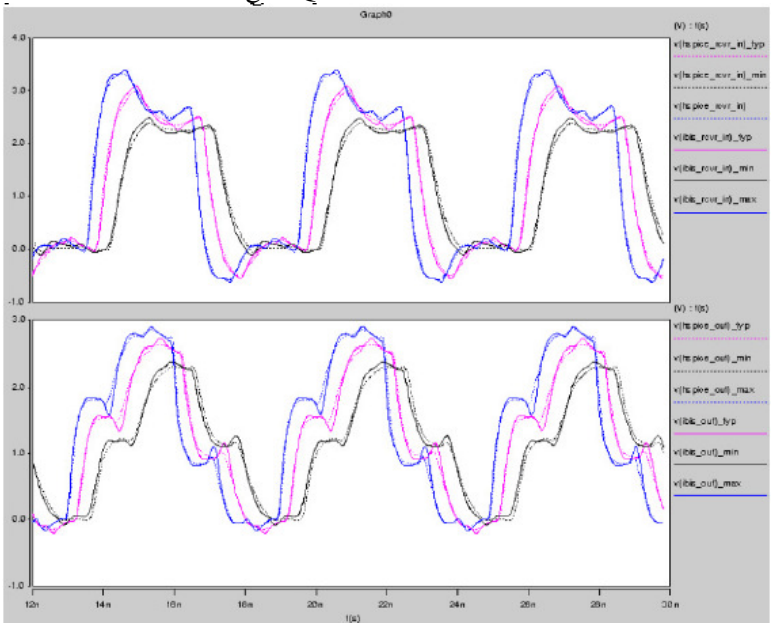
IBIS vs HSPICE Correlation

1. ☒ For all Output or I/O models, run HSpice transient simulations using encrypted netlists and the IBIS model (b-element).
   a. ☒ Use the setup and node naming conventions shown below for the IBIS and HSpice deck file (.sp file). Update the setup diagram if it is different. Indicate the version of HSPICE simulator used for simulations: **2008.09**
   b. ☒ Run simulations for all corners cases and at maximum allowable speed grade

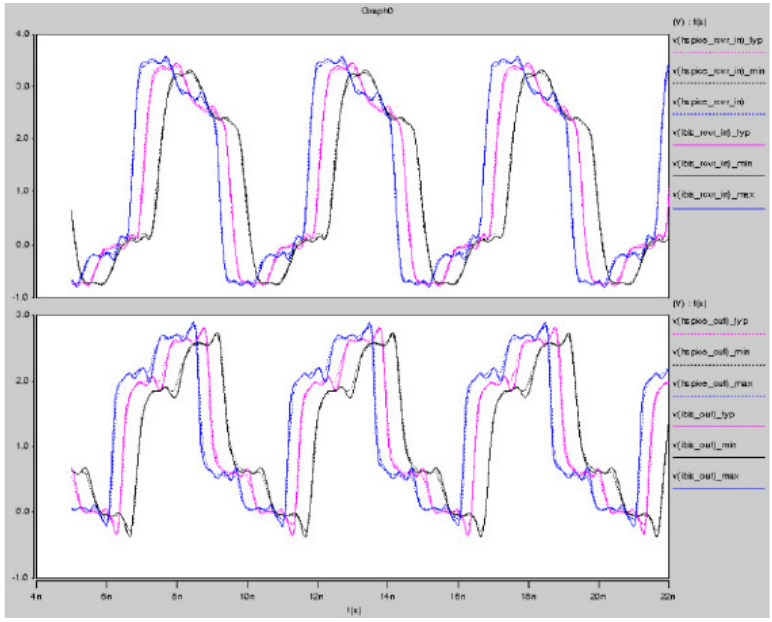
i. DQ_FULL_333 driving DQ_FULL_333



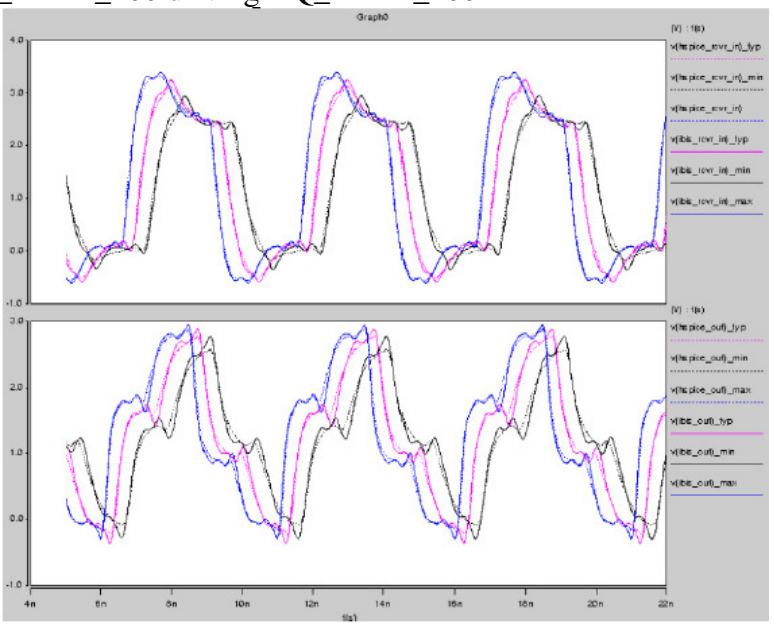
ii. DQ_HALF_333 driving DQ_HALF_333



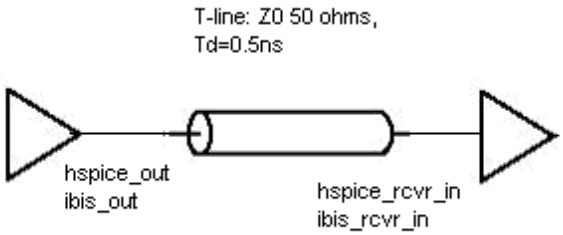
iii. DQ_FULL_400 driving DQ_FULL_400



iv. DQ_HALF_400 driving DQ_HALF_400



Setup



Comments: **Model is compared to Silicon measurements and JEDEC specifications. The driver impedance is calibrated within expected tolerances.**

Document Revision History

Rev **1.0** - Date **03/26/2010**
- a. IBIS revision **1.0**
- b. HSpice revision **1.0**

Rev **1.1** - Date **12/12/2012**
- a. IBIS revision **2.2**
- b. HSpice revision **2.0**

Rev **1.2** - Date **04/08/2013**
- a. IBIS revision **2.3**
- b. HSpice revision **2.0**

