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## **IBIS/HSPICE Model Quality Report**

**Design ID:** T66A

**Description:** 256Mb DDR SDRAM

**Marketing device name(s):** MT46V64M4TG, MT46V32M8TG, MT46V16M16TG, MT46V64M4CV, MT46V32M8CV, MT46V16M16CV, MT46V64M4T66A, MT46V32M8T66A, MT46V16M16T66A

**Valid speed grades:** DDR-333/400

**Zip filename:** t66a\_ibis.zip

**IBIS filename:** t66a.ibs, t66a\_at.ibs, t66a\_it.ibs **File rev:** 2.1

**HSpice filename:** t66a\_hspice.zip **File rev:** 2.0

**EBD filename (if applicable):** N/A **File rev:** N/A

**Die rev:** M

**Date:** September 3, 2019

**Datasheet link:** go to <https://www.micron.com> and search for t66a

For support contact your local Micron FAE/Sales contacts  
(more information at <https://www.micron.com/support/sales-network> ).

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### **Device Parameters**

**VDDQ – Slow:** 2.3 **Typical:** 2.5 **Fast:** 2.7

**VDD – Slow:** 2.3 **Typical:** 2.5 **Fast:** 2.7

**VDDQ-DDR400 - Slow:** 2.5 **Typical:** 2.6 **Fast:** 2.7

**VDD –DDR400- Slow:** 2.5 **Typical:** 2.6 **Fast:** 2.7

**Junction Temperature (Commercial) - Slow:** 85C **Typical:** 50C **Fast:** 0C

**Junction Temperature (Industrial) - Slow:** 95C **Typical:** 50C **Fast:** -40C

**Junction Temperature (Automotive) - Slow:** 110C **Typical:** 50C **Fast:** -40C

**VDDQ/VSSQ Decoupling Capacitance:** 1.58nF

**Included in HSPICE DQ/DQS models?** YES **Amount per DQ/DQS model:** 88pF

**VDDQ/VSSQ Decoupling Capacitance Series Resistance:** 14.8 Ohms

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### **IBIS Quality Summary**

1. ☒ Include the IBIS Quality Specification 2.0 Overall IBIS Quality level. For details on IBIS Quality, reference the quality specification and quality checklist on IBIS quality webpage [http://www.eda.org/pub/ibis/quality\\_wip/](http://www.eda.org/pub/ibis/quality_wip/).

**Overall IBIS Quality Level:** 3MS

**Exceptions:** 0

2. ☒ Include the filename of the IBIS Quality Checklist that accompanies this report.  
**Filename:** t66a\_ibis\_quality\_2.1\_checklist.xls

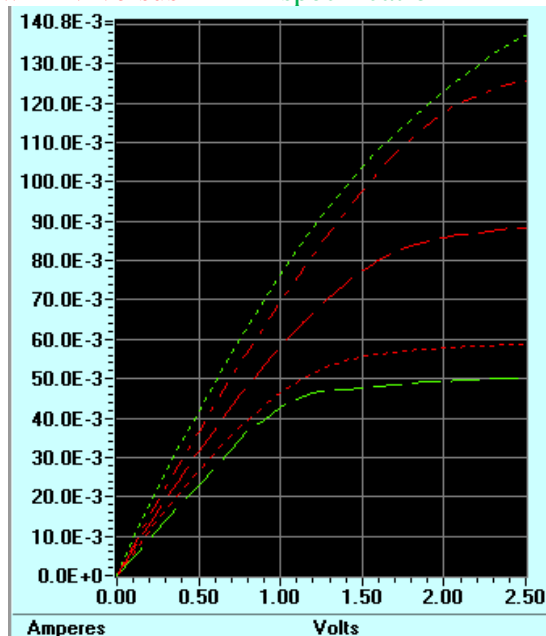
## IBIS MODEL Correlation

### Datasheet Correlation

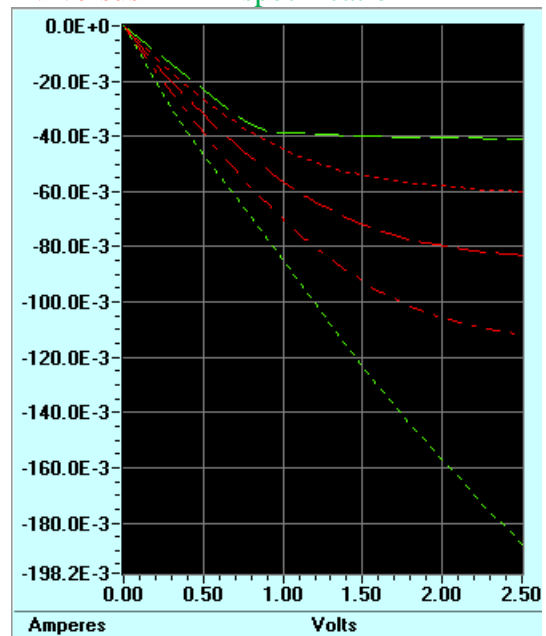
1. ☒ For Output or I/O model compare datasheet IOH/IOL data with IBIS pullup/pulldown data.

- a. Model name: **DQ\_FULL\_333**

- i. **Pulldown I-V versus DDR1 specification**

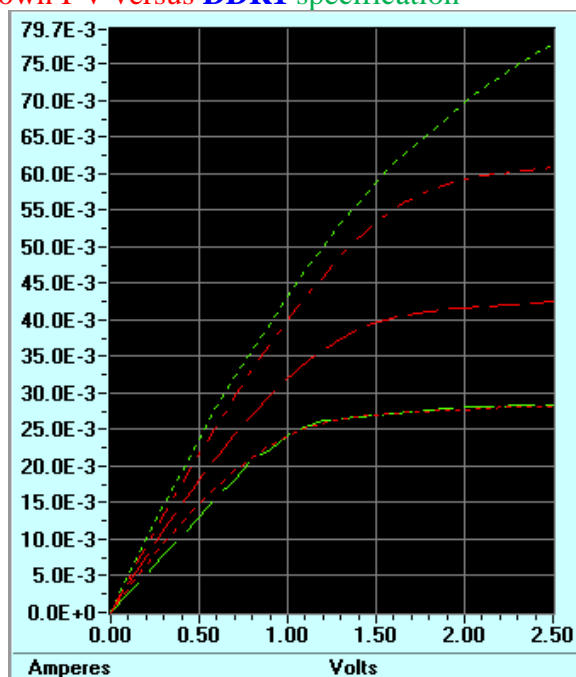


- ii. **Pullup I-V versus DDR1 specification**

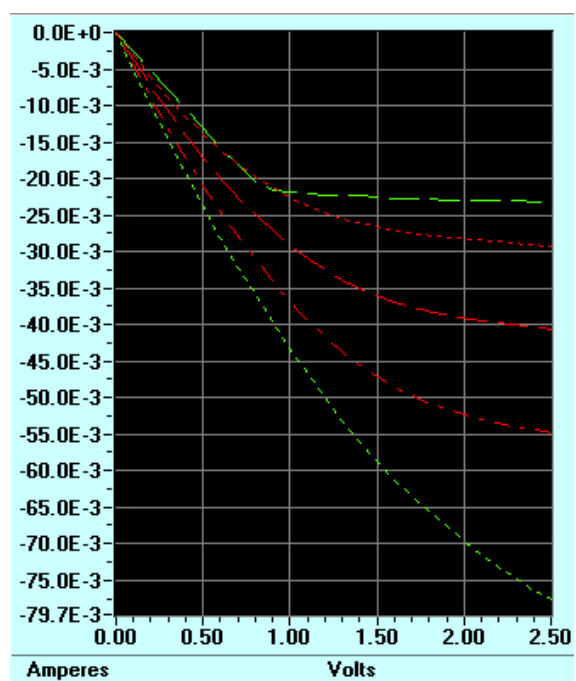


b. Model name: **DQ\_HALF\_333**

i. **Pulldown I-V versus DDR1 specification**

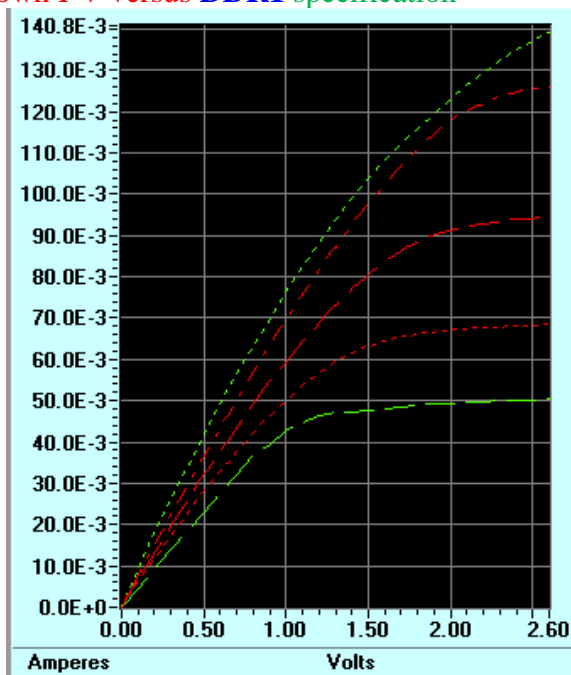


ii. **Pullup I-V versus DDR1 specification**

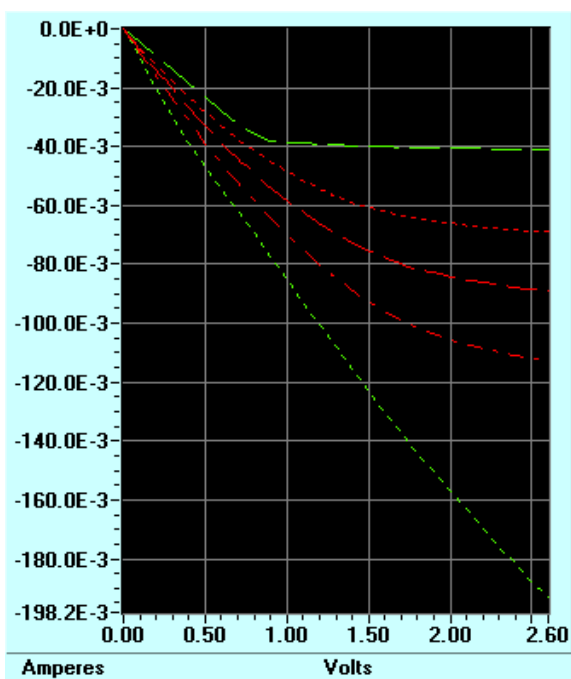


c. Model name: **DQ\_FULL\_400**

iii. **Pulldown I-V versus DDR1 specification**

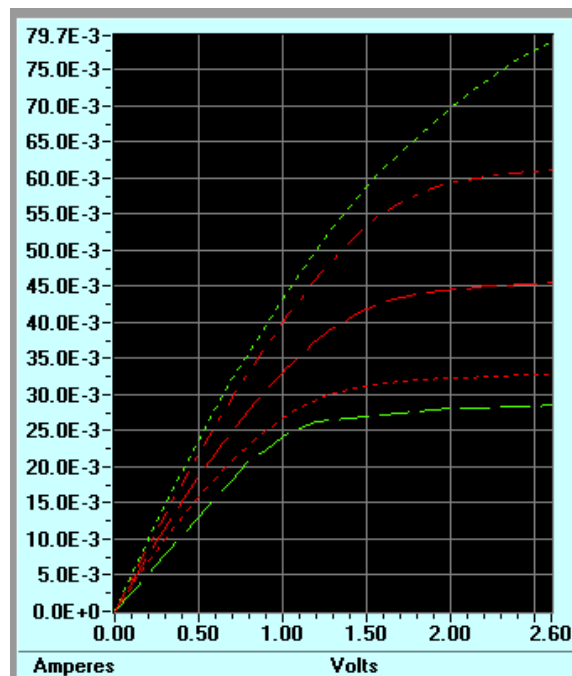


iv. **Pullup I-V versus DDR1 specification**

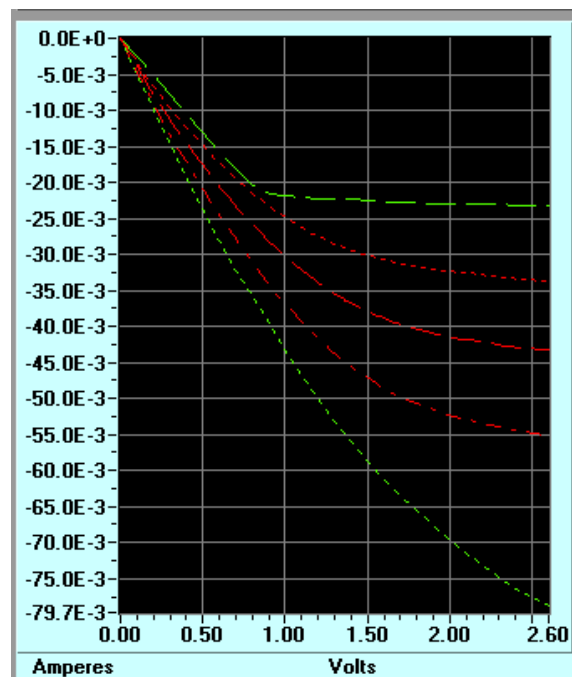


d. Model name: **DQ\_HALF\_400**

iii. **Pulldown I-V versus DDR1** specification



iv. **Pullup I-V versus DDR1** specification



2. ☒ Compare C\_comp with datasheet Input C. Provide C\_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16).

Component name: **MT46V64M4CV, MT46V32M8CV, MT46V16M16CV (FBGA)**

		IBIS		Datasheet	
		min	max	min	max
<b>DQ</b>	C_comp	3.38	3.68	NA	NA
	C_package	0.45	0.99	NA	NA
	C_total	3.83	4.67	3.50	4.50
<b>INPUT</b>	C_comp	1.23	1.43	NA	NA
	C_package	0.52	0.95	NA	NA
	C_total	1.76	2.38	1.50	2.50
<b>CLK</b>	C_comp	1.41	1.61	NA	NA
	C_package	0.57	0.58	NA	NA
	C_total	1.99	2.20	1.50	2.50

Component name: **MT46V64M4TG, MT46V32M8TG, MT46V16M16TG (TSOP)**

		IBIS		Datasheet	
		min	max	min	max
<b>DQ</b>	C_comp	3.38	3.68	NA	NA
	C_package	0.50	1.26	NA	NA
	C_total	3.88	4.94	4.00	5.00
<b>INPUT</b>	C_comp	1.23	1.43	NA	NA
	C_package	0.74	1.15	NA	NA
	C_total	1.98	2.59	2.00	3.00
<b>CLK</b>	C_comp	1.41	1.61	NA	NA
	C_package	0.74	0.75	NA	NA
	C_total	2.15	2.36	2.00	3.00

3. ☐ **Not Included.** If slew rate specifications (rise/fall slew) are available from the datasheet, complete HSpice simulations to generate slew rate data and provide a comparison table.

		IBIS			Datasheet	
Model	Slew Rate (V/ns)	min	typ	max	min	max
<b>DQ Full</b>	Rising					
	Falling					
<b>DQ Half</b>	Rising					
	Falling					

4. ☐ **Not Applicable for DDR1.** Compare ODT data with datasheet.

ODT calculated using the formula  $RTT = (V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IH(ac)}) - I(V_{IL(ac)}))$

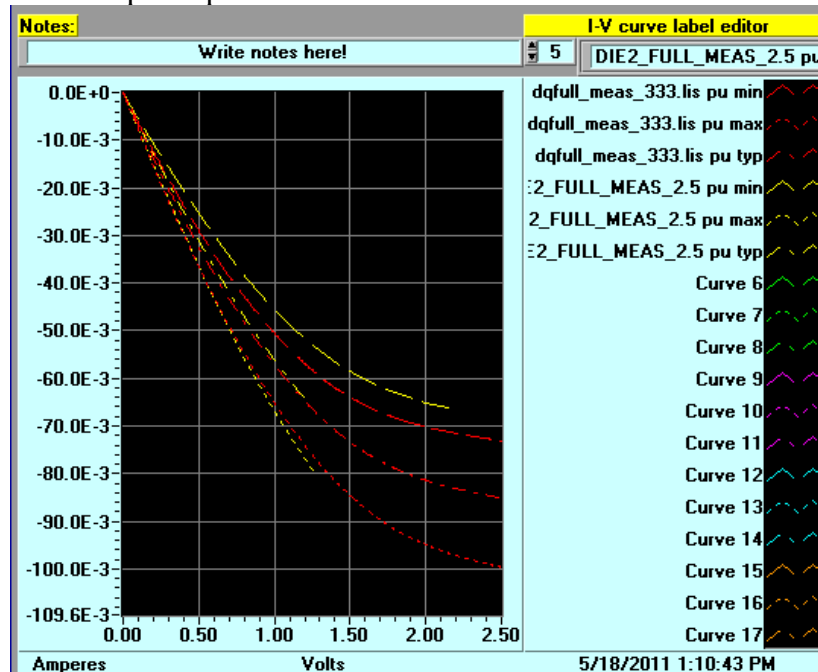
ODTXX	TYP	MIN	MAX
Vil (V)			
Vih (V)			
Ivil (A)			
Ivih (A)			
	TYP	MIN	MAX
Rtt (Model)			
Rtt (datasheet)	XX	XX	XX

### Measurement Correlation

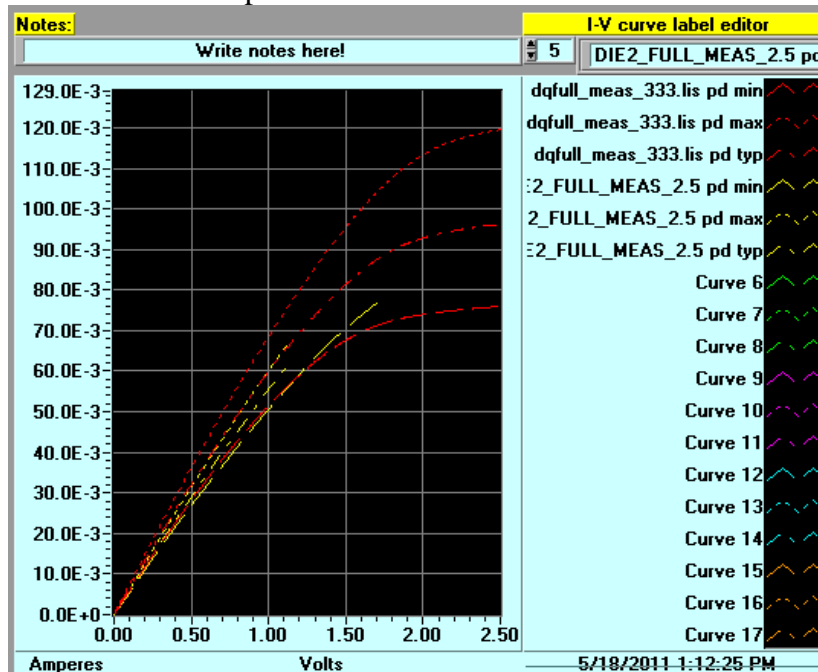
1. ☒ For Output or I/O models compare measured IOH/IOL data with IBIS pullup/pulldown data. If the measurement conditions are different than the IBIS conditions, run HSpice simulations using the same measurement conditions such as VCC, temperature, and process. Include measurement conditions in the pullup/pulldown images.

a. Model name: **DQFULL\_333**

i. Pullup comparison

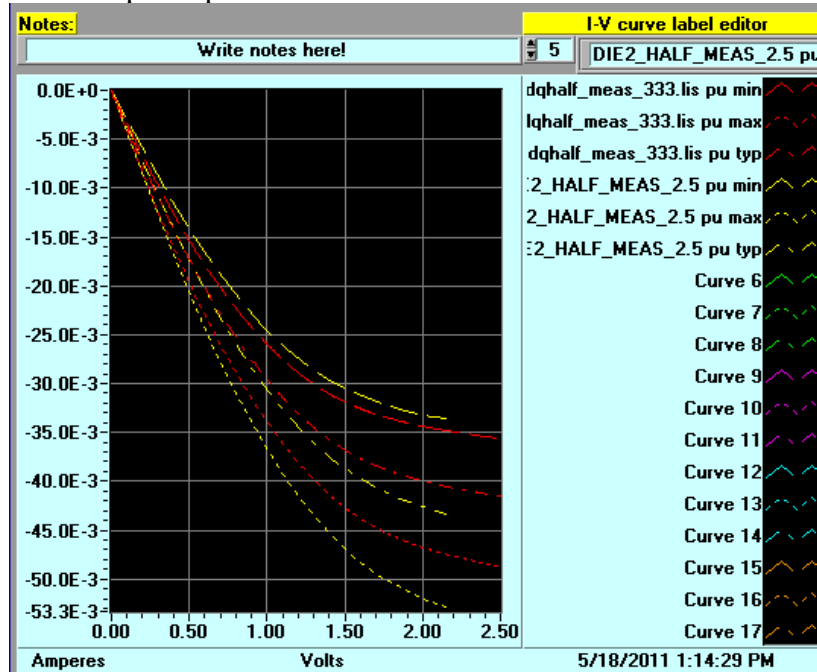


ii. Pulldown comparison

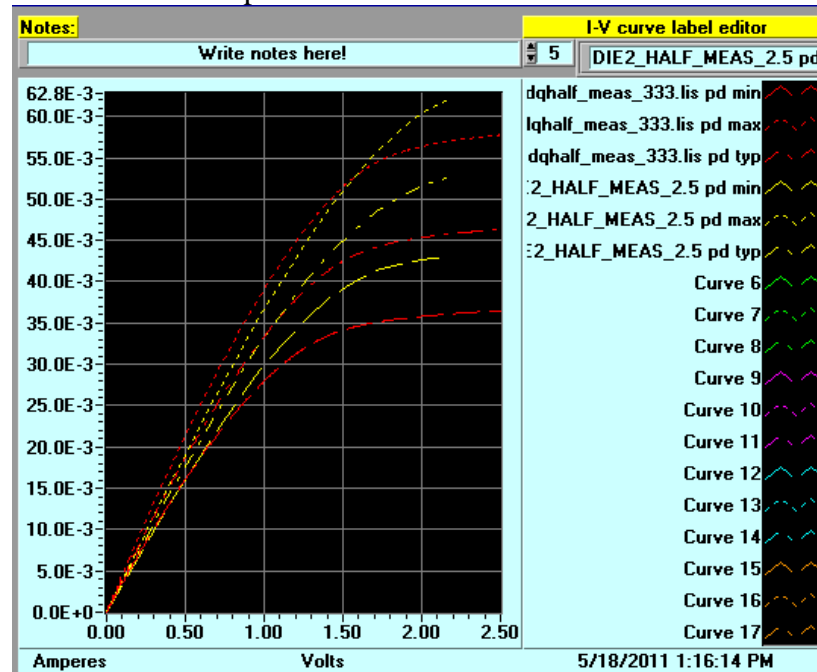


b. Model name: **DQHALF\_333**

i. Pullup comparison

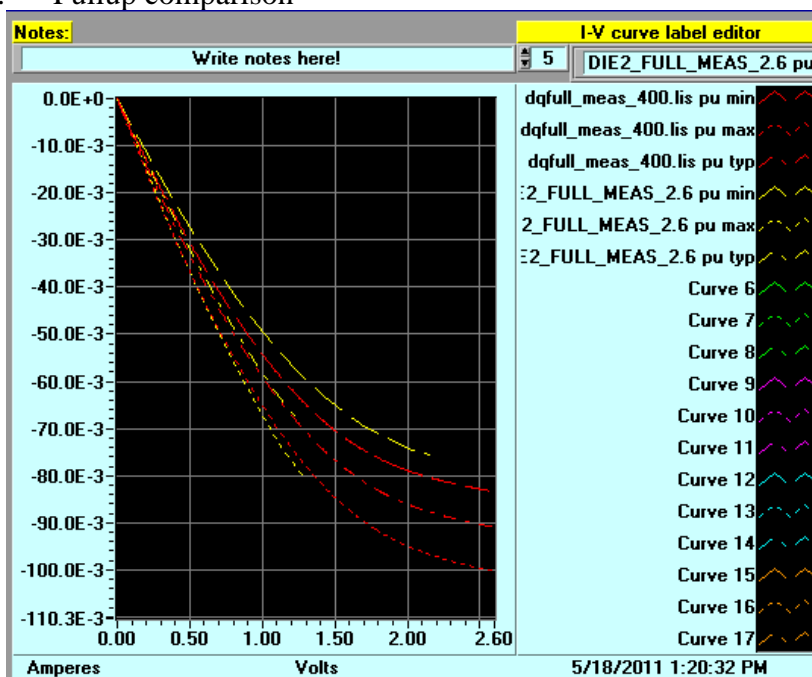


ii. Pulldown comparison

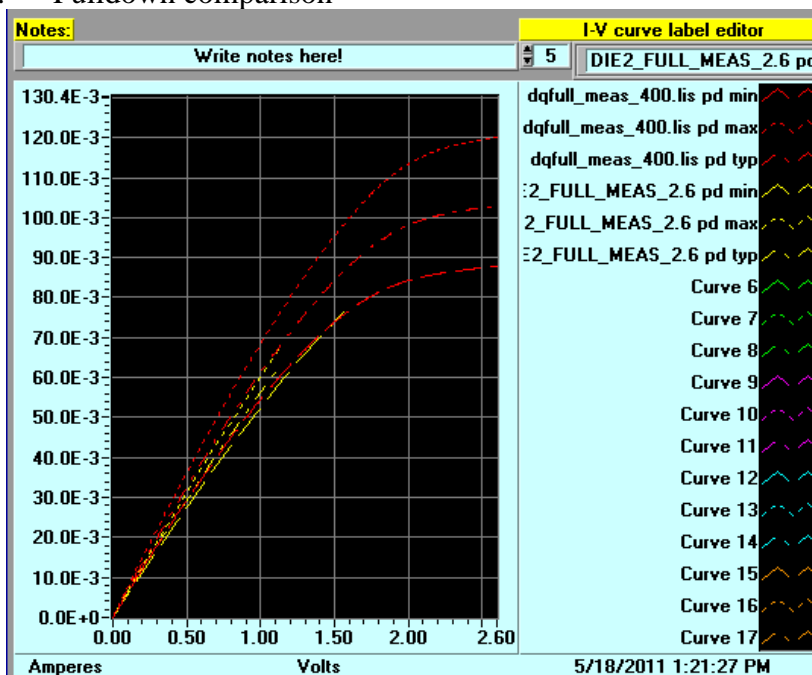


c. Model name: **DQFULL\_400**

i. Pullup comparison

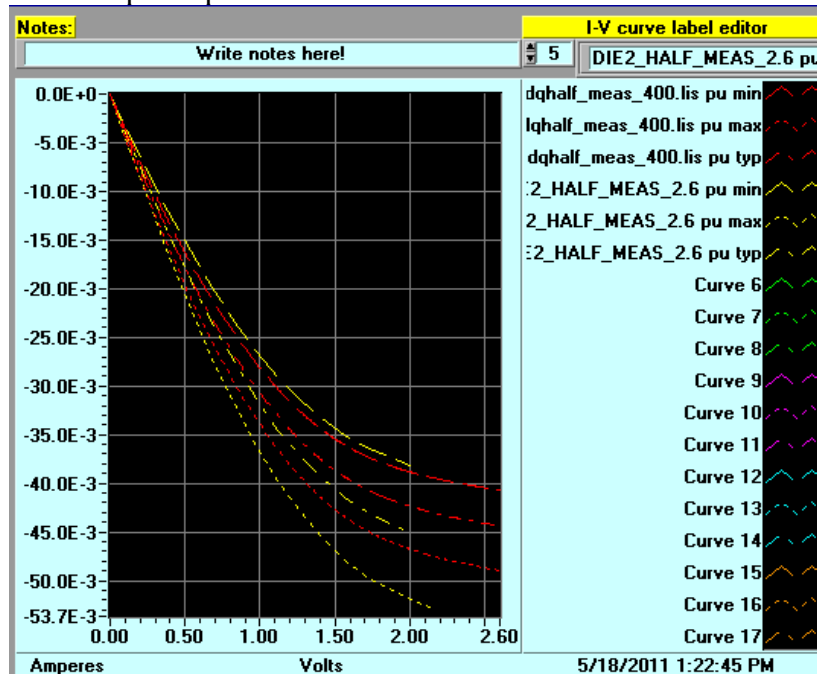


ii. Pulldown comparison

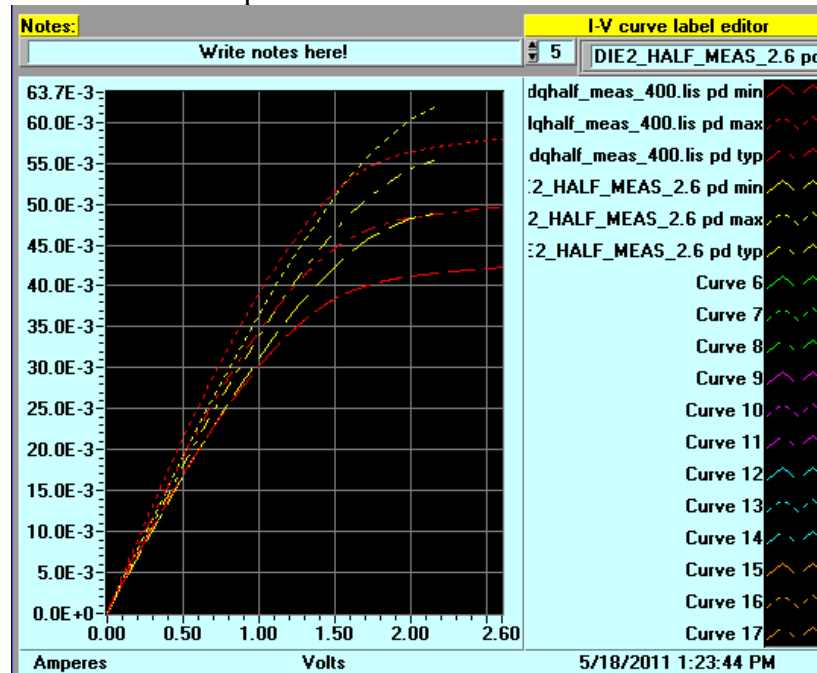


d. Model name: **DQHALF\_400**

i. Pullup comparison



ii. Pulldown comparison



2. ☒ Compare C\_comp with measured C\_comp. Provide C\_comp comparison table for all models and for all package combinations (i.e x4, x8 and x16).

Component name: **MT46V16M16CV ( 60/108 FBGA 16Mx16 )**

		IBIS			Measured		
		min	typ	max	min	typ	max
<b>DQ</b>	C_comp	3.53	3.38	3.68	NA	NA	NA
	C_package	0.71	0.45	0.99	NA	NA	NA
	C_total	4.24	3.83	4.67	3.95	4.24	4.63
<b>INPUT</b>	C_comp	1.33	1.23	1.43	NA	NA	NA
	C_package	0.75	0.52	0.95	NA	NA	NA
	C_total	2.08	1.76	2.38	1.90	2.08	2.22
<b>CLK</b>	C_comp	1.51	1.41	1.61	NA	NA	NA
	C_package	0.58	0.57	0.58	NA	NA	NA
	C_total	2.09	1.99	2.20	2.05	2.09	2.16

Component name: **MT46V16M16TG (T66A 66 TSOP 16Mx16 )**

		IBIS			Measured		
		min	typ	max	min	typ	max
<b>DQ</b>	C_comp	3.53	3.38	3.68	NA	NA	NA
	C_package	0.80	0.50	1.26	NA	NA	NA
	C_total	4.34	3.88	4.94	3.90	4.22	4.53
<b>INPUT</b>	C_comp	1.33	1.23	1.43	NA	NA	NA
	C_package	0.90	0.74	1.15	NA	NA	NA
	C_total	2.24	1.98	2.59	2.09	2.26	2.51
<b>CLK</b>	C_comp	1.51	1.41	1.61	NA	NA	NA
	C_package	0.74	0.74	0.75	NA	NA	NA
	C_total	2.26	2.15	2.36	2.10	2.16	2.24

3. ☐ If measured clamp current data is available provide an IBIS and measurement comparison for all models.

**Not Available**

a. Model name:

- Power-clamp comparison image
- Gnd-clamp comparison image

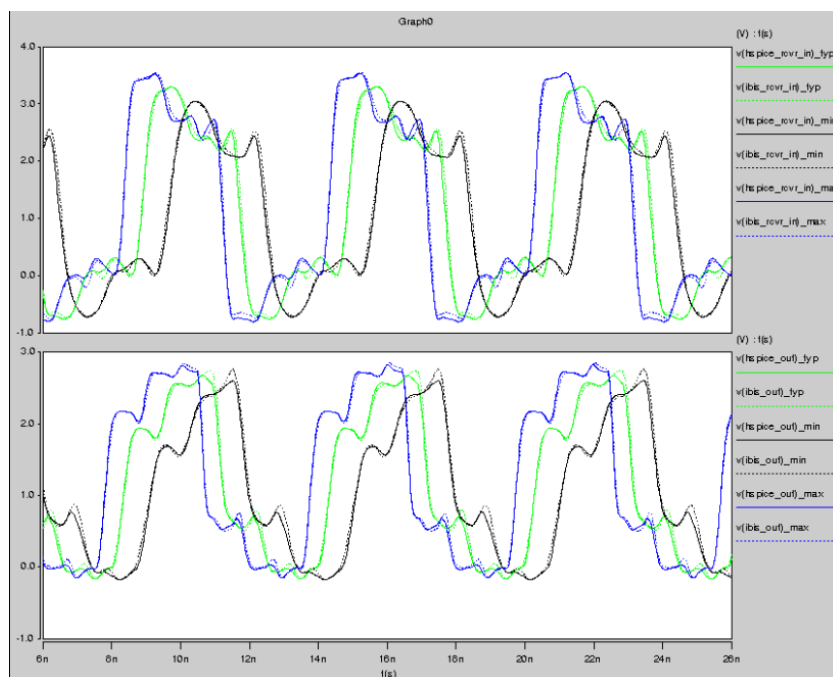
4. ☐ If slew rate data (rise/fall slew) is available from measurements, complete HSpice simulations to generate slew rate data and provide a comparison table.

**Not Available**

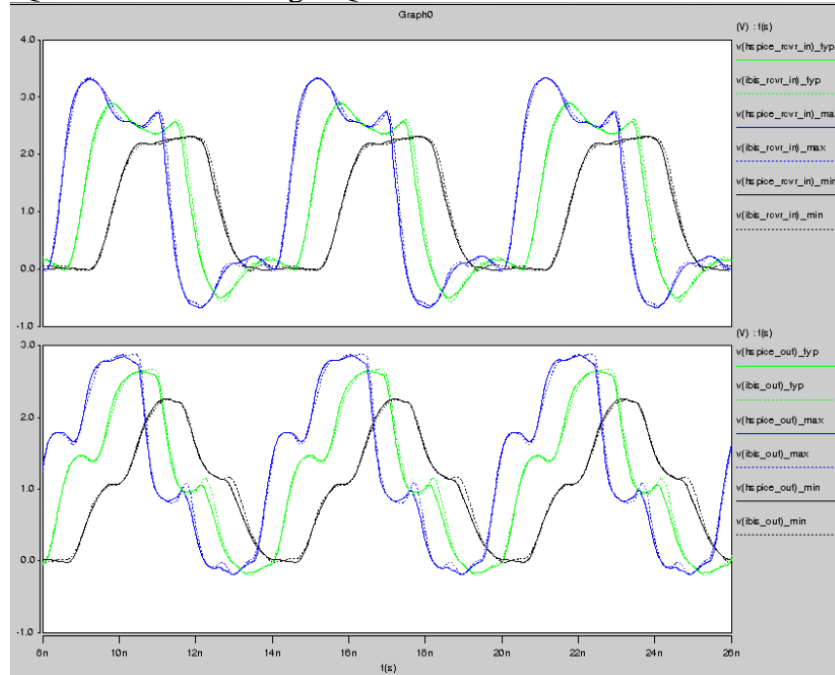
		IBIS			Measurement	
Model	Slew Rate (V/ns)	min	typ	max	min	max
<b>DQ_FULL</b>	Rising					
	Falling					
<b>DQ_HALF</b>	Rising					
	Falling					

## IBIS vs HSPICE Correlation

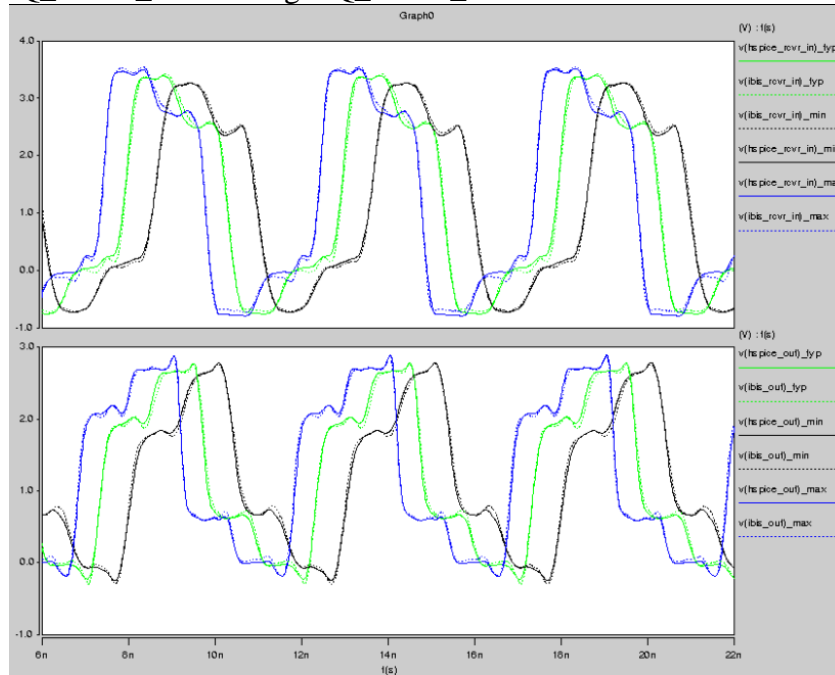
1. ☒ For all Output or I/O models, run HSpice transient simulations using encrypted netlists and the IBIS model (b-element).
  - a. ☒ Use the setup and node naming conventions shown below for the IBIS and HSpice deck file (.sp file). Update the setup diagram if it is different. Indicate the version of HSPICE simulator used for simulations: **2008.09**
  - b. ☒ Run simulations for all corners cases and at maximum allowable speed grade
    - i. DQ\_FULL\_333 driving DQ\_FULL\_333



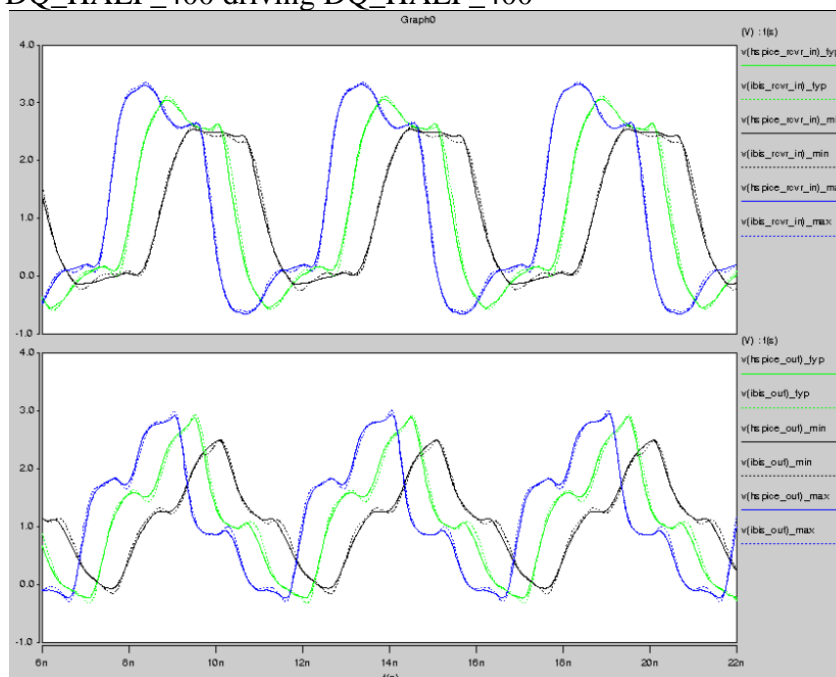
ii. DQ\_HALF\_333 driving DQ\_HALF\_333



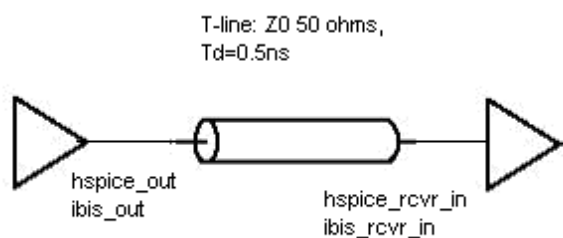
iii. DQ\_FULL\_400 driving DQ\_FULL\_400



iv. DQ\_HALF\_400 driving DQ\_HALF\_400



## Setup



**Comments:** Model is compared to Silicon and Datasheet requirements.  
The driver impedance is calibrated within expected tolerances.

## Document Revision History

Rev 2.0 - Date 05/30/2011

- IBIS revision 2.0
- HSpipe revision 2.0

Rev 2.1 - Date 09/03/2019

- IBIS revision 2.1
- HSpipe revision 2.0