DDR5 SDRAM RDIMM Addendum

MTC40F204WS1RC – 96GB
24Gb Die Revision B

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 RDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 RDIMM core data sheet
- 288-pin, DDR5 registered dual in-line memory module (DDR5 RDIMM)
- Fast data transfer rate: PC5-4800, PC5-5600, PC5-6400
- 96GB (12Gig x 80)
- Dual-rank
- 32 internal banks; 8 groups of 4 banks each

Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	C
• Frequency/CAS latency	
– 0.416ns @ CL = 40 (DDR5-4800)	48B
– 0.357ns @ CL = 46 (DDR5-5600)	56B
– 0.312ns @ CL = 52 (DDR5-6400)	64B

Figure 1: 288-Pin DDR5 RDIMM (R/C-A0)

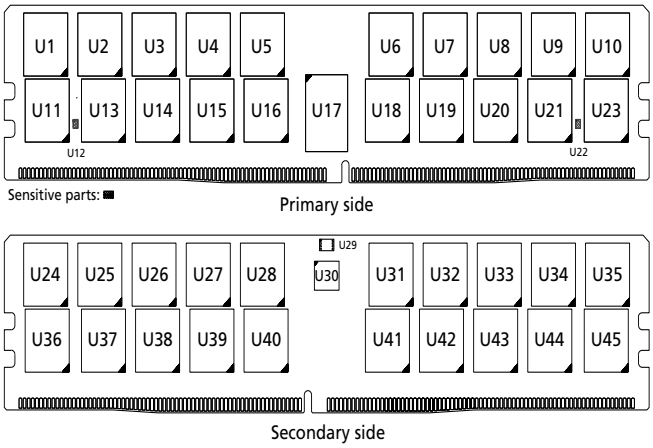

Figure 2: 288-Pin DDR5 RDIMM (R/C-A1)

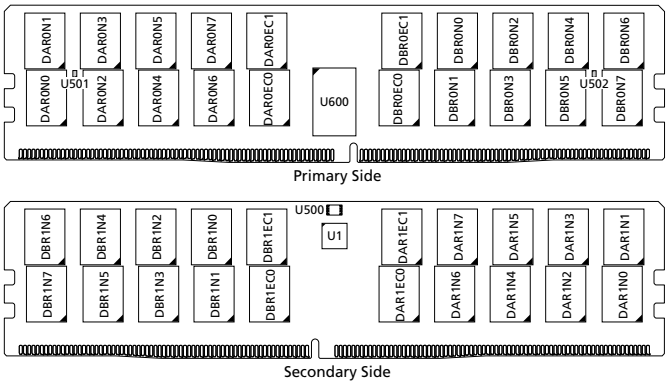

Table 1: Addressing

Parameter	96GB
Row address	96K (R0-R16)[1]
Column address	2K (C0-C10)
Device bank group address	8 (BG0-BG2)
Device bank address per bank group	4 (BA0-BA1)
Device configuration	24Gb (6Gb x 4), 32 banks
Module rank address	2 (CS0_n, CS1_n)

Notes: 1. For non-binary densities, a quarter of the row address space is invalid. When the MSB address bit is HIGH, the MSB-1 address shall be LOW.

Table 2: Part Numbers and Timing Parameters – 96GB Modules

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles ($CL-_nRCD-_nRP$)	Designation[2]
MTC40F204WS1RC48BB1	96GB	12Gb x 80 (EC8)	38.4 GB/s	0.416ns/4800 MT/s	40-39-39	Production
MTC40F204WS1RC56BB1	96GB	12Gb x 80 (EC8)	44.8 GB/s	0.357ns/5600 MT/s	46-45-45	Preliminary
MTC40F204WS1RC64BB1	96GB	12Gb x 80 (EC8)	51.2 GB/s	0.312ns/6400 MT/s	52-52-52	Preliminary
MTC40F204WS1RC64BB2	96GB	12Gb x 80 (EC8)	51.2 GB/s	0.312ns/6400 MT/s	52-52-52	Preliminary

Notes: 1. Base device: MT60B6G4, 24Gb DDR5 SDRAM Die Revision B. The data sheet for the base device can be found on micron.com.
2. **Production**: Although considered final, these specifications are subject to change as further product development and data characterization sometimes occur. **Preliminary**: For evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications. **Advance**: Contains initial descriptions of products still under development. For evaluation purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specification.

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DQ Map

Table 3: Component-to-Module DQ Map (R/C A-0)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	7A	161	U2	0	15A	172
	1	4A	14		1	12A	25
	2	6A	159		2	14A	170
	3	5A	16		3	13A	27
U3	0	23A	183	U4	0	31A	194
	1	20A	36		1	28A	47
	2	22A	181		2	30A	192
	3	21A	38		3	29A	49
U5	0	CB7A	205	U6	0	CB7B	236
	1	CB4A	58		1	CB4B	89
	2	CB6A	203		2	CB6B	234
	3	CB5A	60		3	CB5B	91
U7	0	3B	247	U8	0	11B	258
	1	0B	100		1	8B	111
	2	2B	245		2	10B	256
	3	1B	102		3	9B	113
U9	0	19B	269	U10	0	27B	280
	1	16B	122		1	24B	133
	2	18B	267		2	26B	278
	3	17B	124		3	25B	135
U11	0	3A	154	U13	0	11A	165
	1	0A	7		1	8A	18
	2	2A	152		2	10A	163
	3	1A	9		3	9A	20
U14	0	19A	176	U15	0	27A	187
	1	16A	29		1	24A	40
	2	18A	174		2	26A	185
	3	17A	31		3	25A	42
U16	0	CB3A	198	U18	0	CB3B	243
	1	CB0A	51		1	CB0B	96
	2	CB2A	196		2	CB2B	241
	3	CB1A	53		3	CB1B	98

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U19	0	7B	254	U20	0	15B	265
	1	4B	107		1	12B	118
	2	6B	252		2	14B	263
	3	5B	109		3	13B	120
U21	0	23B	276	U23	0	31B	287
	1	20B	129		1	28B	140
	2	22B	274		2	30B	285
	3	21B	131		3	29B	142
U24	0	24B	133	U25	0	16B	122
	1	27B	280		1	19B	269
	2	25B	135		2	17B	124
	3	26B	278		3	18B	267
U26	0	8B	111	U27	0	0B	100
	1	11B	258		1	3B	247
	2	9B	113		2	1B	102
	3	10B	256		3	2B	245
U28	0	CB4B	89	U31	0	CB4A	58
	1	CB7B	236		1	CB7A	205
	2	CB5B	91		2	CB5A	60
	3	CB6B	234		3	CB6A	203
U32	0	28A	47	U33	0	20A	36
	1	31A	194		1	23A	183
	2	29A	49		2	21A	38
	3	30A	192		3	22A	181
U34	0	12A	25	U35	0	4A	14
	1	15A	172		1	7A	161
	2	13A	27		2	5A	16
	3	14A	170		3	6A	159
U36	0	28B	140	U37	0	20B	129
	1	31B	287		1	23B	276
	2	29B	142		2	21B	131
	3	30B	285		3	22B	274
U38	0	12B	118	U39	0	4B	107
	1	15B	265		1	7B	254
	2	13B	120		2	5B	109
	3	14B	263		3	6B	252

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U40	0	CB0B	96	U41	0	CB0A	51
	1	CB3B	243		1	CB3A	198
	2	CB1B	98		2	CB1A	53
	3	CB2B	241		3	CB2A	196
U42	0	24A	40	U43	0	16A	29
	1	27A	187		1	19A	176
	2	25A	42		2	17A	31
	3	26A	185		3	18A	174
U44	0	8A	18	U45	0	0A	7
	1	11A	165		1	3A	154
	2	9A	20		2	1A	9
	3	10A	163		3	2A	152

Table 4: Component-to-Module DQ Map (R/C A-1)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
DAR0EC0	0	CB3A	198	DAR0EC1	0	CB7A	205
	1	CB0A	51		1	CB4A	58
	2	CB2A	196		2	CB6A	203
	3	CB1A	53		3	CB5A	60
DAR0N0	0	3A	154	DAR0N1	0	7A	161
	1	0A	7		1	4A	14
	2	2A	152		2	6A	159
	3	1A	9		3	5A	16
DAR0N2	0	11A	165	DAR0N3	0	15A	172
	1	8A	18		1	12A	25
	2	10A	163		2	14A	170
	3	9A	20		3	13A	27
DAR0N4	0	19A	176	DAR0N5	0	23A	183
	1	16A	29		1	20A	36
	2	18A	174		2	22A	181
	3	17A	31		3	21A	38

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
DAR0N6	0	27A	187	DAR0N7	0	31A	194
	1	24A	40		1	28A	47
	2	26A	185		2	30A	192
	3	25A	42		3	29A	49
DAR1EC0	0	CB0A	51	DAR1EC1	0	CB4A	58
	1	CB3A	198		1	CB7A	205
	2	CB1A	53		2	CB5A	60
	3	CB2A	196		3	CB6A	203
DAR1N0	0	0A	7	DAR1N1	0	4A	25
	1	3A	154		1	7A	172
	2	1A	9		2	5A	27
	3	2A	152		3	6A	170
DAR1N2	0	8A	18	DAR1N3	0	12A	25
	1	11A	165		1	15A	172
	2	9A	20		2	13A	27
	3	10A	163		3	14A	170
DAR1N4	0	16A	29	DAR1N5	0	20A	36
	1	19A	176		1	23A	183
	2	17A	31		2	21A	38
	3	18A	174		3	22A	181
DAR1N6	0	24A	40	DAR1N7	0	28A	47
	1	27A	187		1	31A	194
	2	25A	42		2	29A	49
	3	26A	185		3	30A	192
DBR0EC0	0	CB3B	243	DBR0EC1	0	CB7B	236
	1	CB0B	96		1	CB4B	89
	2	CB2B	241		2	CB6B	234
	3	CB1B	98		3	CB5B	91
DBR0N0	0	3B	247	DBR0N1	0	7B	254
	1	0B	100		1	4B	107
	2	2B	245		2	6B	252
	3	1B	102		3	5B	109
DBR0N2	0	11B	258	DBR0N3	0	15B	265
	1	8B	111		1	12B	118
	2	10B	256		2	14B	263
	3	9B	113		3	13B	120

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
DBR0N4	0	19B	269	DBR0N5	0	23B	276
	1	16B	122		1	20B	129
	2	18B	267		2	22B	274
	3	17B	124		3	21B	131
DBR0N6	0	27B	280	DBR0N7	0	31B	287
	1	24B	133		1	28B	140
	2	26B	278		2	30B	285
	3	25B	135		3	29B	142
DBR1EC0	0	CB0B	96	DBR1EC1	0	CB4B	89
	1	CB3B	243		1	CB7B	236
	2	CB1B	98		2	CB5B	91
	3	CB2B	241		3	CB6B	234
DBR1N0	0	0B	100	DBR1N1	0	4B	107
	1	3B	247		1	7B	254
	2	1B	102		2	5B	109
	3	2B	245		3	6B	252
DBR1N2	0	8B	111	DBR1N3	0	12B	118
	1	11B	258		1	15B	265
	2	9B	113		2	13B	120
	3	10B	256		3	14B	263
DBR1N4	0	16B	122	DBR1N5	0	20B	129
	1	19B	269		1	23B	276
	2	17B	124		2	21B	131
	3	18B	267		3	22B	274
DBR1N6	0	24B	133	DBR1N7	0	28B	140
	1	27B	280		1	31B	287
	2	25B	135		2	29B	142
	3	26B	278		3	30B	285

I_{DD} Specifications

Table 5: DDR5 I_{DD} Specifications and Conditions – 96GB (Die Revision B)

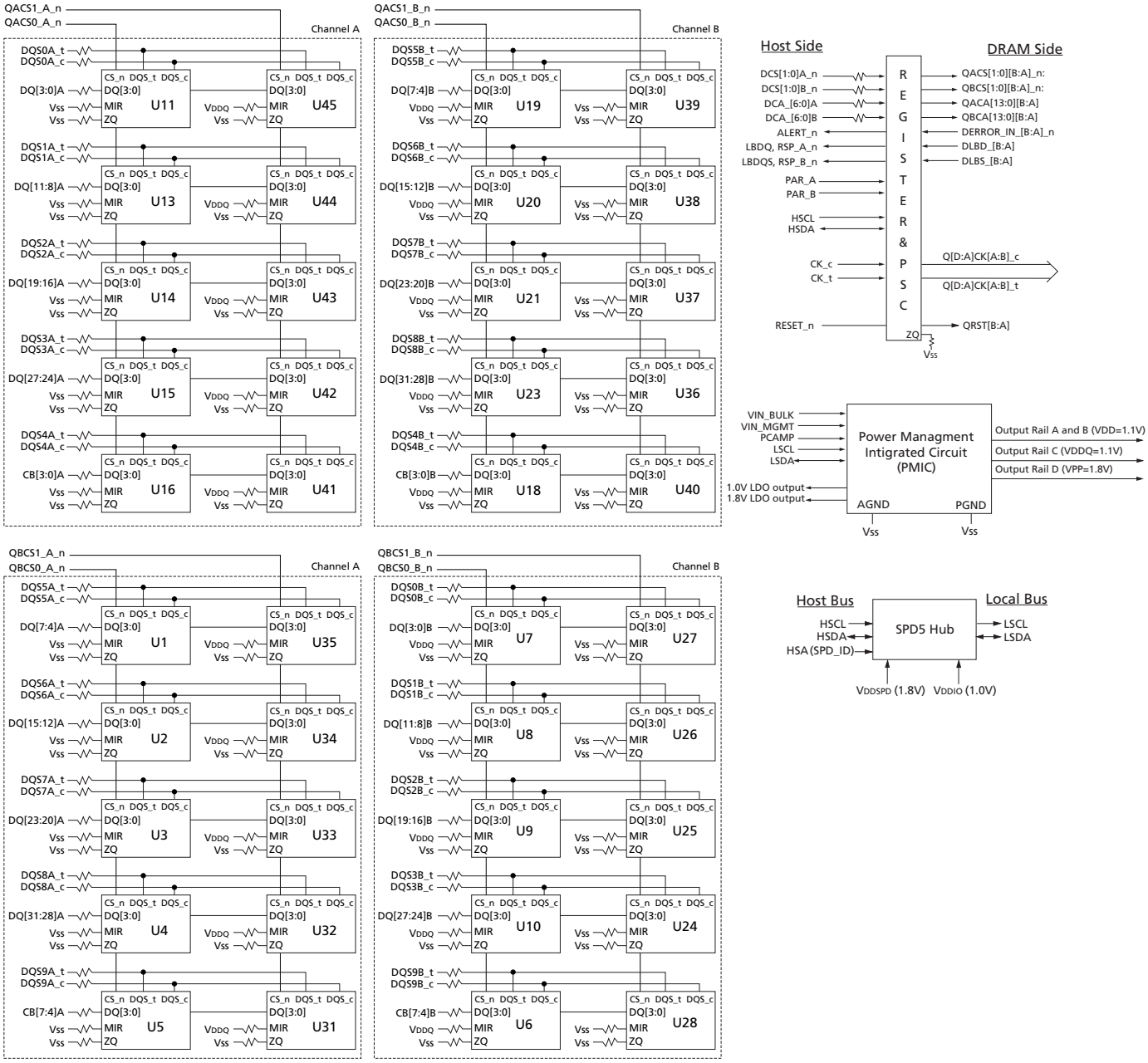
Module I_{DD} is based on PMIC VIN_BULK 12V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency, RCD current and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	5600	6400	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}[1]	443	TBD	TBD	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}[1]	520	TBD	TBD	mA
Precharge standby current	I_{DD2N}[2]	414	TBD	TBD	mA
Precharge standby non-target command	I_{DD2NT}[1]	494	TBD	TBD	mA
Precharge power-down current	I_{DD2P}[2]	409	TBD	TBD	mA
Active standby current	I_{DD3N}[2]	470	TBD	TBD	mA
Active power-down current	I_{DD3P}[2]	465	TBD	TBD	mA
Operating burst read current	I_{DD4R}[1]	901	TBD	TBD	mA
Operating burst write current	I_{DD4W}[1]	1058	TBD	TBD	mA
Operating burst write with write CRC current	I_{DD4WC}[1]	1055	TBD	TBD	mA
Burst refresh (normal refresh mode) current	I_{DD5B}[1]	884	TBD	TBD	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}[1]	858	TBD	TBD	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}[1]	554	TBD	TBD	mA
Self refresh current	I_{DD6N}[2]	345	TBD	TBD	mA
Operating bank interleave read current	I_{DD7}[1]	1220	TBD	TBD	mA
Maximum power saving deep power down mode current	I_{DD8}[2]	328	TBD	TBD	mA

Notes: 1. One module rank in this $I_{DD}/I_{DDQ}/I_{PP}$ condition, the other rank in $I_{DD2N}/I_{DDQ2N}/I_{PP2N}$.
2. Both ranks in this $I_{DD}/I_{DDQ}/I_{PP}$ condition.

Functional Block Diagram

Figure 3: Functional Block Diagram



Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

Revision History

Rev. D – 01/2024

- Added 6400 MPN with PCB tie bar change

Rev. C – 01/2023

- Added IDD limits for 48B, and changed part status for 48B to "Production"
- Removed Micron Confidential marking
- Changed data sheet status to Production

Rev. B – 11/2022

- Added MIR state to Functional Block Diagram
- Added PCB drawing to Features page
- Added values for R/C A-1 DQ map

Rev. A – 04/2022

- Preliminary Release

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