DDR5 SDRAM RDIMM Addendum

MTC10F108YS1RC – 24GB
24Gb Die Revision B

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 RDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 RDIMM core data sheet
- 288-pin, DDR5 registered dual in-line memory module (DDR5 RDIMM)
- Fast data transfer rate: PC5-4800, PC5-5600, PC5-6400
- 24GB (3 Gig x 80)
- Single-rank
- 32 internal banks; 8 groups of 4 banks each

Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	C
• Frequency/CAS latency	
– 0.416ns @ CL = 40 (DDR5-4800)	48B
– 0.357ns @ CL = 46 (DDR5-5600)	56B
– 0.312ns @ CL = 52 (DDR5-6400)	64B

Figure 1: 288-Pin DDR5 RDIMM (R/C-D0)

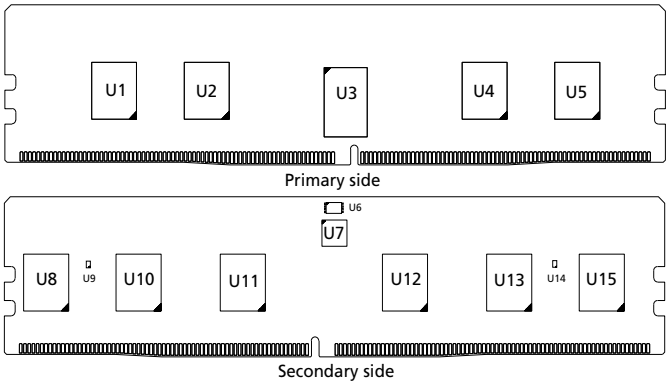

Figure 2: 288-Pin DDR5 RDIMM (R/C-D1)

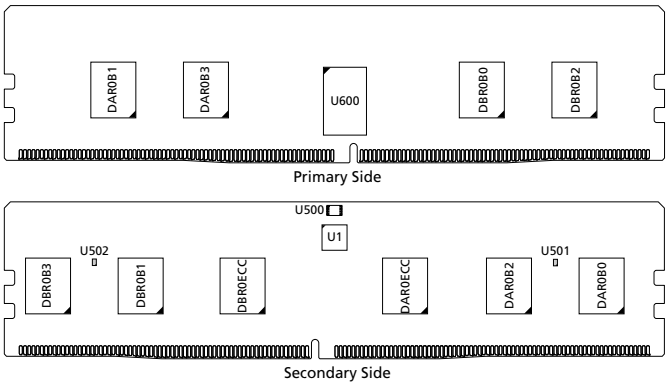

Table 1: Addressing

Parameter	24GB
Row address[1]	96K (R0-R16)[2]
Column address[1]	1K (C0-C9)
Device bank group address[1]	8 (BG0-BG2)
Device bank address per bank group[1]	4 (BA0-BA1)
Device configuration	24Gb (3Gb x 8), 32 banks
Module rank address	1 (CS0_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.
2. For non-binary densities, a quarter of the row address space is invalid. When the MSB address bit is HIGH, the MSB-1 address shall be LOW.

Table 2: Part Numbers and Timing Parameters – 24GB Modules

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles ($CL-_nRCD-_nRP$)	Designation[2]
MTC10F108YS1RC48BB1	24GB	3Gb x 80	38.4 GB/s	0.416ns/4800 MT/s	40-39-39	Production
MTC10F108YS1RC56BB1	24GB	3Gb x 80	44.8 GB/s	0.357ns/5600 MT/s	46-45-45	Preliminary
MTC10F108YS1RC64BB1	24GB	3Gb x 80	51.2 GB/s	0.312ns/6400 MT/s	52-52-52	Preliminary
MTC10F108YS1RC64BB2	24GB	3Gb x 80	51.2 GB/s	0.312ns/6400 MT/s	52-52-52	Preliminary

Notes: 1. Base device: MT60B6G4, 24Gb DDR5 SDRAM Die Revision B. The data sheet for the base device can be found on micron.com.
2. **Production**: Although considered final, these specifications are subject to change as further product development and data characterization sometimes occur. **Preliminary**: For evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications. **Advance**: Contains initial descriptions of products still under development. For evaluation purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specification.

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DQ Map

Table 3: Component-to-Module DQ Map (R/C-D0)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	9A	20	U2	0	25A	42
	1	10A	163		1	26A	185
	2	11A	165		2	27A	187
	3	8A	18		3	24A	40
	4	15A	172		4	31A	194
	5	12A	25		5	28A	47
	6	13A	27		6	29A	49
	7	14A	170		7	30A	192
U4	0	1B	102	U5	0	17B	124
	1	2B	245		1	18B	267
	2	3B	247		2	19B	269
	3	0B	100		3	16B	122
	4	7B	254		4	23B	276
	5	4B	107		5	20B	129
	6	5B	109		6	21B	131
	7	6B	252		7	22B	274
U8	0	26B	278	U10	0	10B	256
	1	25B	135		1	9B	113
	2	24B	133		2	8B	111
	3	27B	280		3	11B	258
	4	28B	140		4	12B	118
	5	31B	287		5	15B	265
	6	30B	285		6	14B	263
	7	29B	142		7	13B	120
U11	0	CB6B	234	U12	0	CB2A	196
	1	CB5B	91		1	CB1A	53
	2	CB4B	89		2	CB0A	51
	3	CB7B	236		3	CB3A	198
	4	CB0B	96		4	CB4A	58
	5	CB3B	243		5	CB7A	205
	6	CB2B	241		6	CB6A	203
	7	CB1B	98		7	CB5A	60

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U13	0	18A	174	U15	0	2A	152
	1	17A	31		1	1A	9
	2	16A	29		2	0A	7
	3	19A	176		3	3A	154
	4	20A	36		4	4A	14
	5	23A	183		5	7A	161
	6	22A	181		6	6A	159
	7	21A	38		7	5A	16

Table 4: Component-to-Module DQ Map (R/C-D1)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
DAR0B0	0	2A	152	DAR0B1	0	9A	20
	1	1A	9		1	10A	163
	2	0A	7		2	11A	165
	3	3A	154		3	8A	18
	4	4A	14		4	15A	172
	5	7A	161		5	12A	25
	6	6A	159		6	13A	27
	7	5A	16		7	14A	170
DAR0B2	0	18A	174	DAR0B3	0	25A	42
	1	17A	31		1	26A	185
	2	16A	29		2	27A	187
	3	19A	176		3	24A	40
	4	20A	36		4	31A	194
	5	23A	183		5	28A	47
	6	22A	181		6	29A	49
	7	21A	38		7	30A	192
DAR0ECC	0	CB2A	196	DBR0B0	0	1B	102
	1	CB1A	53		1	2B	245
	2	CB0A	51		2	3B	247
	3	CB3A	198		3	0B	100
	4	CB4A	58		4	7B	254
	5	CB7A	205		5	4B	107
	6	CB6A	203		6	5B	109
	7	CB5A	60		7	6B	252
DBR0B1	0	10B	256	DBR0B2	0	17B	124
	1	9B	113		1	18B	267
	2	8B	111		2	19B	269
	3	11B	258		3	16B	122
	4	12B	118		4	23B	276
	5	15B	265		5	20B	129
	6	14B	263		6	21B	131
	7	13B	120		7	22B	274

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
DBR0B3	0	26B	278	DBR0ECC	0	CB6B	234
	1	25B	135		1	CB5B	91
	2	24B	133		2	CB4B	89
	3	27B	280		3	CB7B	236
	4	28B	140		4	CB0B	96
	5	31B	287		5	CB3B	243
	6	30B	285		6	CB2B	241
	7	29B	142		7	CB1B	98

I_{DD} Specifications

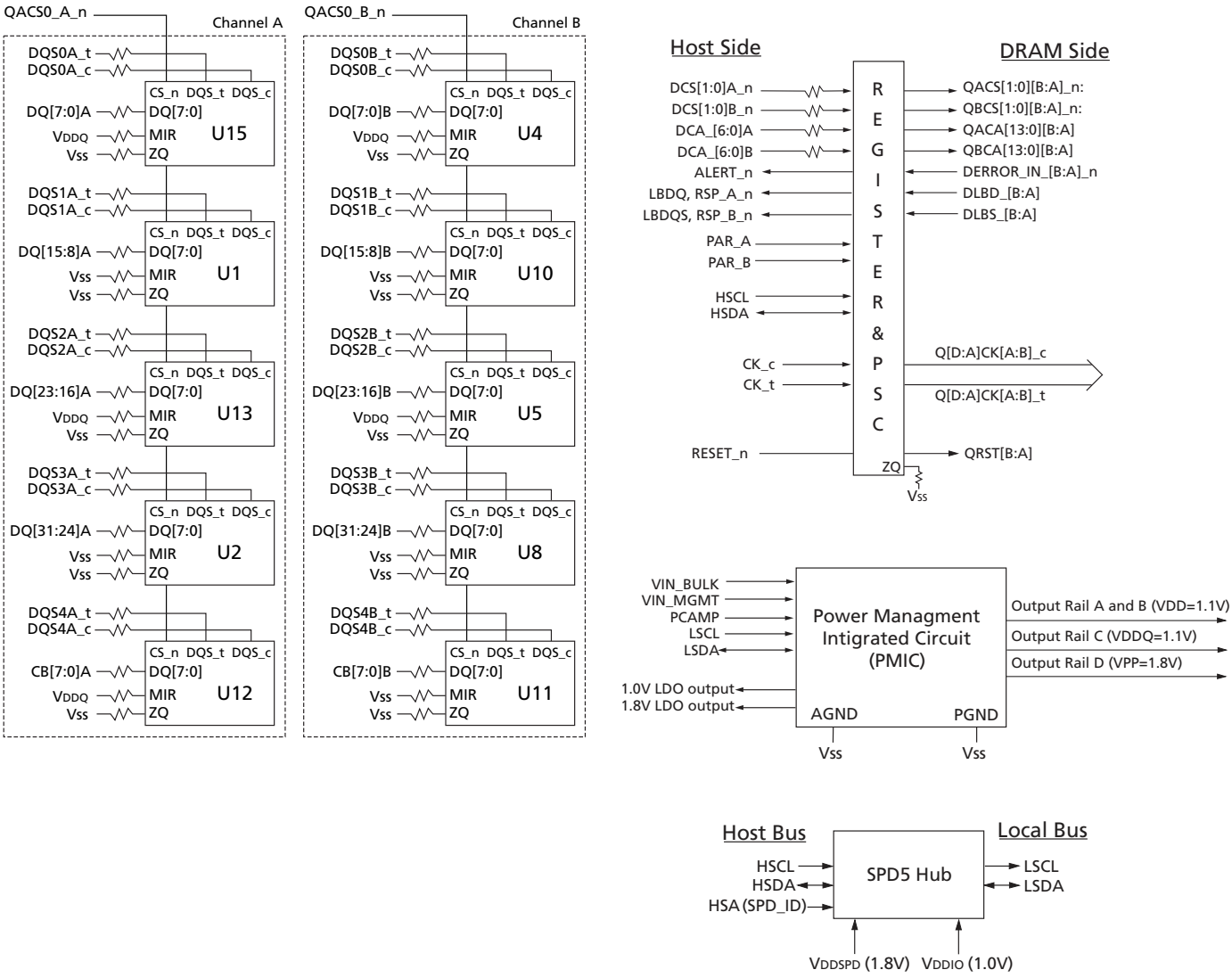
Table 5: DDR5 I_{DD} Specifications and Conditions – 24GB (Die Revision B)

Module I_{DD} is based on PMIC VIN_BULK 12V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency, RCD current and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	5600	6400	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}	196	TBD	TBD	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}	234	TBD	TBD	mA
Precharge standby current	I_{DD2N}	189	TBD	TBD	mA
Precharge standby non-target command	I_{DD2NT}	221	TBD	TBD	mA
Precharge power-down current	I_{DD2P}	178	TBD	TBD	mA
Active standby current	I_{DD3N}	189	TBD	TBD	mA
Active power-down current	I_{DD3P}	187	TBD	TBD	mA
Operating burst read current	I_{DD4R}	468	TBD	TBD	mA
Operating burst write current	I_{DD4W}	592	TBD	TBD	mA
Operating burst write with write CRC current	I_{DD4WC}	568	TBD	TBD	mA
Burst refresh (normal refresh mode) current	I_{DD5B}	414	TBD	TBD	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}	413	TBD	TBD	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}	241	TBD	TBD	mA
Self refresh current	I_{DD6N}	105	TBD	TBD	mA
Operating bank interleave read current	I_{DD7}	600	TBD	TBD	mA
Maximum power saving deep power down mode current	I_{DD8}	172	TBD	TBD	mA

Functional Block Diagram

Figure 3: Functional Block Diagram



Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

Revision History

Rev. D – 01/2024

- Added 6400 MPN with PCB tie bar change

Rev. C – 01/2023

- Added IDD limits for 48B, and changed part status for 48B to "Production"
- Removed Micron Confidential marking
- Changed data sheet status to Production

Rev. B – 11/2022

- Added MIR state to Functional Block Diagram
- Added PCB drawing to Features page
- Added values for R/C D-1 DQ map

Rev. A – 04/2022

- Preliminary Release

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