High Bandwidth Memory with ECC

MT54A8G8040A00BF — 8 channels × 64 Meg × 144 I/O
MT54A16G8080A00AC — 8 channels × 128 Meg × 144 I/O

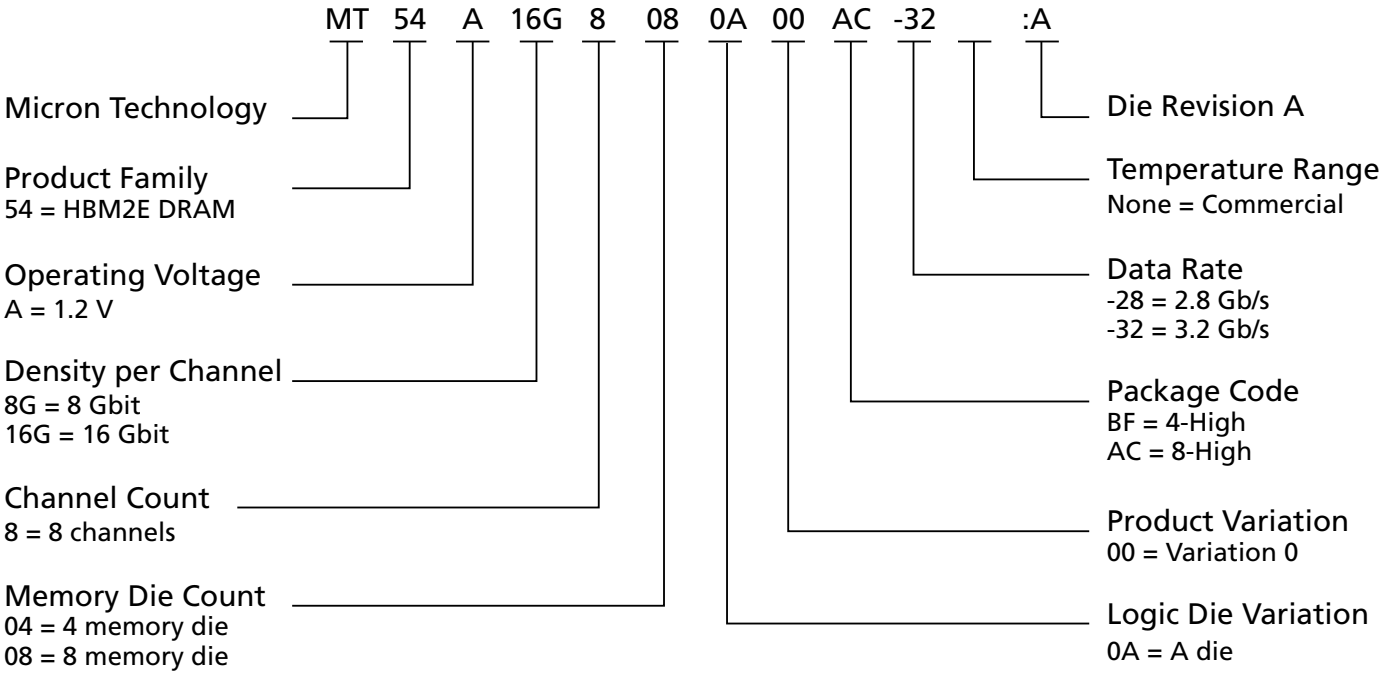
Features

- $V_{DDC} = V_{DDQ} = 1.2V \pm 5\%$
- $V_{PP} = 2.5V -5\%/+10\%$
- Data rate: 2.8 Gb/s and 3.2 Gb/s
- Peak bandwidths: 358 GB/s and 410 GB/s
- ECC support: 9 memory bits per byte
- 8 independent channels with pseudo channel mode
  - 256 bits per array read or write access
- Bank Count:
  - 4-High (8 GB): 16 banks in 4 bank groups
  - 8-High (16 GB): 32 banks in 8 bank groups
- Differential clock input CK_t/CK_c for command/address
- Semi-independent row and column command interfaces allowing ACT/PRE command to be issued in parallel with READ/WRITE commands
- Double data rate (DDR) command and address (CK)
- Differential write data strobes WDQS_t/WDQS_c and read data strobes RDQS_t/RDQS_c, each associated with four data bytes
- DDR data (WDQS, RDQS)
- Programmable READ latency (RL)
- Programmable WRITE latency (WL)
- Programmable parity latency (PL)
- Burst length = 4
- Write data mask function with single byte granularity
- Data bus inversion (DBIac) for writes and reads
- Parity for command/address and data monitoring
- Auto precharge option for each burst access
- Auto refresh mode (32ms, 8k cycles) with single bank refresh option
- Temperature sensor controlled self refresh rate
- ^{t}RAS lockout
- Programmable output driver strength
- Unterminated clock, command, address, and data interfaces
- Temperature sensor with read-out
- IEEE 1500 standard serial test interface

Options[1]	Marking
• Density per channel	
– 8 Gb (9 Gb with ECC)	8G
– 16 Gb (18 Gb with ECC)	16G
• Stack height	
– 4 DRAM layers	04
– 8 DRAM layers	08
• Microbump package	
– 4-High (8 GB)	BF
– 8-High (16 GB)	AC
• Per-pin data rate	
– 2.8 Gb/s	-28
– 3.2 Gb/s	-32
• Operating temperature	
– Commercial ($0°C \le T_{OPER} \le +95°C$)	None
• Revision	A

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Figure 1: Part Numbering



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Signal Descriptions

Table 1: HBM2 Signal Descriptions

Symbol	Type	Description
Per-Channel Signals		
CK[a:h]_t, CK[a:h]_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. Row and column command and address inputs are latched on the rising and falling edges of CK. CKE is latched on the rising edge of CK only. All latencies are referenced to the rising edge of CK.
CKE[a:h]	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock, device input buffers, and output drivers. Taking CKE LOW provides precharge power-down and SELF REFRESH operations (all banks idle), or active power-down (row activated in any bank). CKE must be maintained HIGH throughout read and write accesses.
C[a:h][8:0]	Input	**Column command and address:** The command code, bank and column address for WRITE and READ operations, and the mode register address and code to be loaded with MODE REGISTER SET commands are received on the C[8:0] inputs.
R[a:h][6:0]	Input	**Row command and address:** The command code, bank and row address for ACTIVATE, PRECHARGE, and REFRESH commands are received on the R[6:0] inputs.
DQ[a:h][127:0]	I/O	**Data input/output:** 128-bit data bus
DBI[a:h][15:0]	I/O	**Data bus inversion:** DBI0 is associated with DQ[7:0], DBI1 is associated with DQ[15:8], ... , and DBI15 is associated with DQ[127:120].
DM[a:h][15:0]	I/O	**Data mask or ECC data:** DM0 is associated with [7:0], DM1 is associated with [15:8], ... , and DM15 is associated with [127:120].
PAR[a:h][3:0]	I/O	**Data parity:** One data parity bit per DWord. PAR0 is associated with DQ[31:0], PAR1 is associated with DQ[63:32], PAR2 is associated with DQ[95:64], and PAR3 is associated with DQ[127:96].
DERR[a:h][3:0]	Output	**Data parity error:** One data parity error bit per DWord. DERR0 is associated with DQ[31:0], DERR1 is associated with DQ[63:32], DERR2 is associated with DQ[95:64], and DERR3 is associated with DQ[127:96].
AERR[a:h]	Output	**Address parity error:** One address parity error bit for row and column address and command per channel.
WDQS[a:h][3:0]_t, WDQS[a:h][3:0]_c	Input	**Write data strobe:** WDQS_t and WDQS_c are differential strobe inputs. Write input data are latched on the rising and falling edges of WDQS. One WDQS pair per DWord. WDQS0_t/_c are associated with DQ[31:0], WDQS1_t/_c are associated with DQ[63:32], WDQS2_t/_c are associated with DQ[95:64], and WDQS3_t/_c are associated with DQ[127:96].

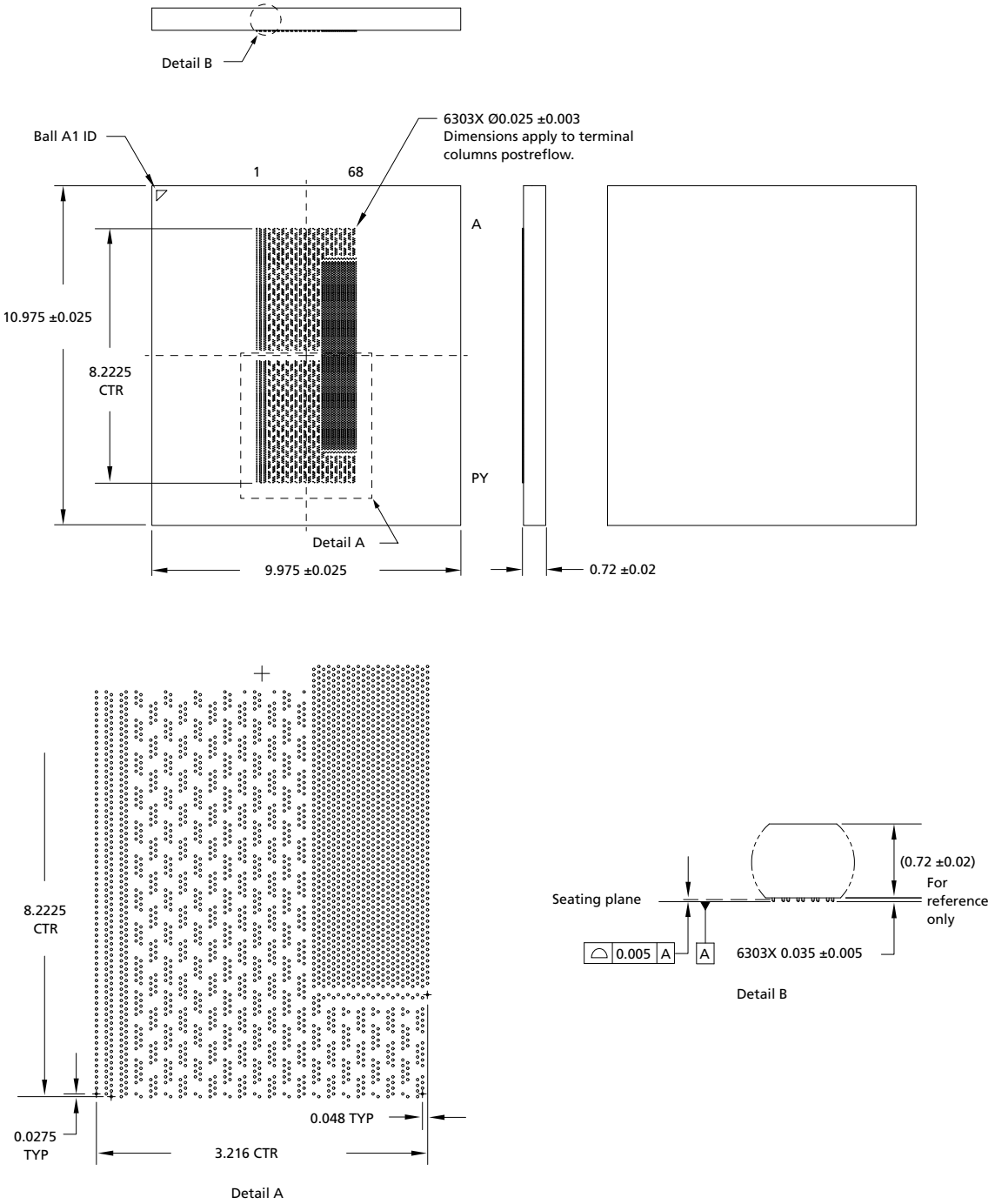
Table 1: HBM2 Signal Descriptions (Continued)

Symbol	Type	Description
RDQS[a:h][3:0]_t, RDQS[a:h][3:0]_c	Output	**Read data strobe:** RDQS_t and RDQS_c are differential strobe outputs. Read output data are sent on the rising and falling edges of RDQS. One RDQS pair per DWord. RDQS0_t/_c are associated with DQ[31:0], RDQS1_t/_c are associated with DQ[63:32], RDQS2_t/_c are associated with DQ[95:64], and RDQS3_t/_c are associated with DQ[127:96].
RD[a:h][7:0]	I/O	Redundant microbumps in DWORD
RC[a:h]	Input	Redundant column command and address microbump in AWORD
RR[a:h]	Input	Redundant row command and address microbump in AWORD
Global Signals		
DA[59:0]	I/O	**Direct access input/output:** These pins are provided for direct access test.
RESET_n	Input	**Reset:** RESET_n LOW asynchronously initiates a full chip reset of the HBM device.
TEMP[2:0]	Output	DRAM temperature report
CATTRIP	Output	DRAM catastrophic temperature report
WRCK	Input	IEEE-1500 wrapper serial port clock
WRST_n	Input	IEEE-1500 wrapper serial port reset
SELECTWIR	Input	IEEE-1500 wrapper serial port instruction register select
SHIFTWR	Input	IEEE-1500 wrapper serial port shift
CAPTUREWR	Input	IEEE-1500 wrapper serial port capture
UPDATEWR	Input	IEEE-1500 wrapper serial port update
WSI	Input	IEEE-1500 wrapper serial port data in
WSO[a:h]	Output	IEEE-1500 wrapper serial port data out
NC	–	**No connect pad:** Electrically isolated
NOBUMP	–	**Depopulated pad:** Reserved as test pad for probing
V_{SS}	Supply	Ground
V_{DDC}, V_{DDQ}, V_{PP}	Supply	Power supply

Note: 1. Index [a:h] represents the channel indicator "a" to "h" of the HBM device; Signal names including the channel indicator are used whenever more than one channel is referenced, as, for example, with the HBM ballout. The channel indicator is omitted whenever features and functions common to all channels are described.

Package Dimensions

Figure 2: Mechanical Outline (Top View)



Note: 1. Refer to JEDEC MO-316.

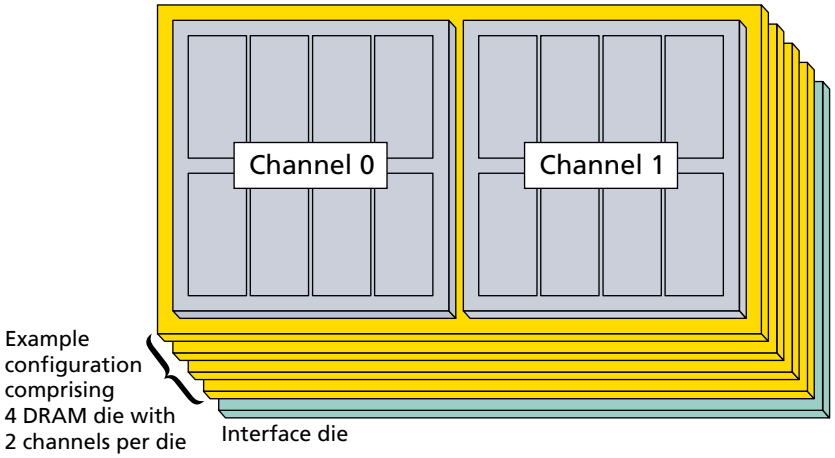
Functional Description

HBM DRAM Organization

The HBM DRAM is optimized for high-bandwidth operation to a stack of multiple DRAM devices across a number of independent interfaces (channels). It is anticipated that each DRAM stack will support up to 8 channels. The figure below shows an example stack containing four DRAM die. Each die supports two channels and contributes additional capacity and additional channels to the stack (up to a maximum of 8 channels per stack).

Each channel provides access to an independent set of DRAM banks. Requests from one channel do not access data attached to a different channel. Channels are independently clocked and need not be synchronous.

Figure 3: HBM DRAM Stack With Channels



The division of channels among the DRAM die within a stack is irrelevant to the memory controller. The example above, with the memory for two channels implemented on each die, is not a required organization.

Because each channel is independent, much of this document will describe a single channel. Where signal names are used, families of signals belonging to a given channel will have the suffix a, b, … , h for channels a through h; if no suffix is present, the signal(s) being described are generic instances of the various per-channel signals.

Channel Definition

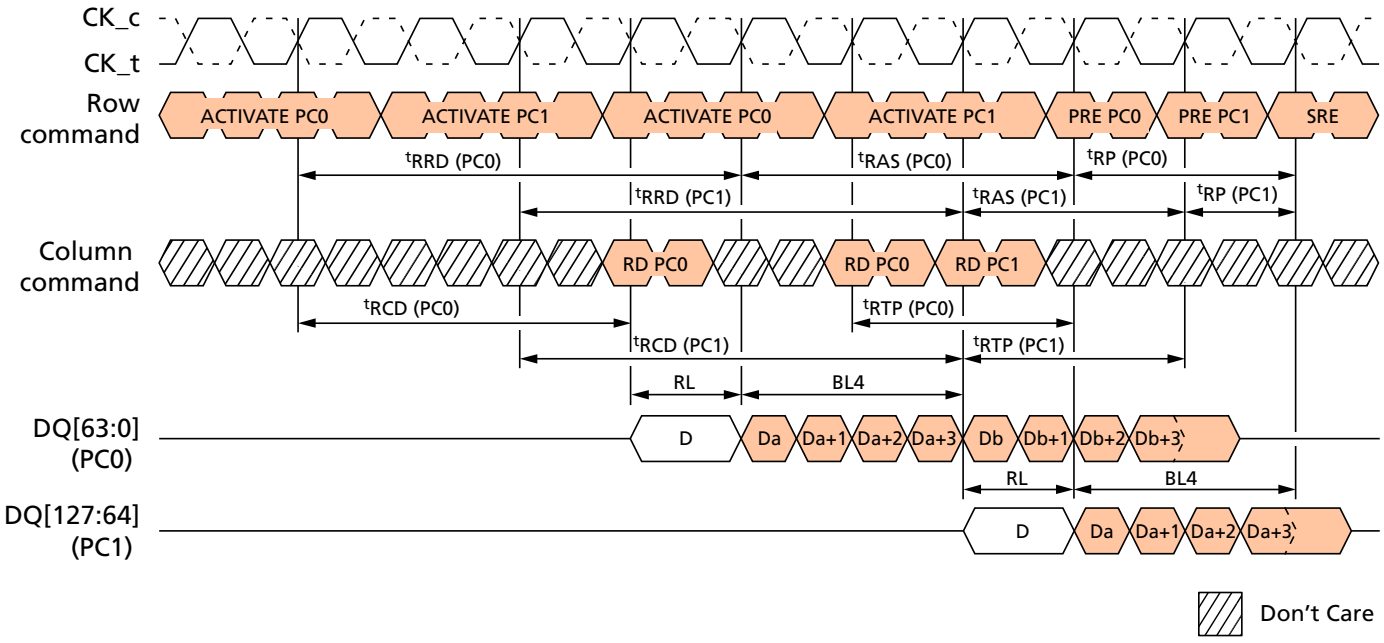
A channel provides access to a discrete pool of memory. Channels are individually clocked and need not to operate synchronously. Each channel consists of an independent command and data interface comprising 214 I/O signals. Reset and temperature signals are common to all channels. See Table 1 (page 4) for a complete signal list including 15 additional global signals associated with the IEEE1500 test access port.

Pseudo Channel Mode

Pseudo channel (PC) mode divides a channel into two individual subchannels of 64-bit I/O each, providing 256-bit prefetch per memory read and write access for each pseudo channel.

Both pseudo channels operate semi-independently: They share the channel's row and column command bus as well as CK and CKE inputs, but decode and execute commands individually as illustrated in the figure below. Address BA4 is used to direct commands to either to pseudo channel 0 (PC0, BA4 = 0) or pseudo channel 1 (PC1, BA4 = 1). Power-down and self refresh are common to both pseudo channels due to a shared CKE pin.

Figure 4: Pseudo Channel Mode Operation



Notes:
1. PC0 = pseudo channel 0 (BA4 = 0); PC1 = pseudo channel 1 (BA4 = 1).
2. RL = 1 is shown as an example. Other timing parameters (^{t}MRD, ^{t}RRD, ^{t}RAS, ^{t}RP, and ^{t}RTP) are not to scale.
3. Self refresh entry (SRE) requires that ^{t}RP is satisfied in both pseudo channels.

Array access timings as listed are applicable for each individual pseudo channel. For example, an ACTIVATE to PC0 can be followed by an ACTIVATE to PC1 as shown Figure 4. However a subsequent ACTIVATE to PC0 can only be done after ^{t}RRD (PC0). For commands that are common to both pseudo channels (PDE, PDX, SRE, SRX, and MRS) it is required that the respective timing conditions are met by both pseudo channels when issuing that command. A fixed burst length of 4 is associated with pseudo channel mode. Both pseudo channels also share the channel's mode registers. All I/O signals of DWORD0 and DWORD1 are associated with PC0, and all I/O signals of DWORD2 and DWORD3 with PC1.

Addressing

Table 2: Channel Addressing

Parameter	8GB	16GB
Density per channel	8Gb	16Gb
Density per pseudo channel (PC)	4Gb	8Gb
Prefetch size per PC (bits)	256	256
Bank address	BA[3:0]	SID, BA[3:0]
Row address	RA[14:0]	RA[14:0]
Column address	CA[5:1]	CA[5:1]
Page size (per PC)	1KB	1KB
Refresh	8K/32ms	8K/32ms
Refresh period	3.9µs	3.9µs

Notes:
1. Prefetch size and page size reflect the effective addressing along with row and column commands. Both do not include the ECC bits.
2. The burst order of a BL4 burst is fixed for reads and writes, and the HBM device does not assign column address bits to distinguish between the four UI of a BL4 burst. A memory controller may internally assign such column address bits but those column address bits are not transmitted to the HBM device.
3. Page Size = $2^{COLBITS}$ × (prefetch size/8); where COLBITS is the number of column address bits.
4. An additional address bit BA4 is provided for row and column commands to direct commands either to pseudo channel 0 (BA4 = 0) or pseudo channel 1 (BA4 = 1).

Operating Conditions

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DDC}	Voltage on V_{DDC} pin relative to V_{SS}	–0.3	1.5	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.3	1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.3	3.0	V	3
V_{IN}/V_{OUT}	Voltage on any pins relative to V_{SS}	–0.3	1.5	V	
T_{STG}	Storage temperature	–55	125	°C	2

Notes:
1. Refer to HBM Power-Up and Initialization Sequence for the relationship between power supplies.
2. Storage temperature is the case surface temperature on the center/top side of the HBM device. For the measurement conditions, please refer to the JESD51-2 standard.
3. V_{PP} must be equal or greater than V_{DDC} and V_{DDQ} at all times the device is powered-up.

Thermal Characteristics

Table 4: Thermal Characteristics

Symbol	Parameter[1]	Value	Unit	Notes
T_{OPER}	Operating temperature	0 to 95	°C	1

Note:
1. Operating temperature is the back side temperature of center of the HBM DRAM.

DC and AC Operating Conditions

Table 5: DC and AC Operating Conditions

Symbol	Parameter	Min	typ	Max	Unit	Notes
V_{DDC}	Core supply voltage	1.14	1.2	1.26	V	1, 2
V_{DDQ}	Output supply voltage	1.14	1.2	1.26	V	1, 2
V_{PP}	Pump voltage	2.375	2.5	2.75	V	2
V_{IH}	Input HIGH voltage	0.7 × V_{DDQ}	–	–	V	3
V_{IL}	Input LOW voltage	–	–	0.3 × V_{DDQ}	V	3
V_{IHD}	Differential input HIGH voltage	V_{REF} + 0.2	–	–	V	4
V_{ILD}	Differential input LOW voltage	–	–	V_{REF} - 0.2	V	4
V_{IHR}	Input HIGH voltage for RESET_n and WRST_n	0.8 × V_{DDQ}	–	–	V	
V_{ILR}	Input LOW voltage for RESET_n and WRST_n	–	–	0.2 × V_{DDQ}	V	
V_{OH}	Output HIGH voltage	0.7 × V_{DDQ}	–	–	V	
V_{OL}	Output LOW voltage	–	–	0.3 × V_{DDQ}	V	

Notes:
1. V_{DDC} and V_{DDQ} supplies are independent and must not be tied together internally on the HBM DRAM. HBM DRAM must tolerate separate V_{DDC} and V_{DDQ} power supply regulators.
2. The voltage ranges are defined at the HBM DRAM micropillars. DC bandwidth is limited to 20 MHz.
3. CMOS input receivers enabled. For CK_t, CK_c, CKE, C, R, DQ, DBI, DM, PAR, WDQS_t, WDQS_c, WRCK, SELECTWIR, SHIFTWR, CAPTUREWR, UPDATEWR, and WSI inputs.
4. V_{REF} based input receiver enabled. For CK_t, CK_c, CKE, C, R, DQ, DBI, DM, PAR, WDQS_t, and WDQS_c inputs.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.